SSD Project

Design MOSFET (Silvaco)

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Instructor

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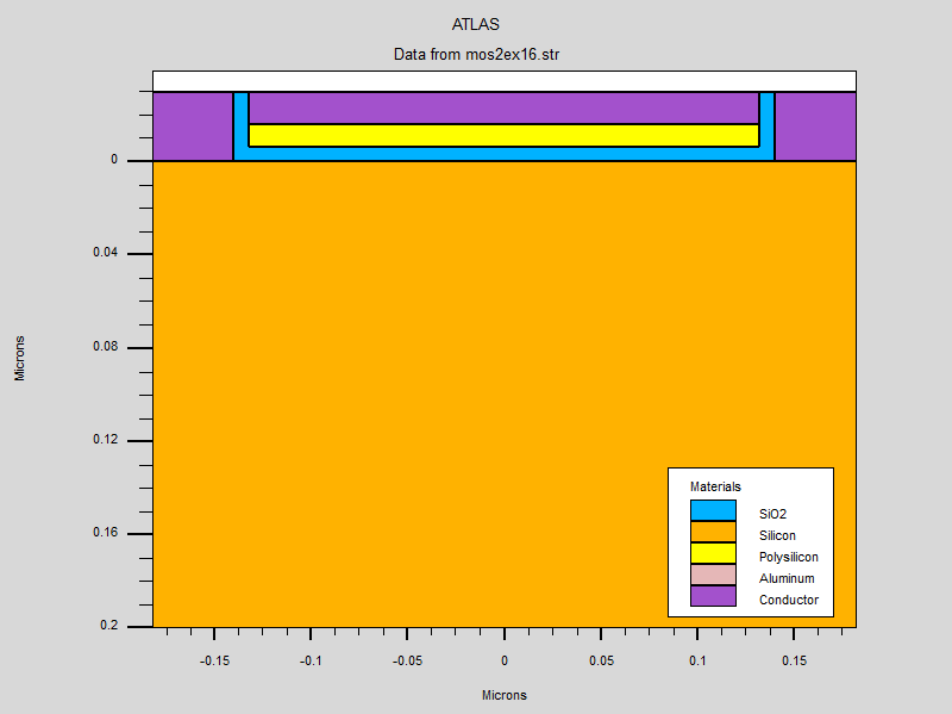
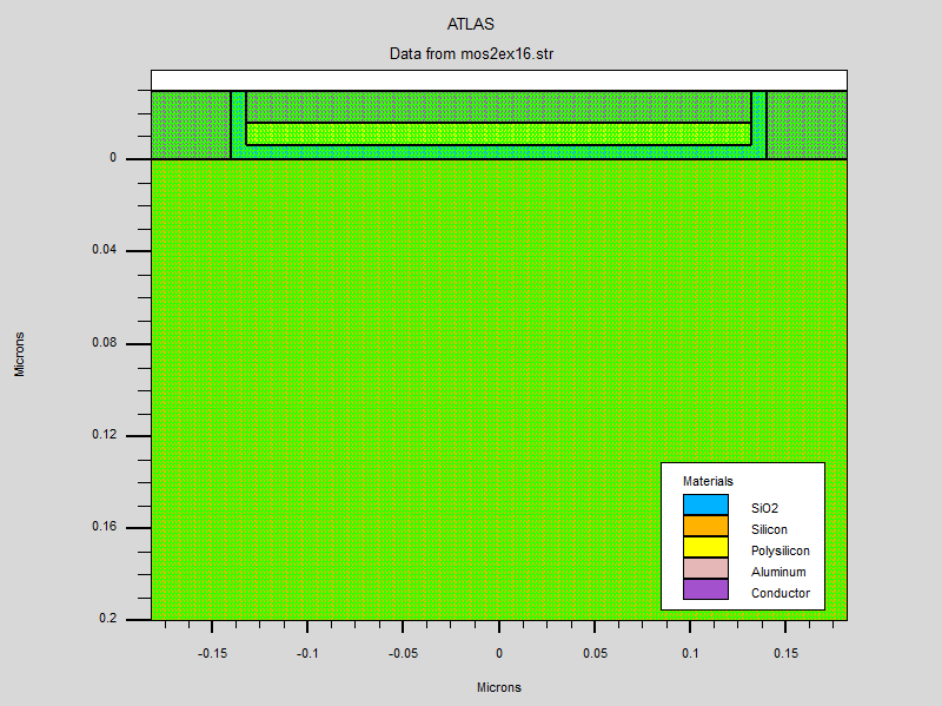
I. Structure

To scale from 90nm to 250nm technology we will use the following:
k =(10/7)= 1.43 as we go from the later tech to old one.
The 250nm technology is 3 generations older than 90nm technology.
Vdd = 1.2* 1.43^3 = 3.4985
Metallurgical gate length L= 90nm * 1.43^3 = 262.39nm
Width = 1234 nm
Gate oxide thickness = 2nm * 1.43^3 = 5.83nm
Qss= +5x10^10 electron charges/cm^2
Source/Drain (S/D) junction depth= 60nm * 1.43^3 = 174.92 nm
Source/Drain (S/D) doping = 1x10^19cm^-3 * 1.43^-3 = 3.43*10^18 cm^-3
Source/Drain (S/D) doping area = 1376970.242 nm^2
Polysilicon gate.
Channel/substrate doping: 1x10^18 cm^-3 * 1.43^-3 = 3.43*10^17 cm^-3
Body depth (substrate) 200 nm



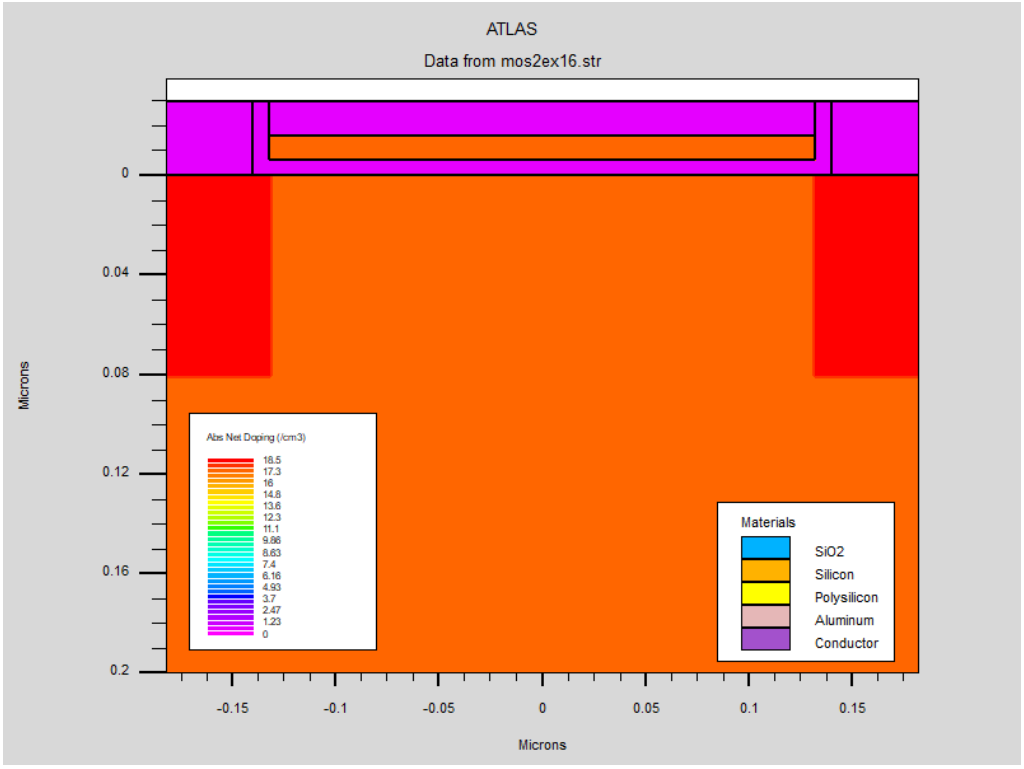
II. Mesh

The mesh density is higher in critical areas such as the channel, source, and drain regions.



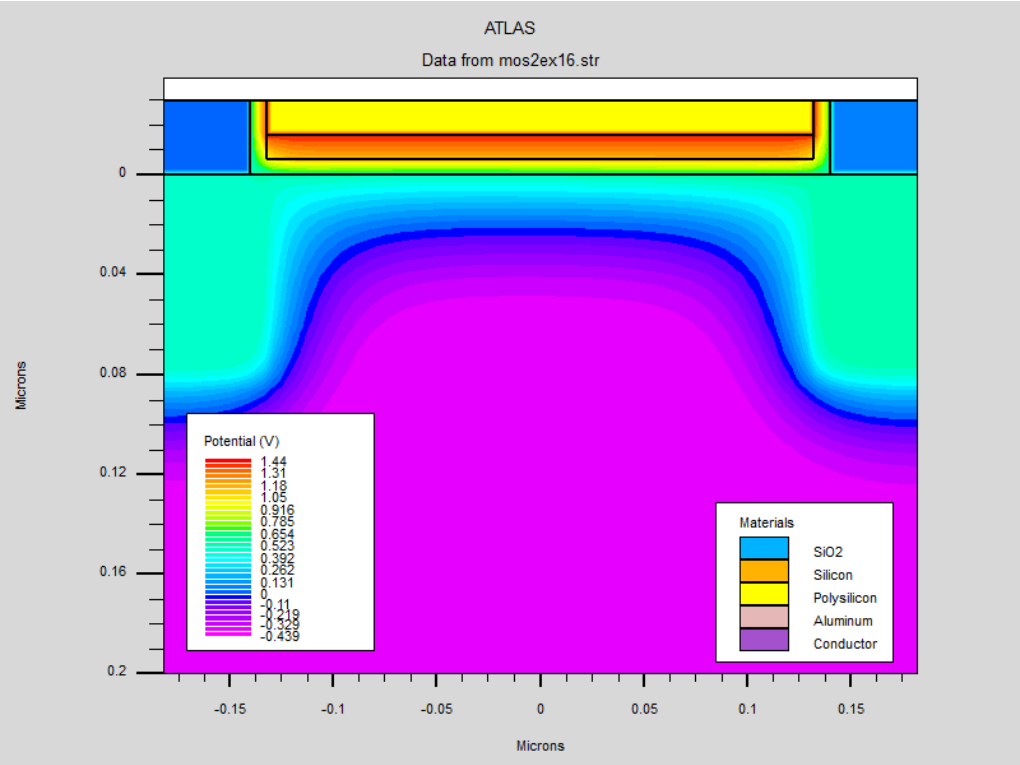
III. Doping

The doping concentration reaches its peak at the source and drain regions, measuring $3.43 * 10^{18}\ cm^{-3}$. Similarly, the polysilicon region also exhibits the highest doping level.



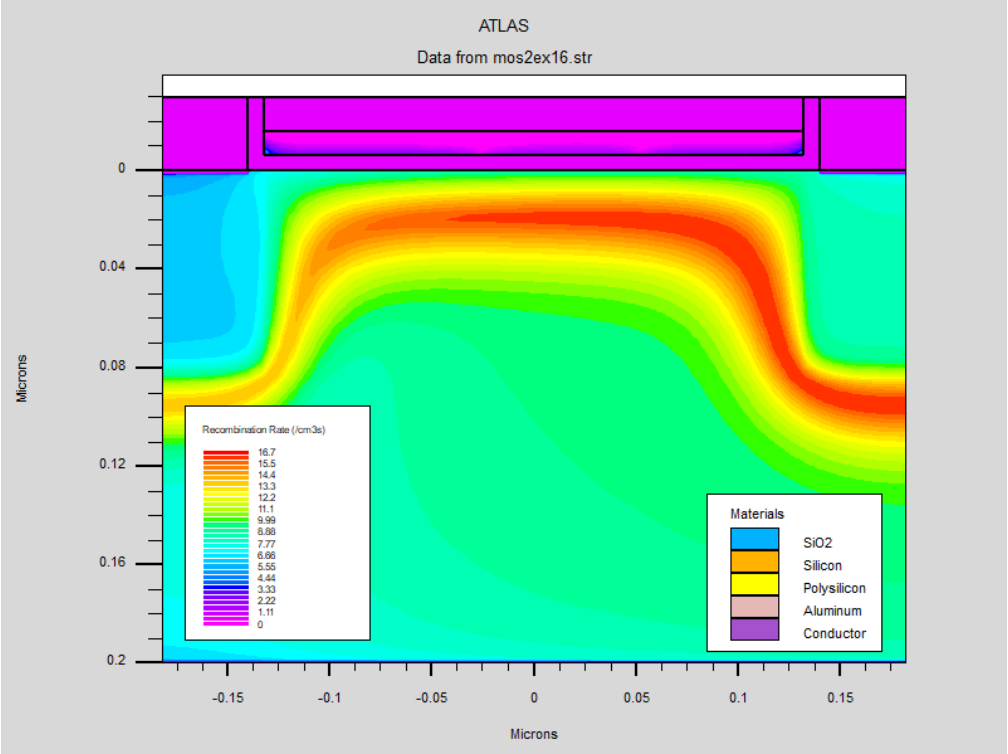
IV. Electrostatic potential

The electrostatic potential in the gate region is determined by the gate voltage. When a positive gate voltage (Vgs) is applied, it attracts electrons from the source region. This accumulation of electrons forms an inversion layer in the channel region, resulting in a decrease in the potential.



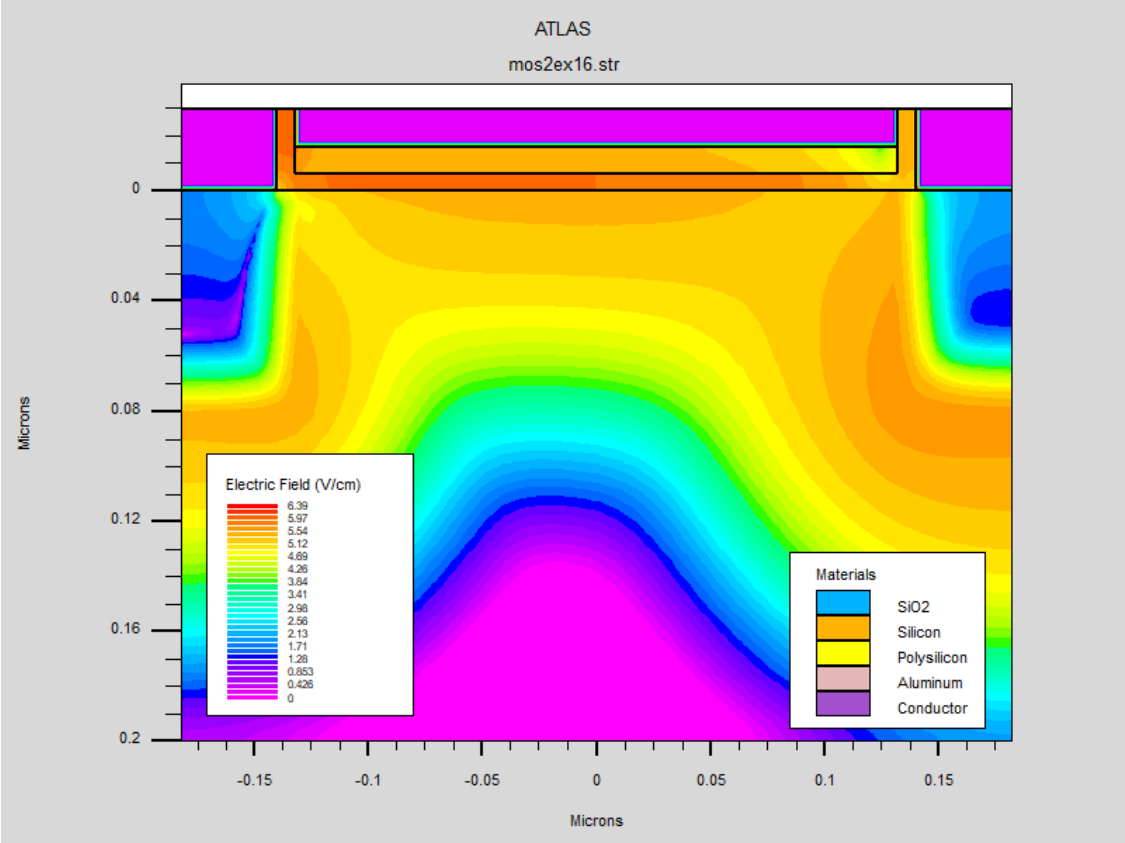
V. Recombination Rate

The recombination rate within a MOSFET device pertains to the speed at which minority carriers (holes in an n-type MOSFET or electrons in a p-type MOSFET) combine with majority carriers (electrons in an n-type MOSFET or holes in a p-type MOSFET) within the channel region. Recombination can transpire through diverse mechanisms, including Shockley-Read-Hall recombination.



VI. Electric Field

Due to the high doping in the polysilicon region, the interface between the polysilicon region and the oxide region experiences the highest electric field intensity.

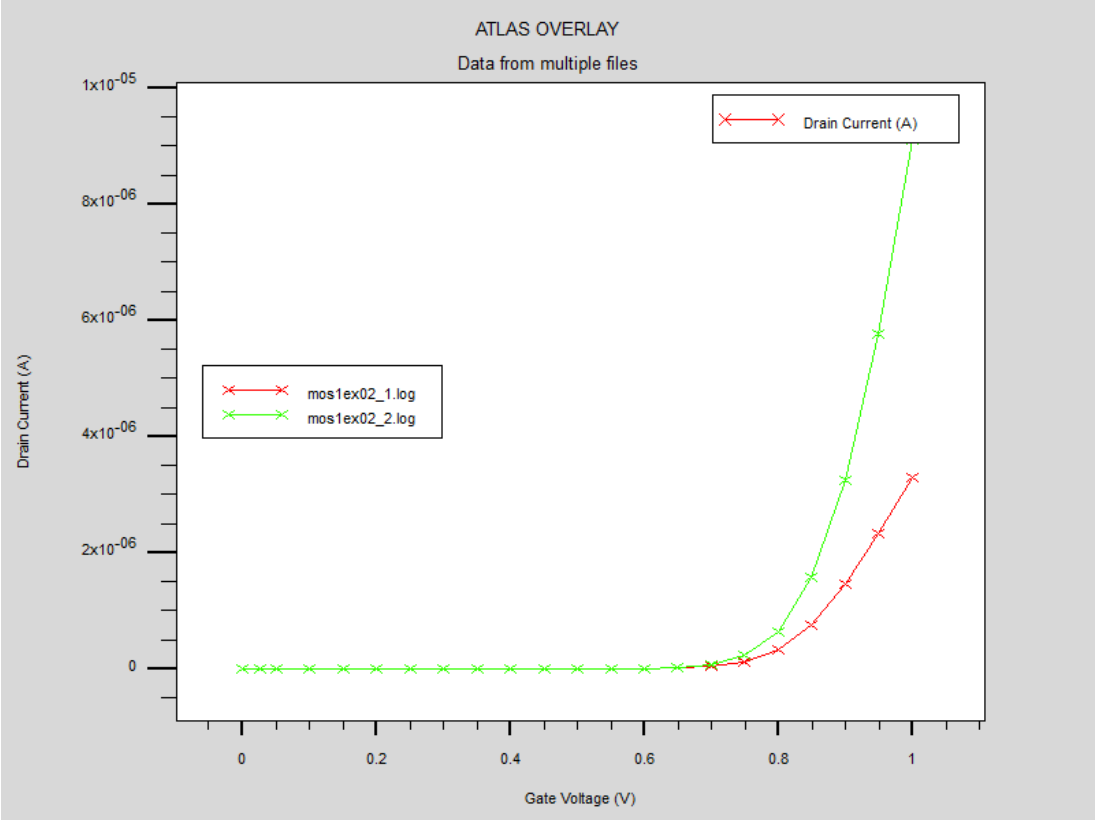


VII. Ids-Vgs showing relationship in subthreshold, linear and saturation regimes (Vd= 50 mV and Vd = 1.2 V).

In the subthreshold regime, the MOSFET functions when the gate-source voltage (Vgs) is below the threshold voltage (Vt), and the drain current (Ids) is exponentially related to Vgs. The equation describing the relationship between Ids and Vgs in this regime is Ids = Id0 * exp[(Vgs - Vt)/nVt], where Id0 represents the drain current at Vgs = Vt, n is the subthreshold slope factor, and Vt/n denotes the thermal voltage.

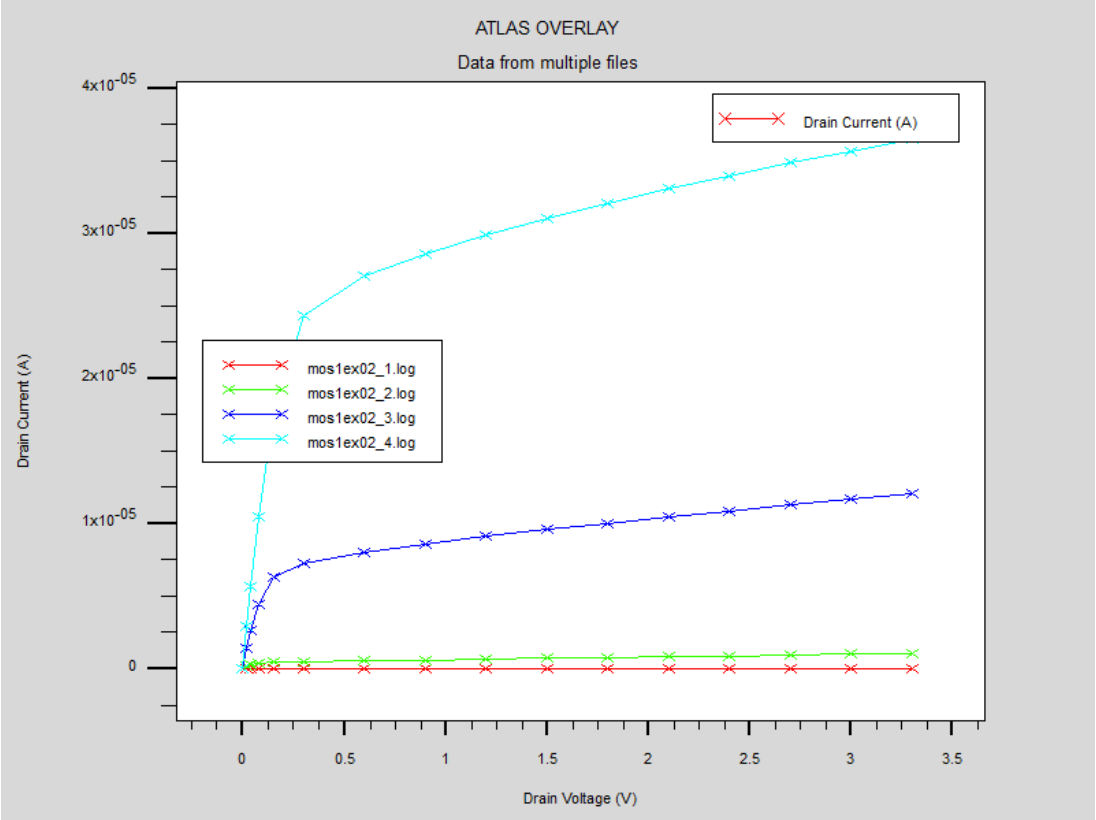
Moving to the linear regime, the MOSFET operates when Vgs exceeds the threshold voltage (Vt), and the drain current is directly proportional to Vgs - Vt.

In the saturation regime, the MOSFET operates with Vgs greater than the threshold voltage (Vgs > Vt), and the drain current remains relatively constant regardless of Vgs. The relationship between Ids and Vgs in this regime can be described by:



VIII. Ids-Vds for Vgs Values of 0.5, 0.8, 1 and 1.2 V showing subthreshold, linear and saturation regimes.

The plot depicts the Ids-Vds characteristics at a Vgs of 0.5V, showcasing the response of drain current for different Vds values. As Vds increases, the drain current experiences an initial rapid growth, but eventually reaches a saturation point where further Vds increment has a minimal impact on the current flow. Similarly, for Vgs values of 0.8V, 1V, and 1.2V, the graph illustrates the corresponding behavior of Ids-Vds. These curves may exhibit variations in terms of saturation current levels, slopes, and the voltage ranges where the drain current remains relatively constant.



IX. Show is the saturation region performance limited by pinch-off or velocity saturation in short channel? (By looking at the curves).

X. Subthreshold swing value gm and gd and its dependence on Vgs at Vds =50 mV and Vds =Vdd. Explain the dependence.

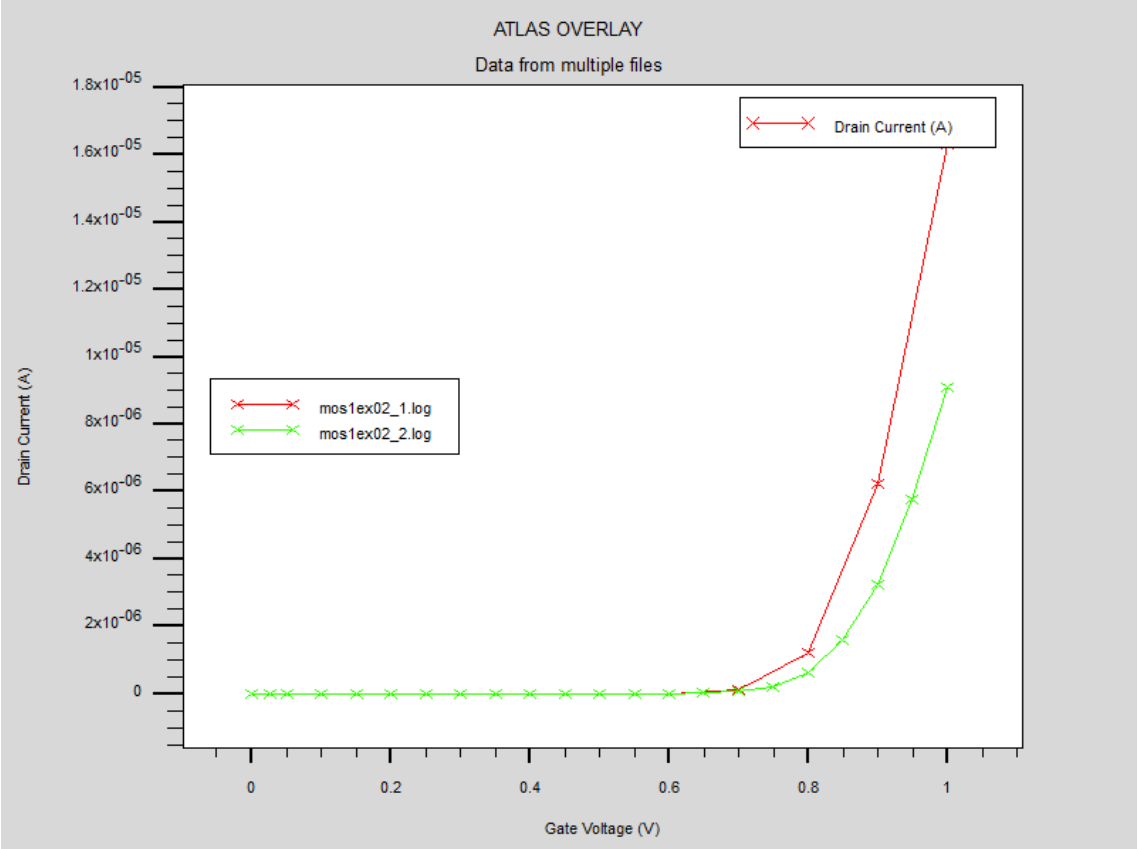
To determine gm, calculate the change in drain current (Ids) resulting from a small change in gate-to-source voltage (Vgs).

To find gd, calculate the change in drain current (Ids) caused by a small change in drain-to-source voltage (Vds).

Increasing Vgs improves control and increases carrier concentration in the channel, leading to a reduction in subthreshold swing and enhancement of gm and gd.

When the drain voltages (Vds) are low (Vds << Vdd), the MOSFET operates in the subthreshold region where the drain current exponentially depends on the gate voltage. In this case, the subthreshold swing is strongly influenced by the gate voltage, which serves as the primary factor controlling the channel current. Thus, at low Vds, an increase in Vgs is expected to decrease the subthreshold swing.

On the other hand, at high drain voltages (Vds = Vdd), the MOSFET operates in the saturation region where the drain current remains relatively independent of the gate voltage. In this scenario, the subthreshold swing depends more on the output conductance (gd) of the MOSFET, which is associated with the slope of the drain current versus drain voltage characteristic. As Vgs increases and consequently gd increases, the subthreshold swing is expected to rise with increasing Vgs at high Vds.



XI. Vth in both linear and saturation region (linear region Vds = 50 mV)

In the given diagram, the threshold voltage (Vth) of a MOSFET can be determined by analyzing the transfer characteristic, which represents the relationship between the drain current and the gate voltage. Various methods exist for extracting Vth, depending on the operating region of the device and the desired accuracy. Two commonly used methods are described below:

1. Linear region method: In this approach, the MOSFET is biased in the linear region, characterized by a small drain-source voltage (Vds), and the drain current is directly proportional to Vgs - Vth. Vth can be extracted by examining the slope of the transfer characteristic at low

drain voltages. To perform this extraction, one can either simulate or measure the MOSFET transfer characteristic at a small Vds value, such as 50 mV, and then fit a straight line to the linear portion of the curve. The threshold voltage, Vth, can be calculated as the point of intersection between the fitted line and the gate voltage axis.

2. Saturation region method: In the saturation region, the intersection point of the square root of the drain current (Id) curve with the x-axis is used to find Vth. In this case, the Vth value is determined to be 0.4 V.

XII. Gate oxide tunneling.

Gate oxide tunneling refers to the phenomenon in which electrons pass through the gate oxide of a MOSFET, resulting in leakage current and potential device failure. The gate oxide tunneling current can be determined by analyzing the gate current versus gate voltage (Ig-Vg) characteristic of the MOSFET.

One commonly employed method for extracting gate oxide tunneling is the charge pumping technique, which operates at high frequencies. In this technique, an alternating current (AC) signal is applied to the MOSFET's gate, and the resulting gate current is measured and analyzed. The AC signal causes the MOSFET channel to periodically charge and discharge, producing a pumping current that is proportionate to the gate capacitance and the channel charge. When gate oxide tunneling occurs, electrons tunnel through the gate oxide and accumulate in the channel, causing a reduction in the channel capacitance and consequently a decrease in the pumping current.

To extract the gate oxide tunneling current using the charge pumping technique, the following steps can be followed:

1. Apply an AC voltage to the MOSFET's gate, with a frequency ranging from 1 MHz to 1 GHz.
2. Measure the gate current as a function of the gate voltage using a high-impedance current meter.
3. Calculate the pumping current using the provided equation.

$$I_p = \frac{1}{2} c_g v_{PP} f$$

The pumping current (Ip) can be calculated using the equation where Cg represents the gate capacitance, Vpp denotes the peak-to-peak AC voltage, and f signifies the frequency of the AC signal.

To determine the gate oxide tunneling current, plot the pumping current against the gate voltage and extract it as the difference between the total gate current and the pumping current.

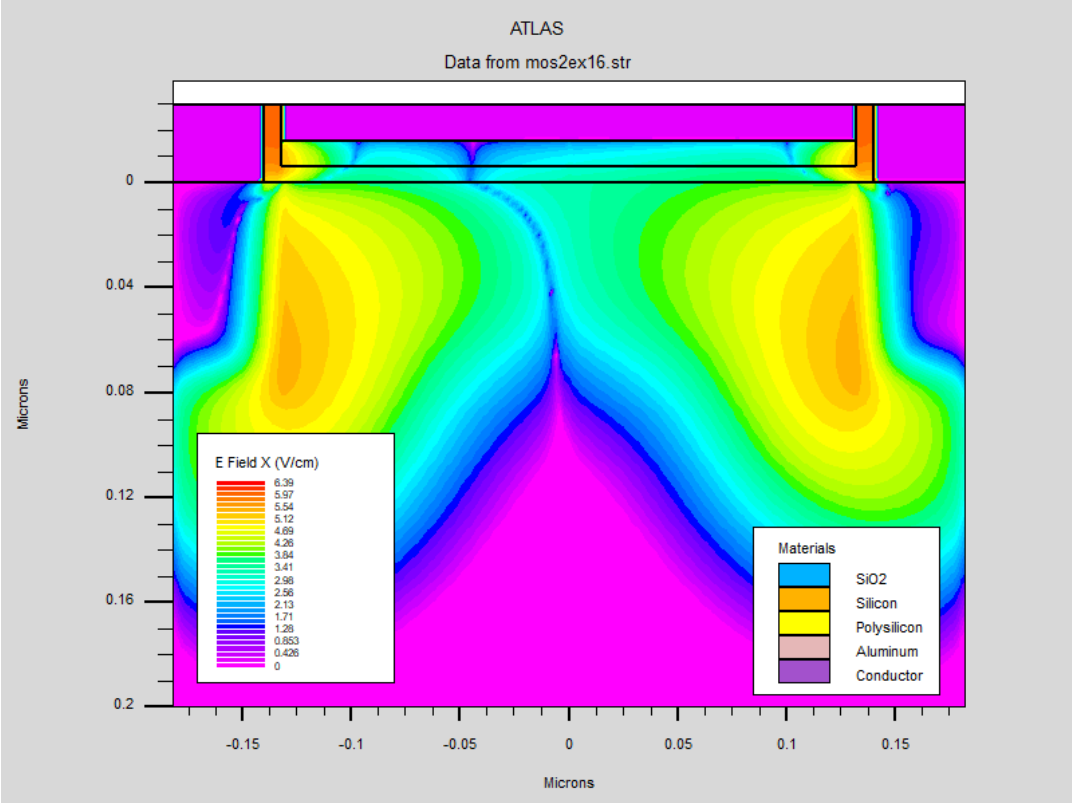
To accurately account for other contributors to the gate current, such as interface states and band-to-band tunneling, the gate oxide tunneling current can be obtained by subtracting the pumping current from the total gate current at each gate voltage.

XIII. Electron density along the x and y directions, and explain the dependence.

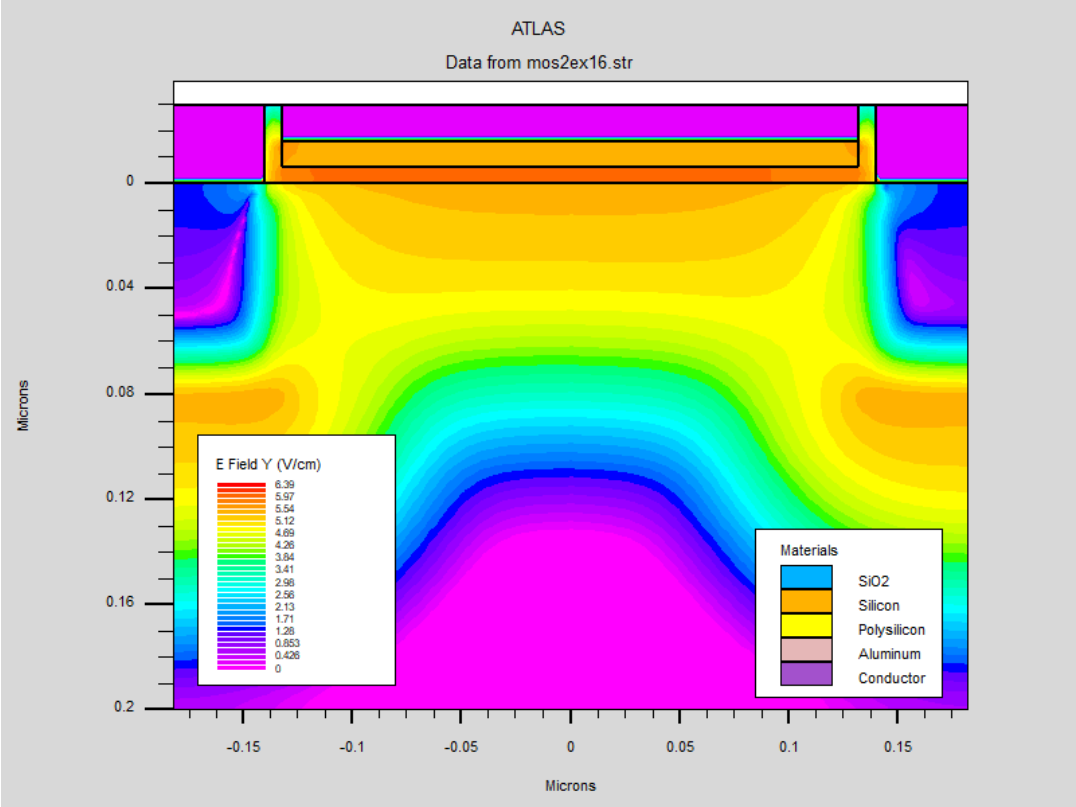
The channel region, located between the source and drain terminals, exhibits the highest electron density. The conductivity and performance of the device are determined by the gate voltage (Vgs) applied to the transistor, which governs the electron density in the channel. The primary factors influencing the electron density in an NMOS transistor are the applied gate voltage (Vgs) and the threshold voltage (Vth).

XIV. Longitudinal and transverse electric filed, explain the contour graph.

The transverse electric field, perpendicular to the channel direction, facilitates the movement of carriers across the channel. It arises from the voltage applied to the drain and is directly proportional to the drain-source voltage. As the drain voltage rises, the transverse electric field intensifies, leading to an increased current flow between the source and drain.

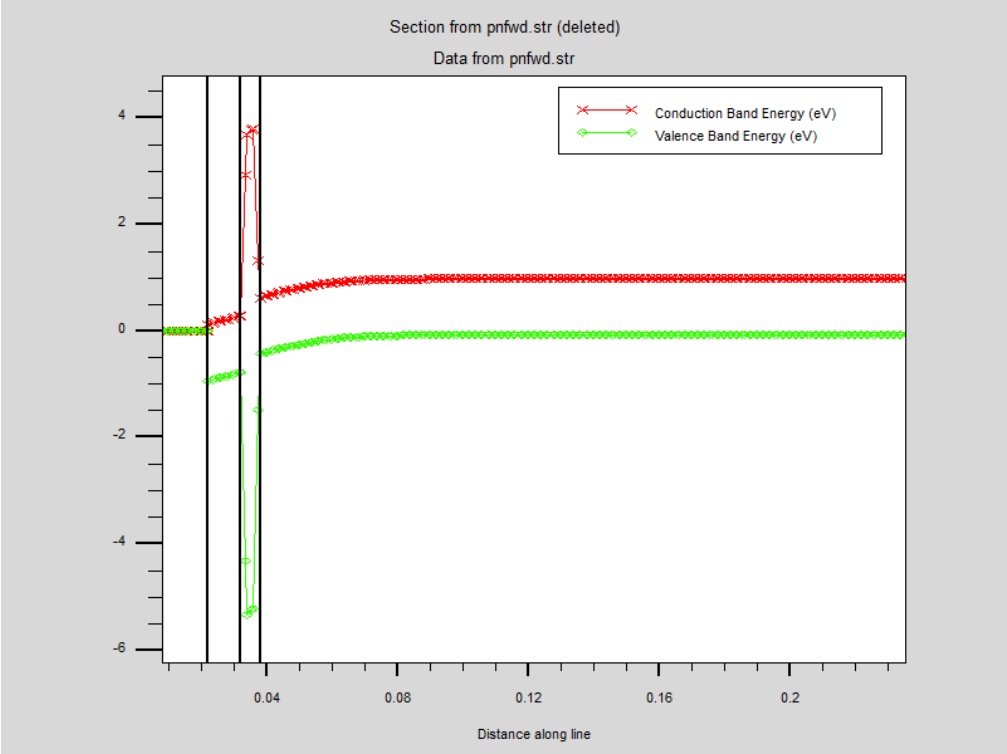


The longitudinal electric field, aligned with the channel direction, facilitates the movement of carriers along the channel. It originates from the voltage applied to the gate and is directly proportional to the gate-source voltage. As the gate voltage increases, the longitudinal electric field strengthens, leading to an amplified current flow between the source and drain.



XV. Drain induced barrier lowering (DIBL), explaining its behavior. Draw the band diagram and the IV-curve.

The nMOS band diagram visually illustrates the energy levels, charge carriers, and electron behavior within the device, aiding in the comprehension of how voltage application and device doping affect its semiconductor operation.



XVI. Channel length modulation parameter, explain how does it affect the IV characteristics and why compared to long channel.

XVII. Extract channel effective mobility curve and explain its dependence on Vgs, and Vds.

The parameter known as the effective channel mobility (μeff) characterizes the movement capability of carriers within a MOSFET's channel when subjected to an electric field. Several factors, including doping concentration, temperature, gate oxide thickness, and electric field in the channel, influence μeff. To determine the μeff curve of a MOSFET, one can conduct measurements or simulations of the drain current versus gate voltage (Ids-Vgs) at various drain-source voltage (Vds) values. By employing the following equation, the μeff value can be derived.

$$\mu_{eff} = \frac{I_d}{WC_{ox}V_{ds} * (V_{gs} - V_{th})}$$

The drain current (Id) is influenced by several factors, including the channel width (W), gate oxide capacitance per unit area (Cox), drain-source voltage (Vds), gate-source voltage (Vgs), and threshold voltage (Vth). To extract the μeff value, the drain current versus gate voltage (Ids-Vgs) can be measured or simulated for different Vds values, utilizing the equation:

By plotting the μeff curve as a function of Vgs for various Vds values, insights into the MOSFET's behavior can be obtained. Generally, μeff increases as Vgs rises due to an enhanced electric field in the channel, subsequently improving carrier mobility. Furthermore, μeff is also affected by Vds as the electric field in the channel fluctuates, influencing carrier mobility.

During operation in the linear region at low Vds, μeff remains relatively constant and primarily relies on doping concentration and temperature. In this region, μeff shows minimal dependence on Vds, whereas its relationship with Vgs becomes more pronounced.

Conversely, during operation in the saturation region at high Vds, the channel experiences a high electric field, leading to various effects like velocity saturation and impact ionization that affect carrier mobility. Consequently, μeff may decrease with increasing Vds due to carrier depletion and saturation of carrier velocity.

XVIII. For short channel effect, Run Ids-Vgs simulations with Vds = Vdd (corresponding tothe saturation region of operation), for gate length values of 40, 60, 90 and 130nm, while keeping all other parameters constant.

XIX. Manually extract the saturation threshold voltage (VTsat) for each simulated curve and plot VTsat vs channel length to see the short channel effect.

To determine the saturation threshold voltage (VTsat) for each simulated curve, it is necessary to plot the drain current (Ids) against the gate voltage (Vgs) at a fixed drain-source voltage (Vds = Vdd) and identify the Vgs value at which Ids saturates. VTsat is defined as the gate voltage where the drain current reaches 90% of its saturation value.

To examine the short-channel effect, we will simulate the MOSFET for various gate lengths (Lg) such as 40 nm, 60 nm, 90 nm, and 130 nm while keeping all other parameters constant. The simulation can be conducted using device simulators like TCAD or SPICE.

After simulating the MOSFET for each gate length, we can obtain the saturation threshold voltage by plotting the Ids-Vgs curve and determining the gate voltage at which Ids saturates. Subsequently, VTsat can be plotted

against Lg to observe the short-channel effect. This plot demonstrates how VTsat decreases with decreasing Lg due to the impact of the short-channel effect. The short-channel effect arises from channel depletion near the drain, which reduces the effective channel length and causes a shift in the saturation threshold voltage towards lower values. This effect becomes more significant for shorter channel lengths as the depletion region grows and influences the channel behavior. The decreasing trend in VTsat as Lg decreases on the plot reveals the impact of the short-channel effect. Furthermore, the plot enables the estimation of different design parameters' influence on the short-channel effect and facilitates device performance optimization for specific applications.

XX. Change the S/D junction depth and show its effect on Vth for different Depth values (20, 40, 60, 90 nm), can you explain why?

To investigate the impact of the source/drain (S/D) junction depth on the threshold voltage (Vth), we can simulate MOSFETs with different S/D junction depths of 20 nm, 40 nm, 60 nm, and 90 nm, while maintaining all other parameters constant. This simulation can be conducted using device simulators such as TCAD or SPICE.

After simulating the MOSFETs for each S/D junction depth, we can determine Vth by plotting the transfer characteristic curve (Ids-Vgs) and identifying the gate voltage at which the MOSFET turns on. Subsequently, Vth can be plotted against the S/D junction depth to examine the effect of S/D junction depth on Vth.

The plot of Vth versus S/D junction depth demonstrates how Vth changes as the S/D junction depth increases. When the S/D junction depth increases, the doping concentration near the channel region decreases, resulting in an expanded depletion region width and a reduction in the electric field within the channel. Consequently, Vth decreases. This effect is particularly noticeable for shorter S/D junction depths, where the doping concentration is higher and the depletion region width is smaller.

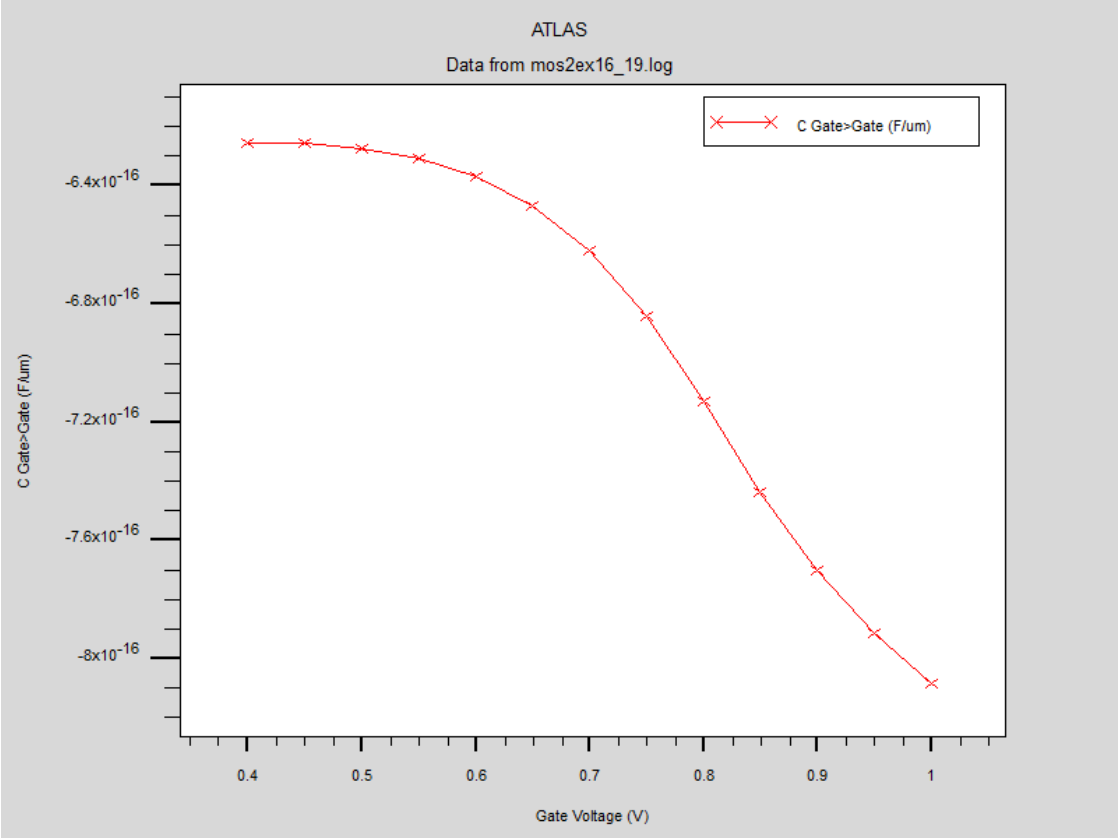
The plot will reveal a decreasing trend in Vth as the S/D junction depth increases, indicating the influence of the S/D junction depth on Vth.

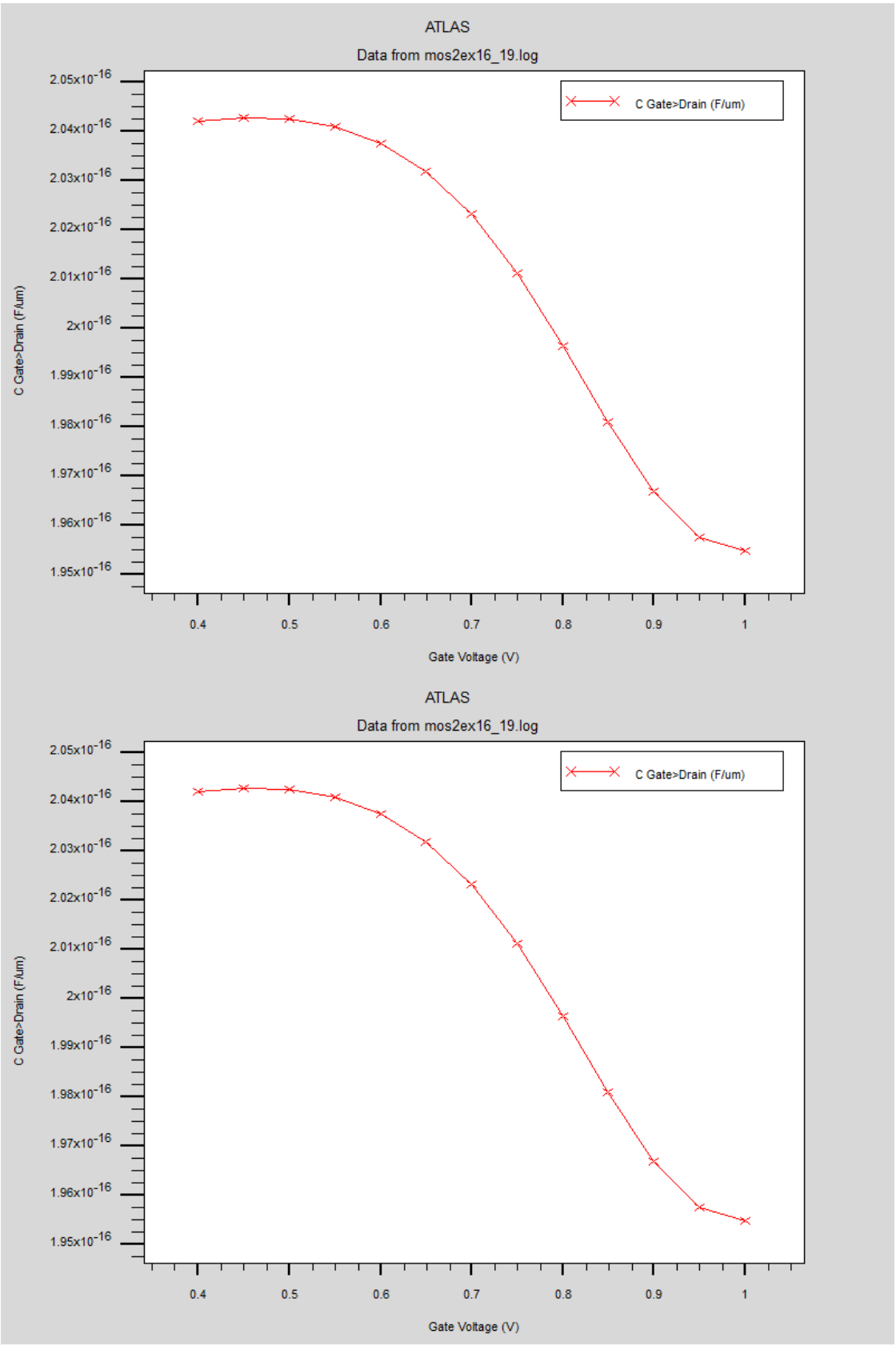
XXI. Fixing all other parameters, optimize your design again by changing channel doping, S/D doping and S/D depth to achieve ION >500 uA and IOFF < 1 nA

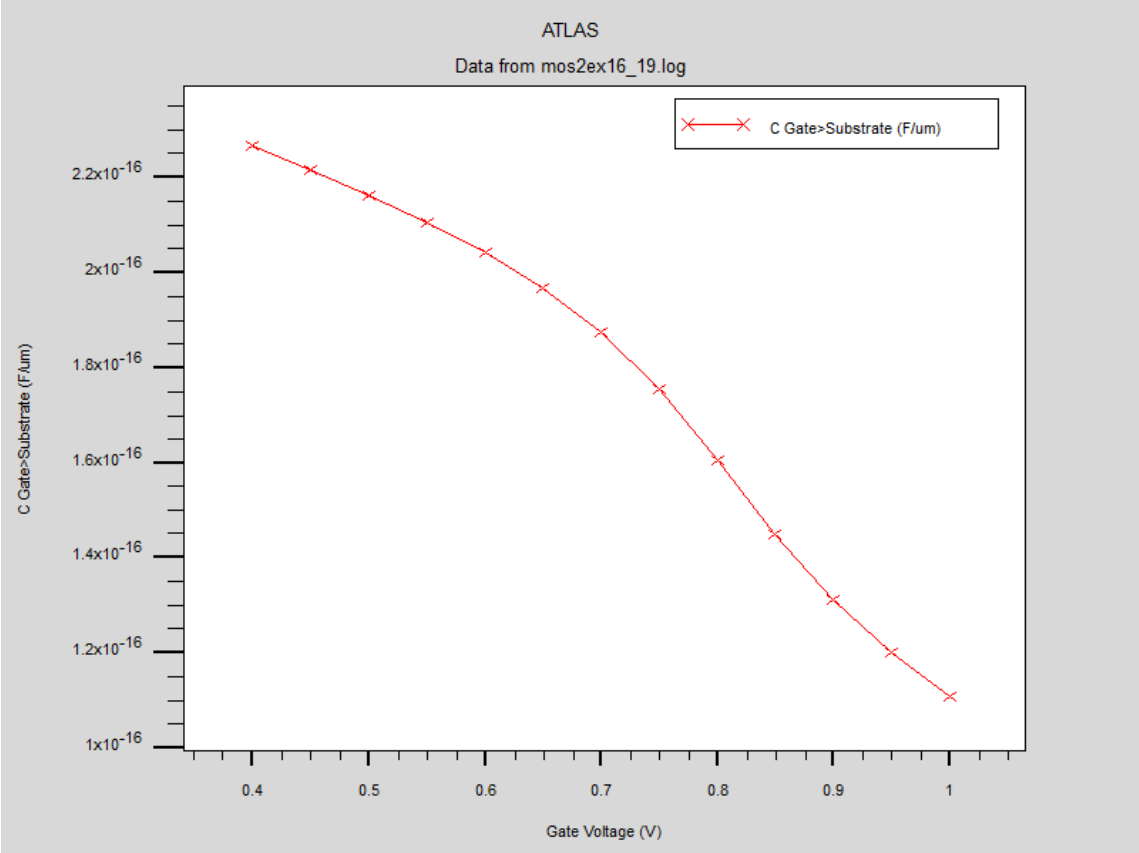
XXII. CV characteristics (Cgate, Cgs, Cgd) in both low frequency and high frequency, and verify the built-in potential.

For Low frequency:

At low frequencies, the capacitance-voltage (CV) characteristics of the MOSFET device are primarily influenced by three regions: accumulation, depletion, and inversion. In the accumulation region, the gate capacitance remains relatively constant and is predominantly determined by the oxide capacitance. In the depletion region, the gate capacitance reduces as the channel experiences a depletion of mobile carriers, leading to a decrease in Cgs (gate-source capacitance) and an increase in Cgd (gate-drain capacitance). In the inversion region, the gate capacitance is primarily governed by the charge density in the channel, resulting in a further decrease in Cgs and an increase in Cgd.

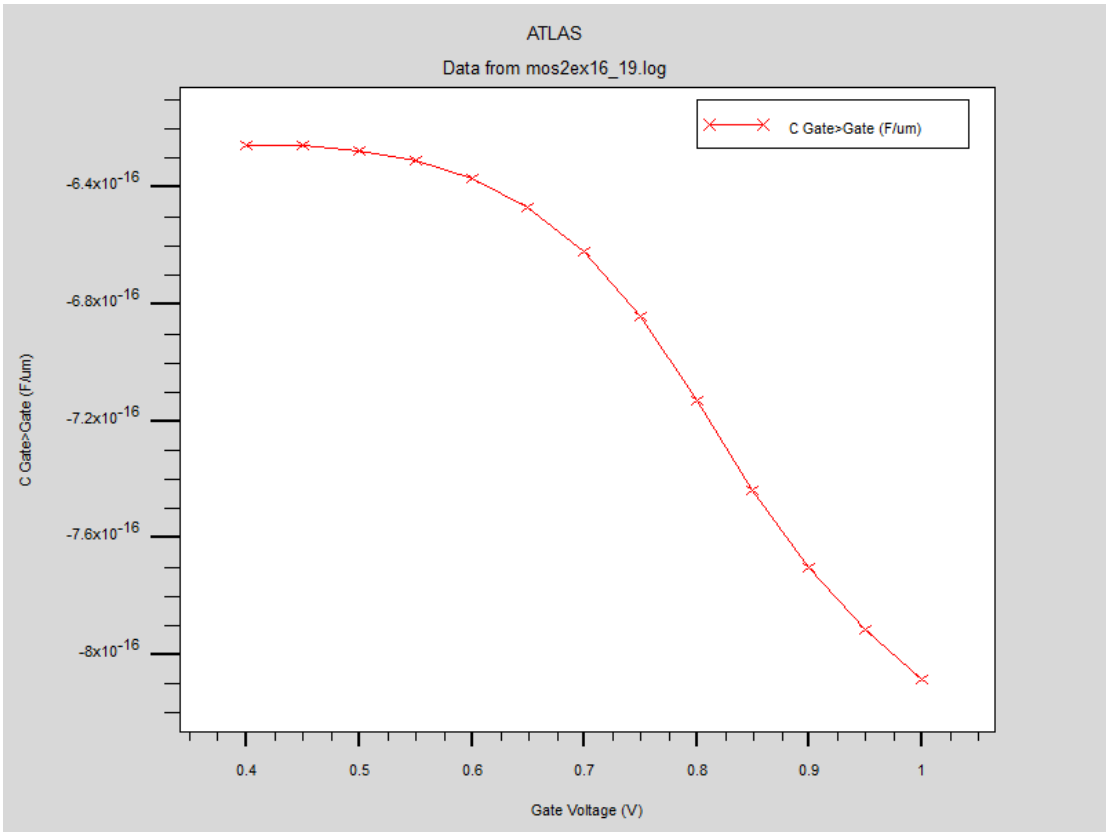


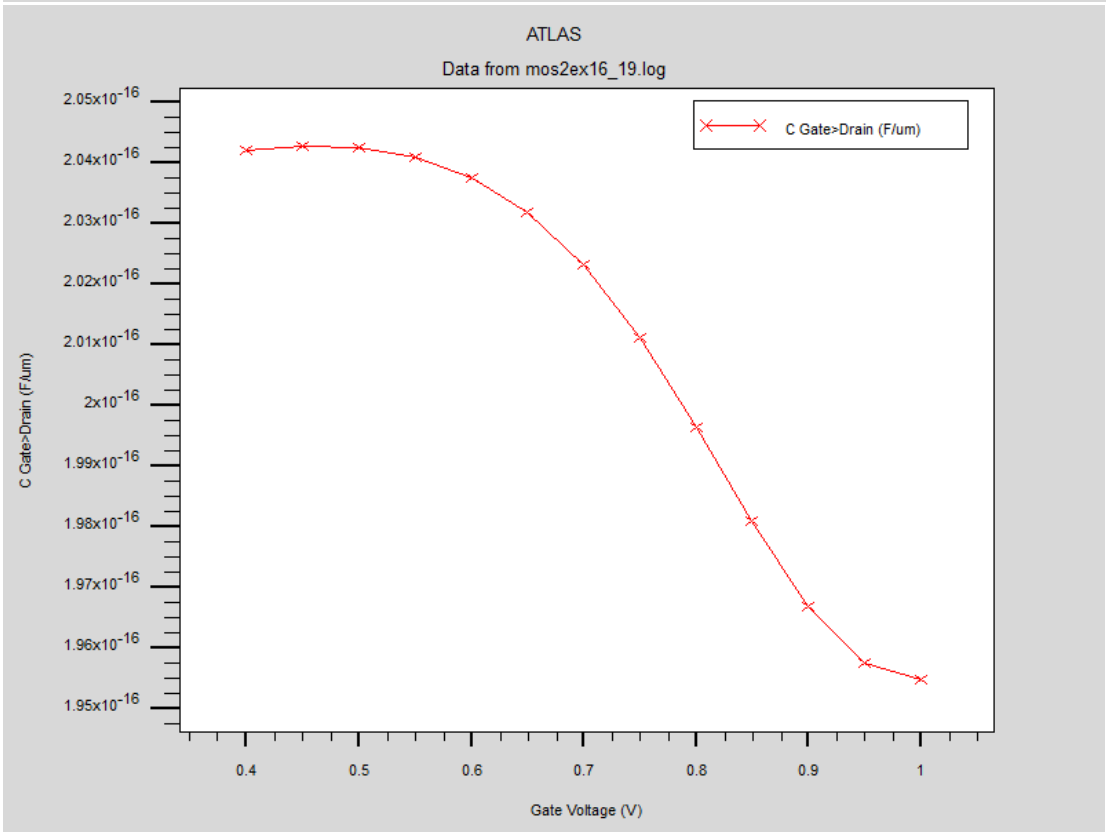

ATLAS
Data from mos2ex16_19.log
C Gate>Drain (F/um)
2.05x10^-16
2.04x10^-16
2.03x10^-16
2.02x10^-16
2.01x10^-16
2x10^-16
1.99x10^-16
1.98x10^-16
1.97x10^-16
1.96x10^-16
1.95x10^-16
0.4
0.5
0.6
0.7
0.8
0.9
1
Gate Voltage (V)
ATLAS
Data from mos2ex16_19.log
C Gate>Drain (F/um)
2.05x10^-16
2.04x10^-16
2.03x10^-16
2.02x10^-16
2.01x10^-16
2x10^-16
1.99x10^-16
1.98x10^-16
1.97x10^-16
1.96x10^-16
1.95x10^-16
0.4
0.5
0.6
0.7
0.8
0.9
1
Gate Voltage (V)

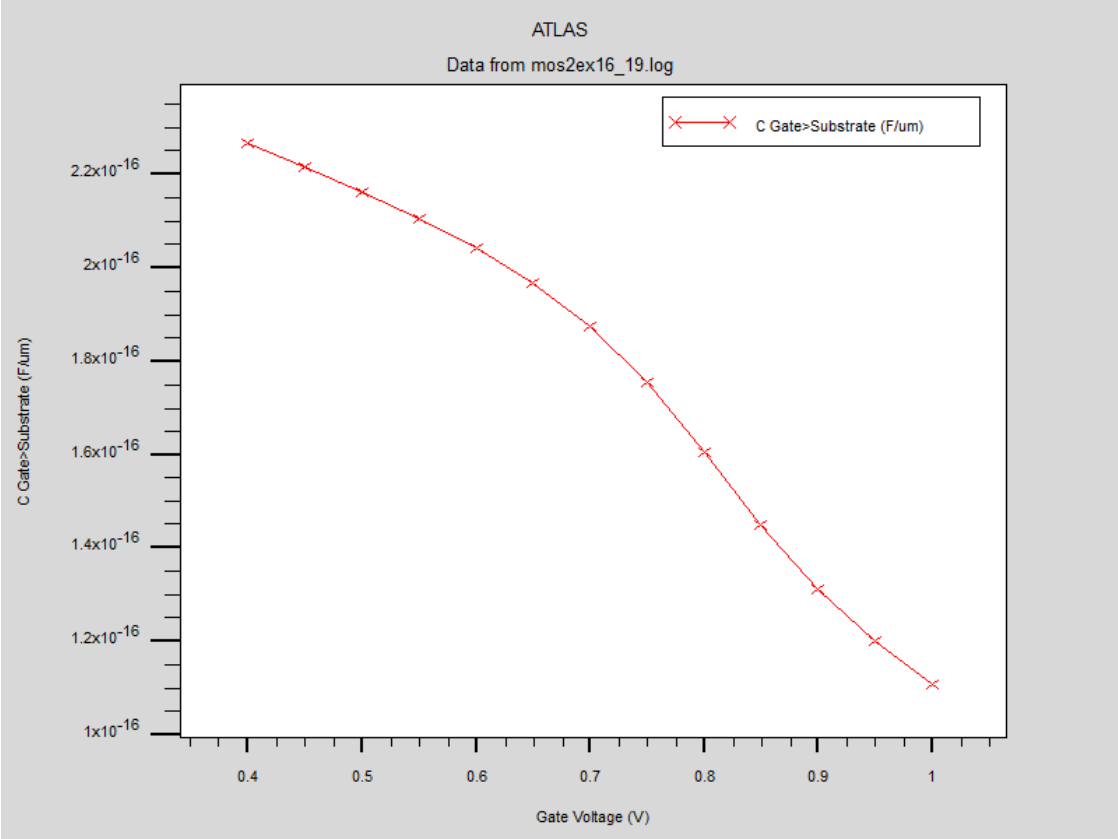


For High frequency:

At high frequencies, the capacitance-voltage (CV) characteristics of the MOSFET device are primarily influenced by parasitic effects, including series resistance and gate-source/gate-drain overlap capacitances. These parasitic effects can lead to a reduction in the gate capacitance and a shift in the CV curve towards lower voltages. Understanding the high-frequency CV characteristics is crucial for evaluating the performance of MOSFET devices in high-speed applications like digital logic circuits.


ATLAS
Data from mos2ex16_19.log
C Gate>Gate (F/um)
-6.4x10^-16
-6.8x10^-16
-7.2x10^-16
-7.6x10^-16
-8x10^-16
C Gate>Gate (F/um)
0.4
0.5
0.6
0.7
0.8
0.9
1
Gate Voltage (V)


ATLAS
Data from mos2ex16_19.log
C Gate>Drain (F/um)
2.05x10^-16
2.04x10^-16
2.03x10^-16
2.02x10^-16
2.01x10^-16
2x10^-16
1.99x10^-16
1.98x10^-16
1.97x10^-16
1.96x10^-16
1.95x10^-16
C Gate>Drain (F/um)
0.4
0.5
0.6
0.7
0.8
0.9
1
Gate Voltage (V)



The inherent voltage of a MOSFET device can be calculated by examining the CV characteristics and identifying the voltage at which the capacitance reaches its lowest value. This particular voltage indicates the moment when the depletion region spans the entire channel region, leading to the maximum width of depletion and the minimum capacitance of the gate. The built-in potential is determined by the disparity between the semiconductor's Fermi potential and the flat-band voltage of the MOSFET device.

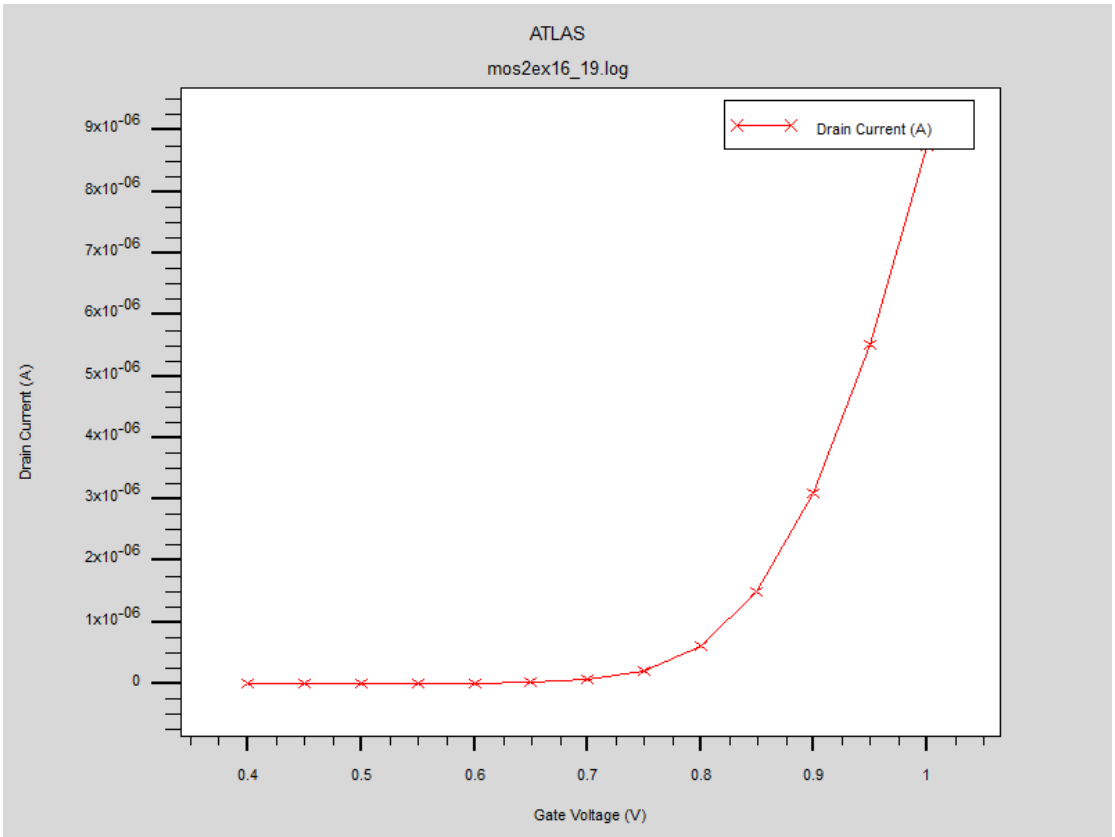
XXIII. Report the change of threshold voltage, transconductance and output resistance with temperature (from 300K to 500K).

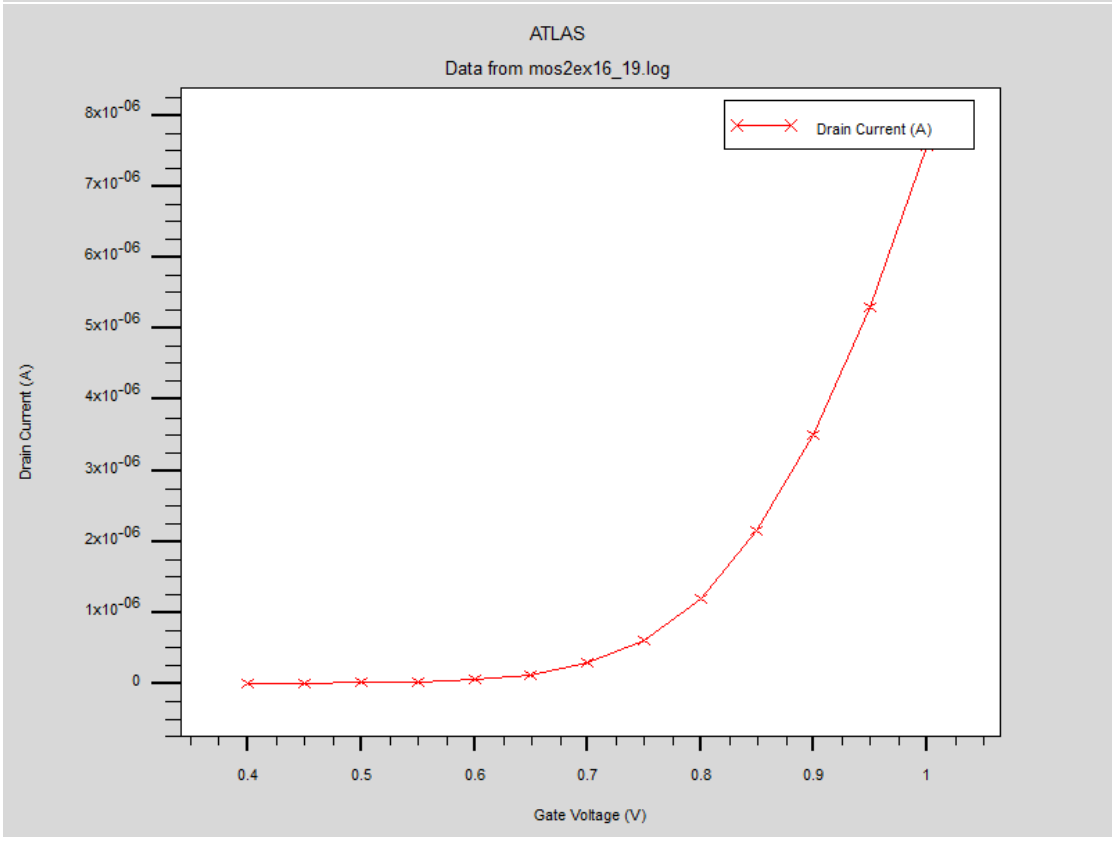
The temperature has a significant impact on the threshold voltage (Vt), transconductance (gm), and output resistance (ro) of a MOSFET device. When the temperature rises from 300K to 500K, the following changes can be expected:

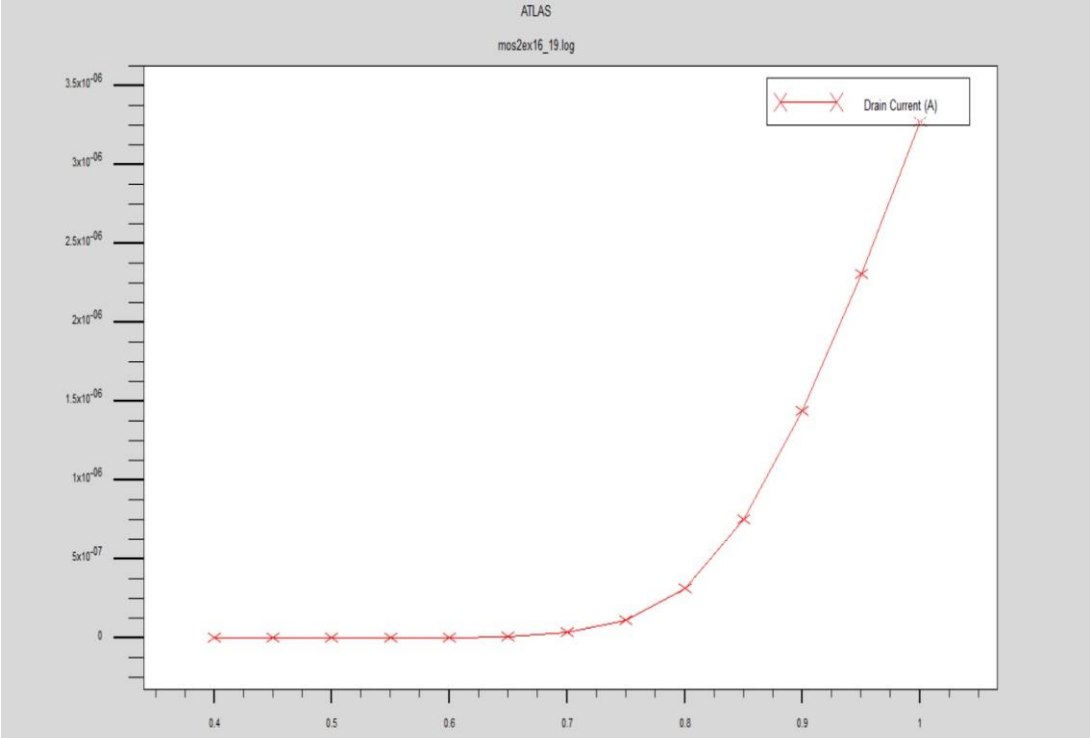
1. Threshold Voltage (Vt): The threshold voltage of a MOSFET device decreases as the temperature increases. This is because the temperature rise leads to an increase in carrier concentration, causing a decrease in the threshold voltage.

2. Transconductance (gm): The transconductance of a MOSFET device decreases with higher temperatures. This decline can be attributed to two factors: a decrease in carrier mobility and an increase in carrier scattering. The reduced mobility restricts the movement of carriers, resulting in a lower transconductance. Additionally, increased carrier scattering disrupts the flow of carriers, further reducing the transconductance.

3. Output Resistance (ro): The output resistance of a MOSFET device increases as the temperature rises. This is due to the combined effects of decreased carrier mobility and increased thermal noise. The reduced mobility hampers the flow of carriers, leading to a higher output resistance. Additionally, the increase in thermal noise affects the accuracy of signal transmission and contributes to the overall increase in output resistance.


ATLAS
mos2ex16_19.log
Drain Current (A)
9x10-06
8x10-06
7x10-06
6x10-06
5x10-06
4x10-06
3x10-06
2x10-06
1x10-06
0
0.4
0.5
0.6
0.7
0.8
0.9
1
Gate Voltage (V)


ATLAS
Data from mos2ex16_19.log
Drain Current (A)
8x10-06
7x10-06
6x10-06
5x10-06
4x10-06
3x10-06
2x10-06
1x10-06
0
0.4
0.5
0.6
0.7
0.8
0.9
1
Gate Voltage (V)



XXIV. References

[1] S.Sedra, A. and C.Smith, K., 2021. Microelectronics Circuits. 7th ed. New York: Oxford press.
[2] Neamen, D., 2012. Semiconductor Physics And Devices. 4th ed. New York: McGraw-Hill