32×12 BITS 6T SRAM

ASIC and FPGA Design - NANENG422

BY:
ABDELRAHMAN FOUDA
202001261

Design of a 32×12 bits 6T SRAM Using 65nm

I. Abstract:

This project focuses on the design and implementation of a compact 32x12 6T SRAM module using the 65nm CMOS technology in Cadence Virtuoso. The design journey involved detailed transistor-level schematics, simulation analysis, and physical layout design, ensuring optimized power and area efficiency. Key design challenges addressed include stability under minimum operating voltage and robustness against process variations. Integrated peripherals facilitate seamless embedding into broader system architectures. Utilizing the capabilities of Cadence Virtuoso and the 90nm design kit, the SRAM module demonstrated stable functionality and reliable data handling capabilities, positioning it as a suitable candidate for low-power and space-constrained applications.

II. Introduction:

6T SRAM, also known as six-transistor SRAM, is a type of memory cell prevalent in integrated circuits and microprocessors, playing a crucial role in modern electronic devices like computers, smartphones, and various digital systems. The term "6T" refers to the six transistors required to construct each memory cell. These transistors are arranged in a cross-coupled flip-flop formation, working together to reliably store a single bit of data, either a 0 or a 1. A key advantage of 6T SRAM is its ability to retain data as long as it remains powered, making it ideal for use in cache memory where fast and dependable data retrieval is necessary. Its swift read and write capabilities are well-suited for high-speed data access applications. However, 6T SRAM is not without its limitations. It occupies more space compared to other types of memory, such as DRAM (Dynamic Random-Access Memory), due to the multiple transistors each cell requires. Additionally, it tends to consume more power, which can be a drawback in low-power devices. Despite these challenges, 6T SRAM's rapid access times, non-volatility, and robustness keep it in extensive use across various fields, crucially supporting the efficient functionality of processors and other digital technology by facilitating rapid data storage and retrieval.

III. Schematic and Circuit analysis:

Below is the illustration of the 6T bit-cell schematic. Precise dimensions have been applied to guarantee its proper operation. All components are configured with a length of 65nm.

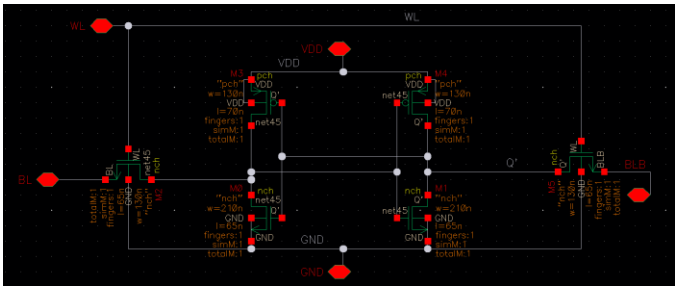

Figure 1 6T SRAM cell schematic

Pulldown Net	Pullup Net	Access net
W/L= 210/65	W/L= 130/70	W/L= 130/65
NMOS	PMOS	NMOS

As specified in the Table, the widths of the pull-down network (PDN) are set to their maximum to ensure that in scenarios where contention may arise such as when pulling the Bitline Bar to Vdd and the PDN to ground the PDN prevails. The pull-up network (PUN) is intentionally designed to be weaker than the access transistors, which have equal widths, to prevent them from pulling the Qbar to Vdd during a write operation of '1'.

IV. Layout:

A layout design for the individual bit-cell was conducted using Layout XL in Cadence, yielding an area of 6.225 µm2 for a single bit-cell, including the external

connections for Vdd, GND, and Word Line. The layout is depicted in the figure below:

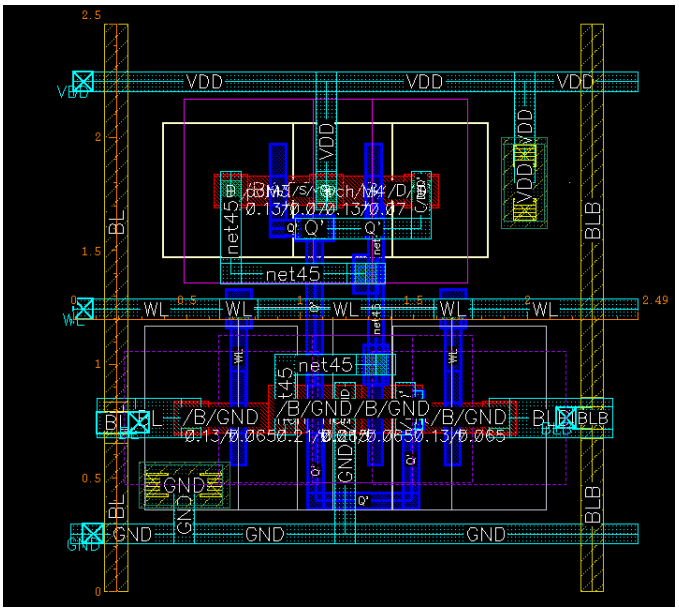

Figure 2 Layout for one cell

The whole layout of 32×12 bits 6T SRAM is shown in the figure below:

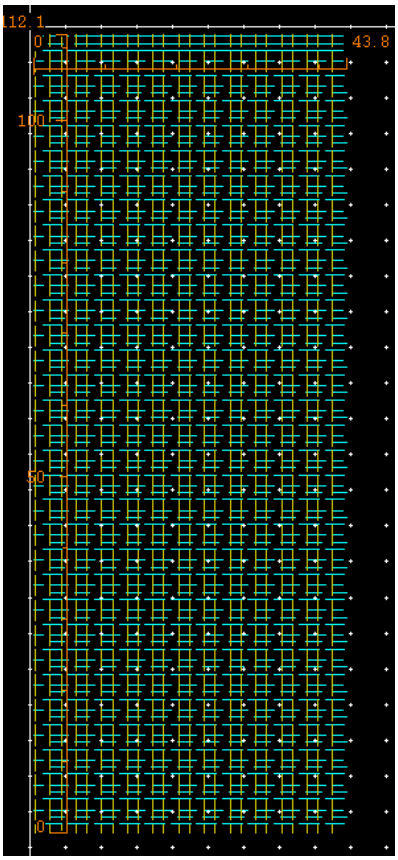

Figure 3 32×12 bits 6T SRAM Layout

From the previous layout the whole area is 4909.98 µm2

V. Results:

Static Noise Margin:

The minimum required Static Noise Margin (SNM) is 0.1Vdd or 0.1V. By examining the butterfly curve (VTC) depicted below, it's apparent that the margin surpasses this prescribed threshold. The margin can be assessed by computing the length of the largest square that can fit within the regions of the butterfly curve.

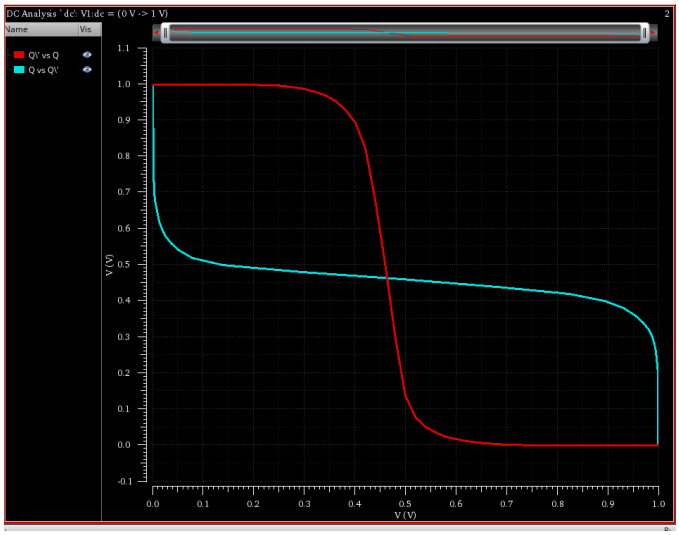

Figure 4 Butterfly Curve

Power curve:

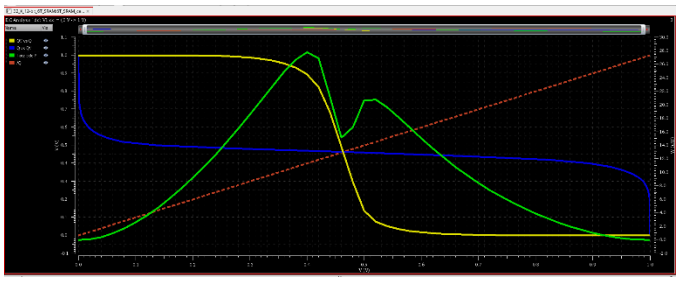

Figure 5 Butterfly Curve power consumption

Write Operation:

The write operation can be summarized as follows:

When writing a '1', the write driver ensures that the designated cell, identified by the Row and Column Decoder, receives the correct data, notwithstanding any imperfections in the peripherals.

Similarly, in the case of writing a '0', the write operation is executed accurately, compensating for any non-ideal characteristics present in the peripherals.

Figure 6 Waveform to Test the functionality of 6t cell

Write parameters:

Write 1 delay	39.4p s
Write 0 delay	36p s
Write 1 power	72.6u W
Write 0 power	78u W

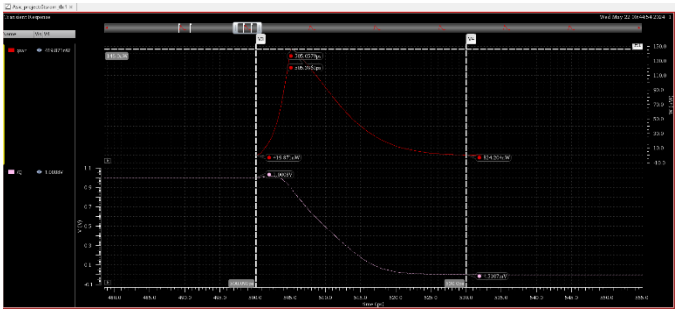

Figure 7 Write 0 Delay and power consumption.

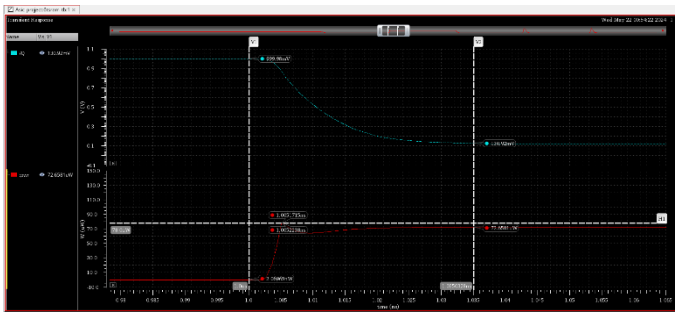

Figure 8 Write 0 Delay and power consumption.

Read Operation:

The reading operation involves the Row decoder, column decoder, and the latch-type sense amplifier. When the Write driver is active, it writes data onto the bit lines. The latch-type sense amplifier offers significant advantages over traditional Operational Transconductance Amplifiers (OTAs) by minimizing delay. Moreover, it exhibits reduced susceptibility to noise on the bit lines and consumes less power due to a self-timed mechanism that activates the sense amplifier only when necessary. Consequently, the power consumption of the latch-type sense amplifier is notably lower compared to that of a current mirror type. By initializing the simulation with the value of '1' on Q, the delay can be computed effectively.

Read parameters:

Read 1 delay	30.4p s
Read 0 delay	45p s
Read 1 power	146u W
Read 0 power	146u W

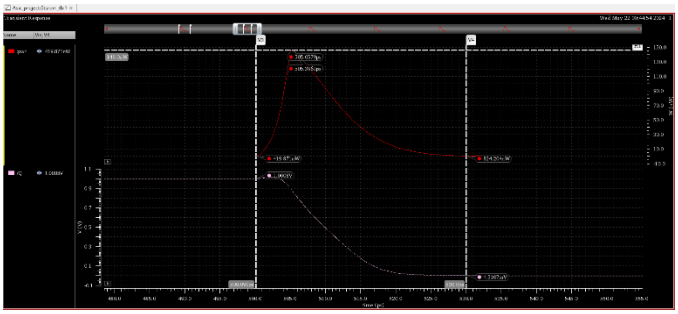

Figure 9 Read 0 Delay and power consumption.

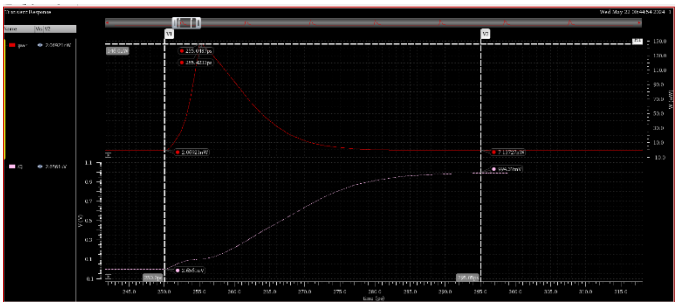

Figure 10 Read 1 Delay and power consumption.

Conclusion and discussion:

In conclusion, implementing a 768-bit 6T SRAM Design went well and was successfully tested with the aid of the peripherals. the specs of the design could be considered to be good enough and ready for synthesizing.

Average POWER	110u W *32*12
AREA	4909.98u m^2
Average DELAY	150.8 ps *32*12

The figure of merit can be calculated as follows: $FM = POWER \times AREA \times DELAY \wedge 2$ so calculating the final number after averaging it should be: 0.3178 (W)(ns)^2(μm2)

Caliber checks:

1- LVS: Correct connections are achieved.
2- DRC: Clean DRC was achieved.

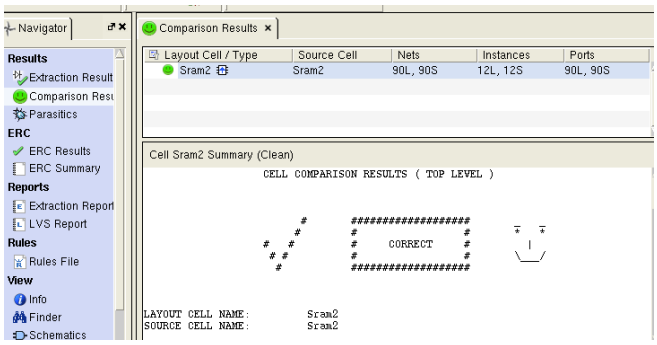

Figure 11 LVS

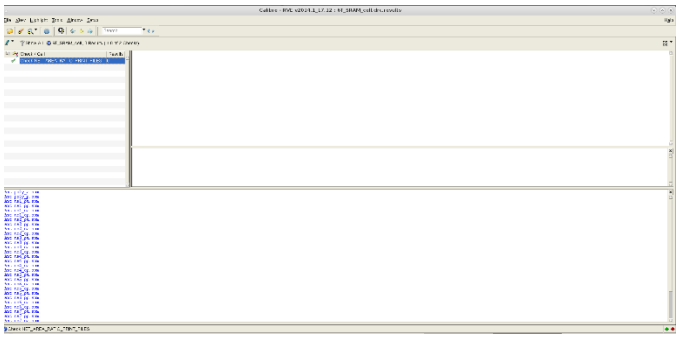

Figure 12 DRC

References

[1] J. M. Rabaey, *Digital Integrated Circuits*. 2nd ed. Upper Saddle River, NJ: Prentice Hall,2002.

[2] SUBBARAYAPPA, M , *The implementation of a hierarchical predecoder/decoder structure in OpenRAM, an open-source memory compiler,* 2011