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Analog Project: Two-Stage CMOS operational amplifier

Introduction:

In this project, we design a two-stage CMOS operational amplifier. This type of amplifier features a differential amplifier as its initial stage, followed by a high-gain stage. The high-gain stage is powered by the output from the differential amplifier, effectively making it a critical component of the two-stage operational amplifier configuration.

For this design, specific objectives need to be met using 65 nm technology, as detailed in the following table:

V_{DD}	1.2 V
GND	0 V
Bias current of M_{12}	80 µA
C_L	0.2 pF
Nominal input common-mode (input DC level)	0.6V
Nominal output common-mode (output DC-level)	0.6 ± 0.1 V
Overall power consumption (including bias circuit)	≤ 1 mW
Output peak-to-peak Swing	0.7 V
Low-frequency differential to single-ended gain	≥ 60 dB
Unity gain frequency	≥ 900 MHz
Phase Margin	≥ 60°
Slew rate	≥ 5 V/µs
Maximum length of transistors	$5\times L_{min}$

The circuit relevant to this design is depicted in Figure 1.

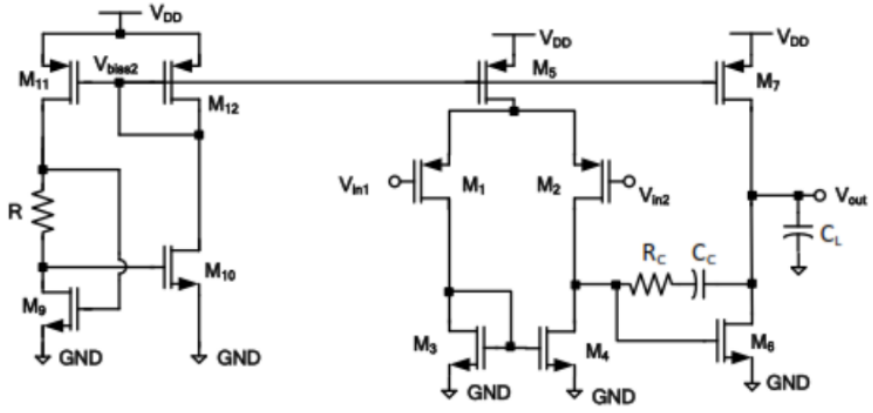

Figure 1 Two-stage op amp circuit

Current source bias circuit:

This circuit is engineered to generate approximately 80 µA of current with a Vdd of 1.2 V. To achieve this, we carefully selected the appropriate widths and lengths for the transistors, resulting in the following specifications:

- Resistance: A polyresistor with a value of 1k ohms is used.
- Transistor Length: All transistors have a length of 5*lmin, which equals 325 nm.
- PMOS Transistors (M0 and M1): Each has a width of 10 µm.
- NMOS Transistor (M8): Has a width of 3 µm.
- NMOS Transistor (M9): Has a width of approximately 6.275 µm.

It's important to note that while the PMOS transistors (M0 and M1) share the same width, there is a variance in the widths of the NMOS transistors (M8 and M9). This difference is crucial for facilitating the flow of current and achieving the target output current of nearly 80 µA, as observed in the drain current (Id) of M1.

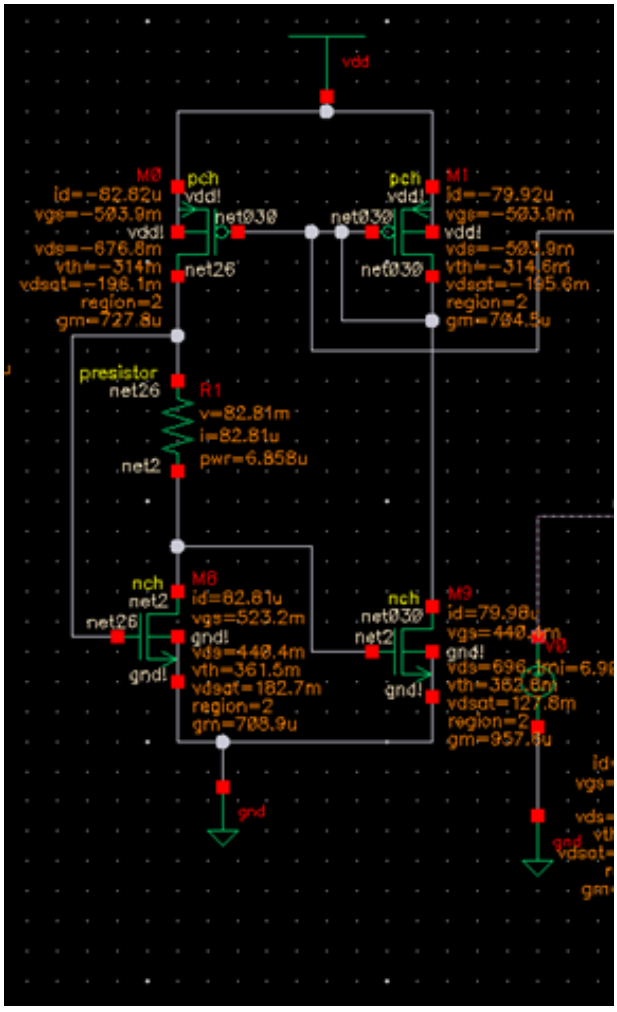

Figure 2 Current source circuit

Additionally, all transistors have been verified to be operating in the saturation region (region 2), as demonstrated in Figure 3.

Schematic in Cadence:

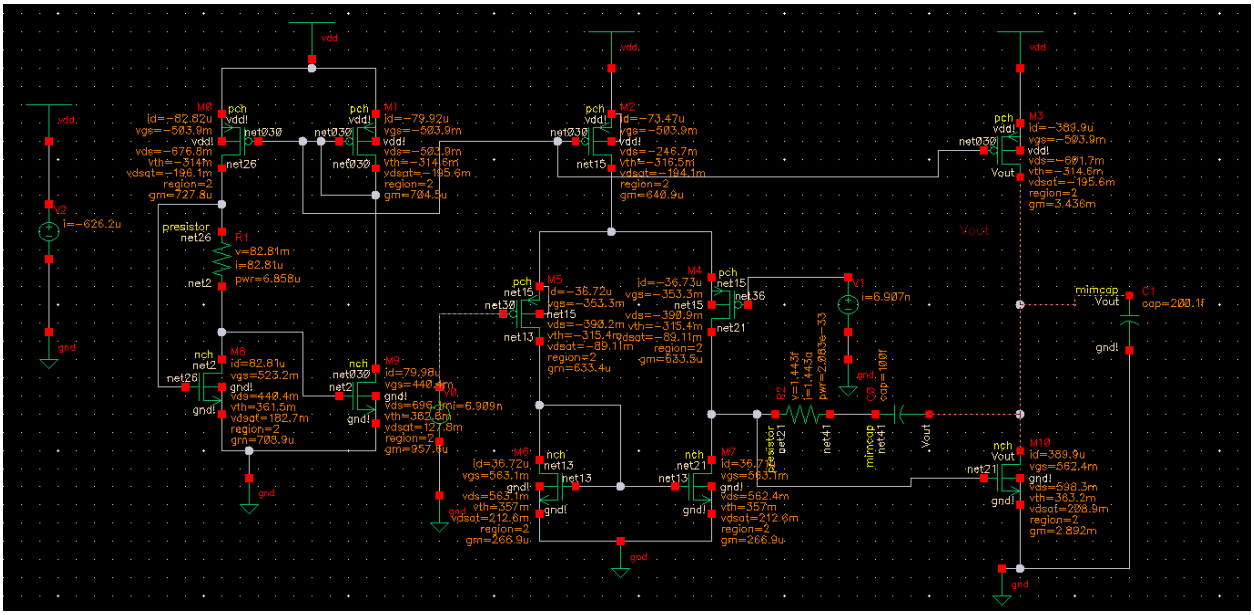

Figure 3 Schematic of whole circuit

Amplifier stages:

In the operational amplifier's design, the first stage is primarily responsible for generating gain, while the second stage is dedicated to achieving the required output swing. To determine the optimal widths and lengths for the transistors, both PMOS and NMOS, we employed the gm/id methodology. This approach involves analyzing the relationships between gm/id, gm/gds, and I/W (current per unit width). By carefully examining these parameters, we were able to precisely tailor the dimensions of the transistors to meet our specific design goals.

M5 and M4 sizing using gm/id methodology with PMOS curves:

The curve depicting the relationship between gm/gds and gm/id is crucial for our analysis, as demonstrated in Figure 6. In our case, the specific curve we focused on is the one colored blue, representing a transistor length of 325 nm. This curve was selected because it aligns with our target specifications for gain. Furthermore, to determine the appropriate width for the transistors, we referred to the I/W (current per unit width) relationship, as illustrated in Figure 5. By combining insights from both these figures, we were able to accurately derive the required dimensions for the transistors to achieve the desired operational characteristics of the amplifier.

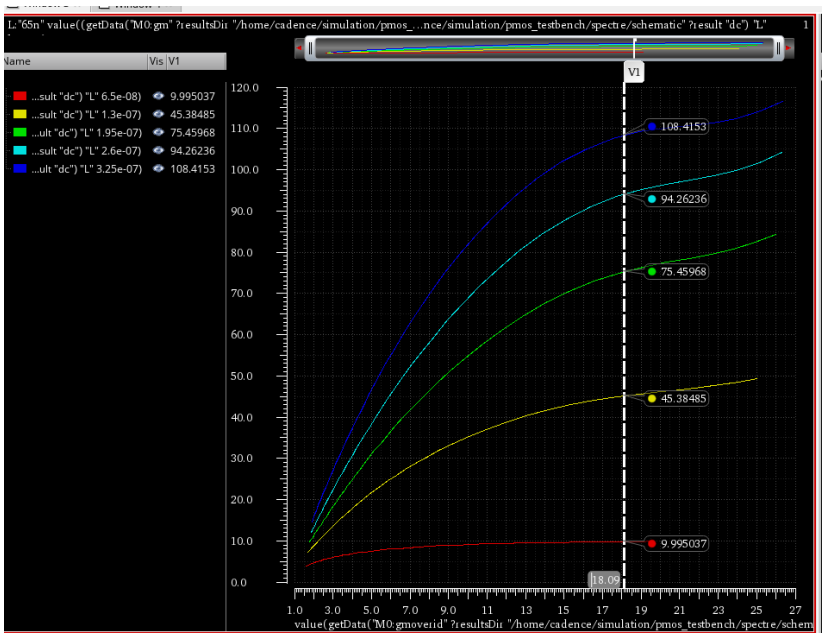

Figure 4 gm/id at 18.09

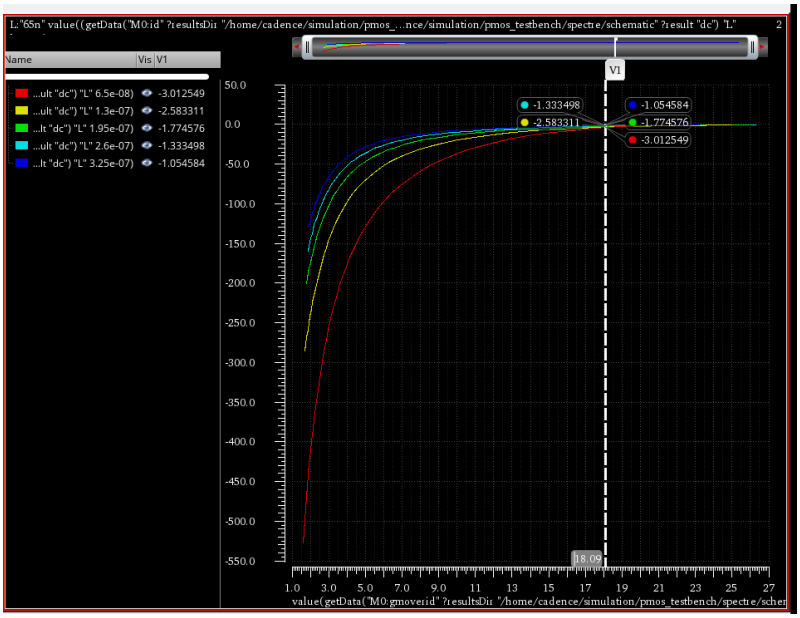

Figure 5 gm/gds vs. Id/w at 18.09

Based on the data from Figure 5, the Id/W (drain current per unit width) value that aligns with my analysis is 1.054584. This value is a key factor in determining the appropriate dimensions for our transistors. Additionally, Figure 6 includes a detailed, handwritten analysis that guides us in calculating the length and width for the PMOS transistors, specifically M5 and M6. According to this analysis, the length for these transistors is set at 325 nm, while their width is determined to be 31.34 µm. This careful calculation ensures that the PMOS transistors (M5 and M6) are correctly sized to meet the operational requirements of our amplifier design.

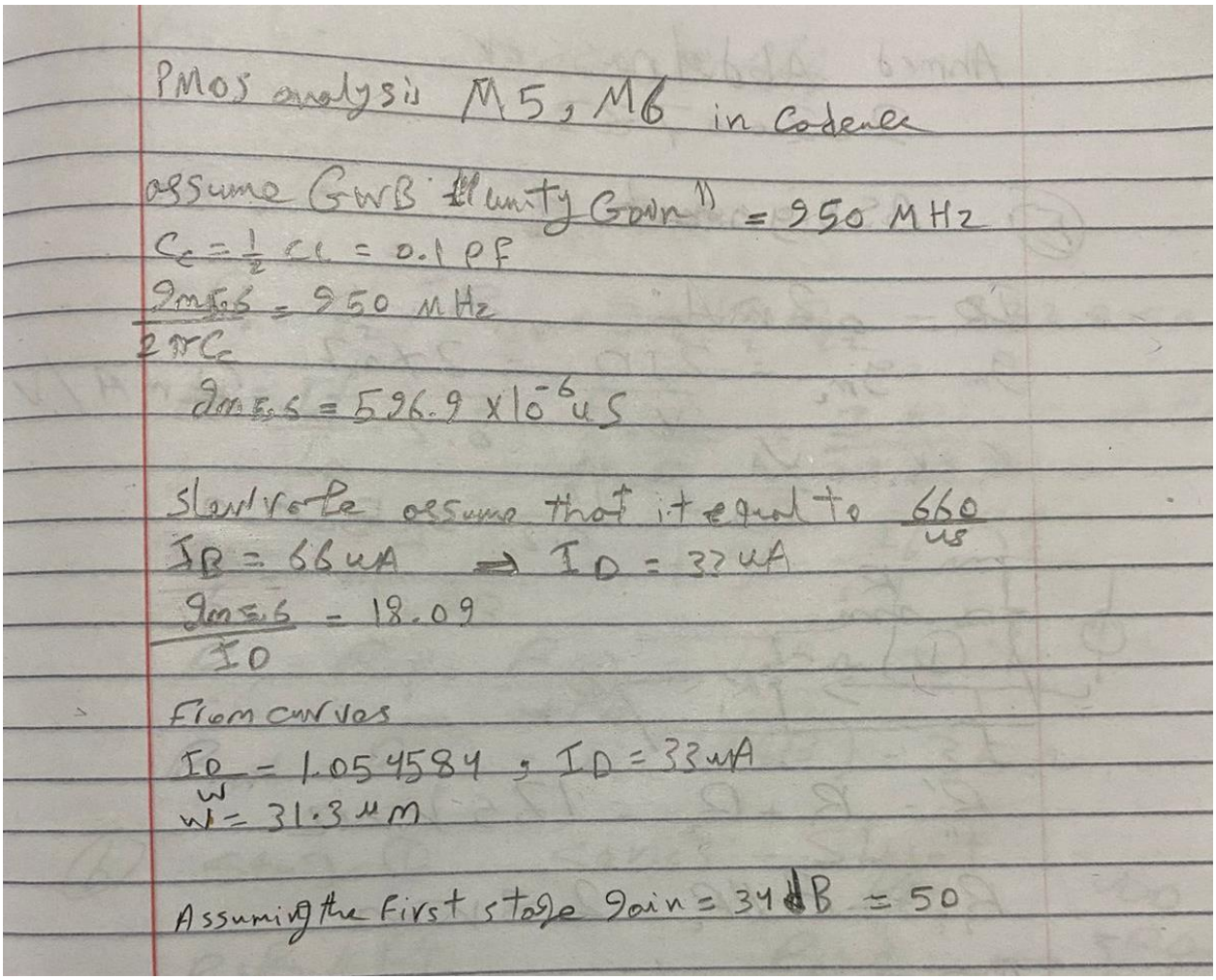

Figure 6

NMOS sizing using gm/id methodology with NMOS curves:

Similarly, to the PMOS transistors, the same analytical approach was applied to the NMOS transistors. The detailed analysis for the NMOS transistors is presented in Figure 7. From this analysis, the length for the NMOS transistors M6and M7 is determined to be 325 nm, and their width is calculated to be 0.960 µm. This meticulous process ensures that the dimensions of the NMOS transistors M6 and M7are precisely tailored to meet the design specifications and performance criteria of our operational amplifier.

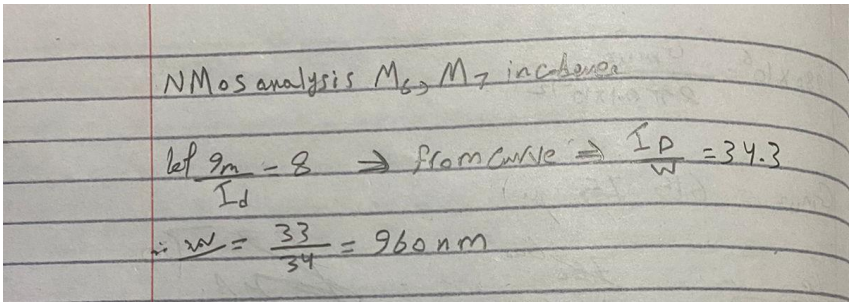

Figure 7

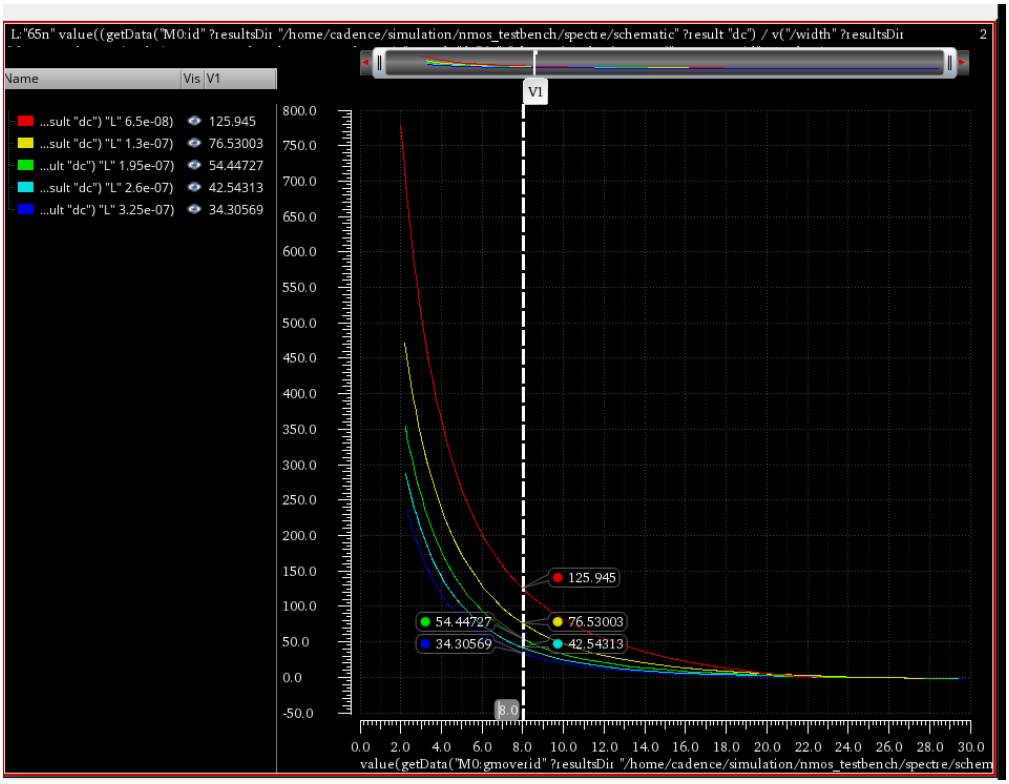

Figure 8

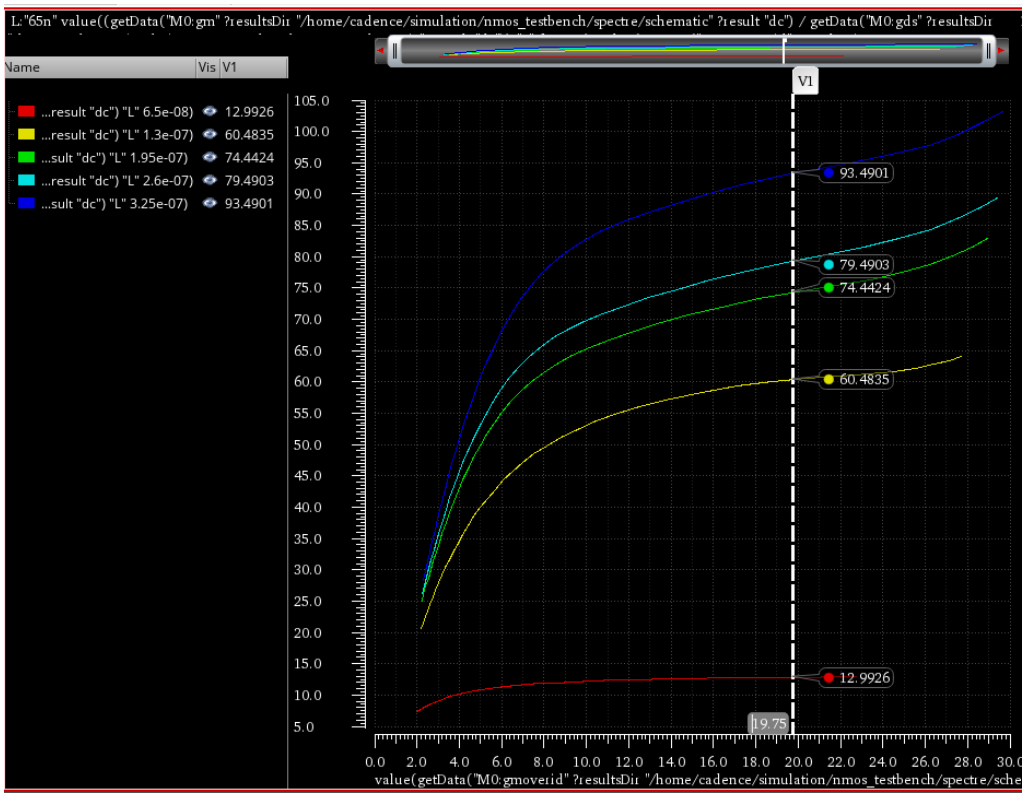

Figure 9

To ensure the desired gain and to maintain all transistors in the saturation region, the dimensions of the remaining transistors in the operational amplifier circuit were carefully manipulated:

- Length: The length for all transistors is uniformly set at 325 nm.
- The width of M0 is matched to that of M1 and M2, which is 10 µm.
- The width of M3 is adjusted to be five times that of M2, resulting in a width of 50 µm. This proportionate increase in width is intended to yield an Id (drain current) in M3 that is approximately five times greater than in M2.
- The width for M10 is determined to be 9.15 µm. This width is chosen to achieve the targeted gain while ensuring the transistor operates in the saturation region.
- C1 is specified as 0.2 pF. In conjunction, C0 is set at half the value of C1, equating to 0.1 pF.
- Resistors: R0, R1 are fixed at a value of 1K ohms.

These adjustments and specifications are crucial for the operational amplifier to meet its performance objectives, particularly in terms of gain and ensuring that all transistors operate within the desired saturation region.

Table with final L and W of all transistors.

Transistor	L	W
M0	325n m	10u m
M1	325n m	10u m
M2	325n m	10um
M3	325n m	47.3u m
M4	325n m	31.3u m
M5	325n m	31.3u m
M6	325n m	960n m
M7	325n m	960n m
M8	325n m	3u m
M9	325n m	6.275u m
M10	325n m	9.15u m

Parameters Test:

Gian and phase Curves:

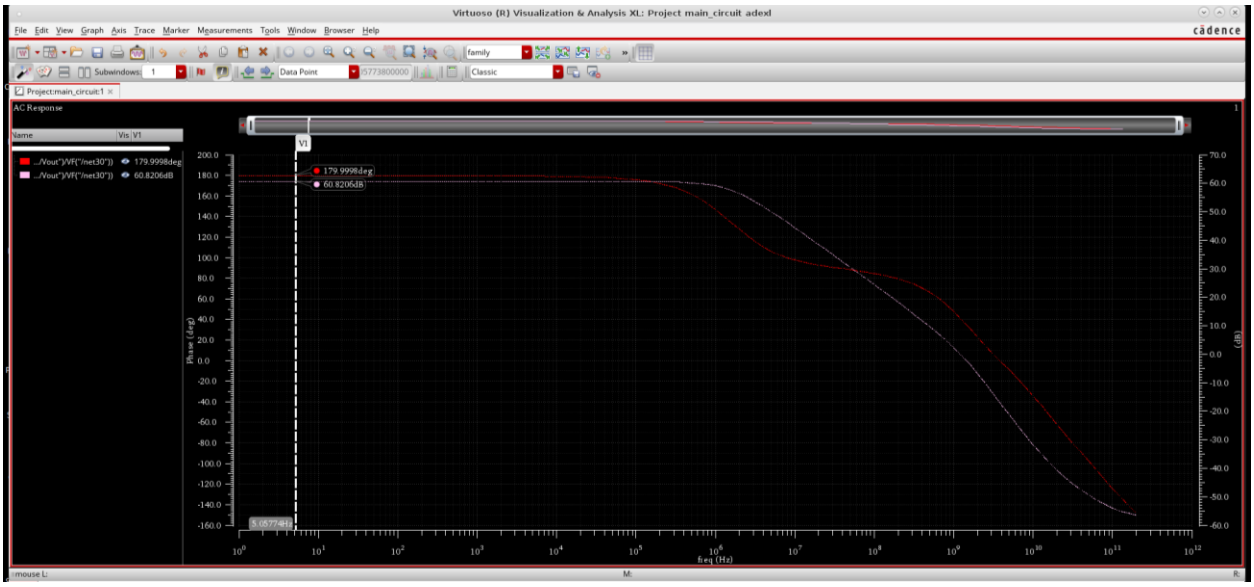

Figure 10 Gain = 60dB in the BW region

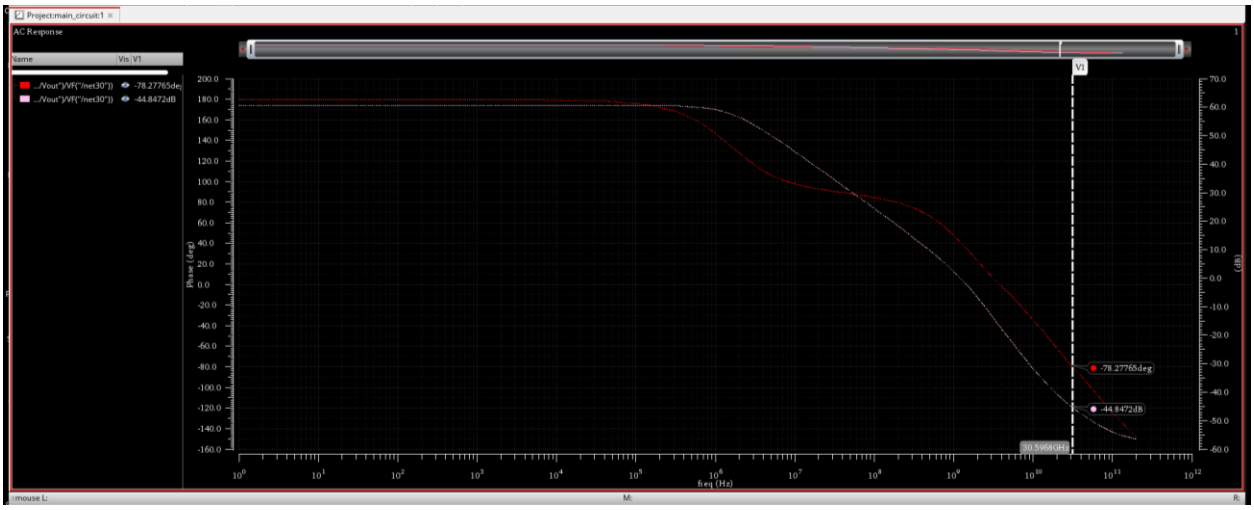

Figure 11 The gain is negative before the phase get to -180

From fig 10,11 we can say that the system is stable and achieve the asked parameters.

Figure 12 presents the outcomes of additional parameters that have been extracted from the designed circuit. These results are crucial for evaluating the overall performance and effectiveness of the circuit in meeting its design specifications the swing is near to 0.7V.

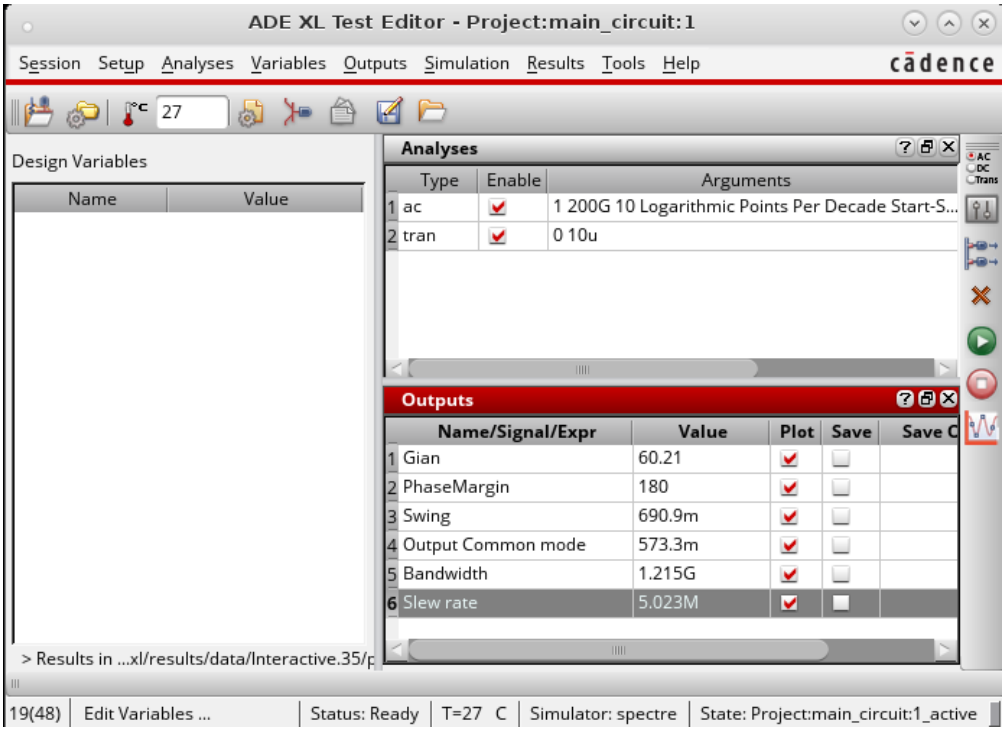

Figure 12

Pre_layout_symbol.

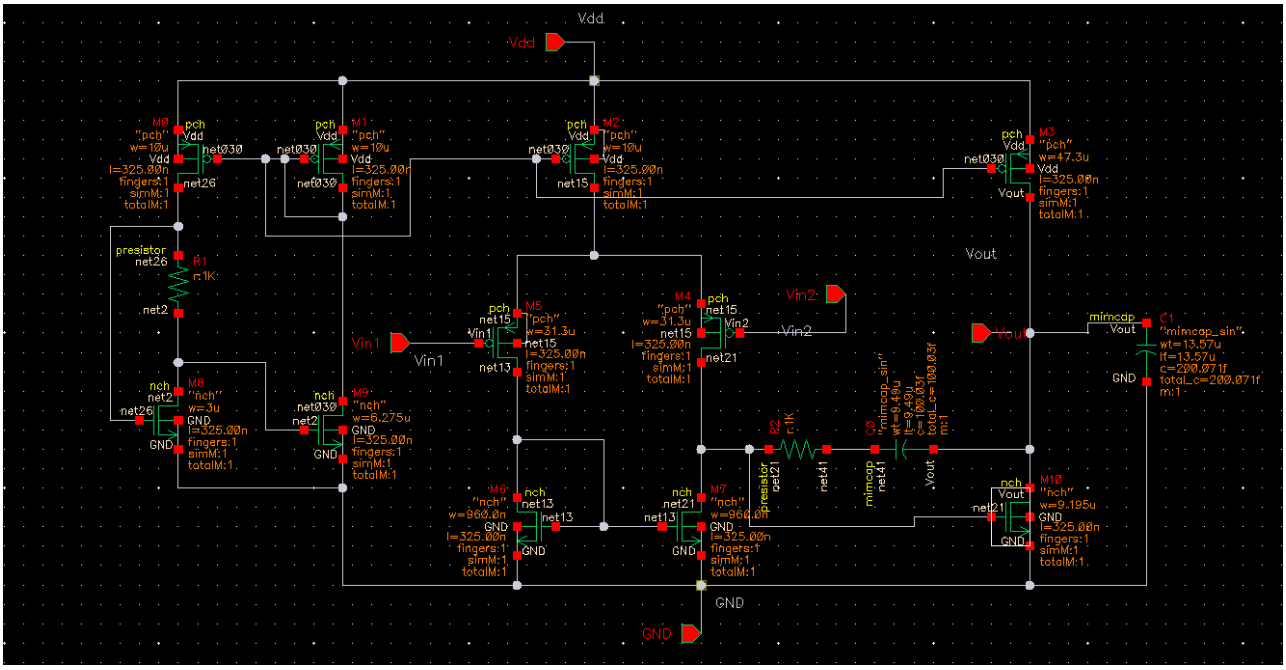

Figure 13

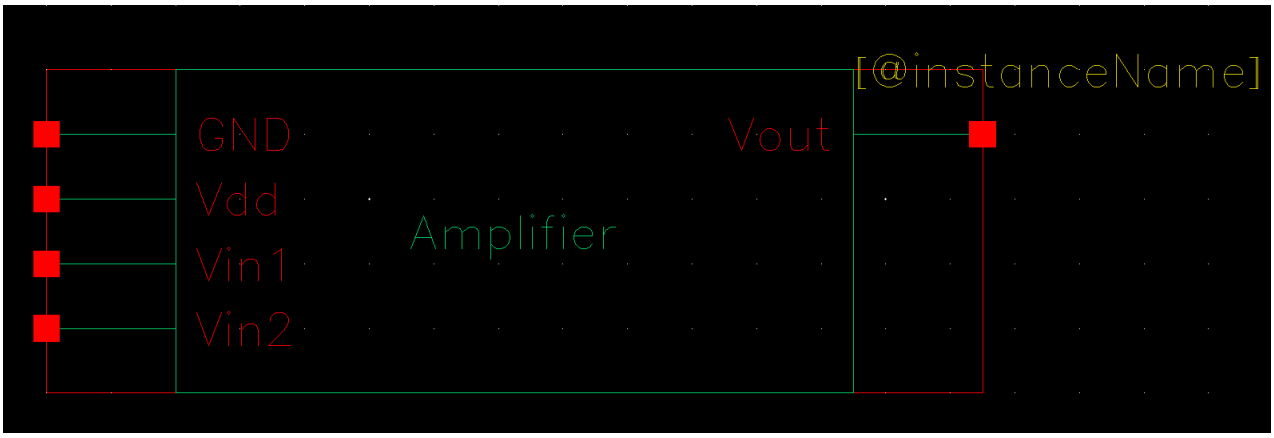

Figure 14

Connecting the generated symbol to test the output.

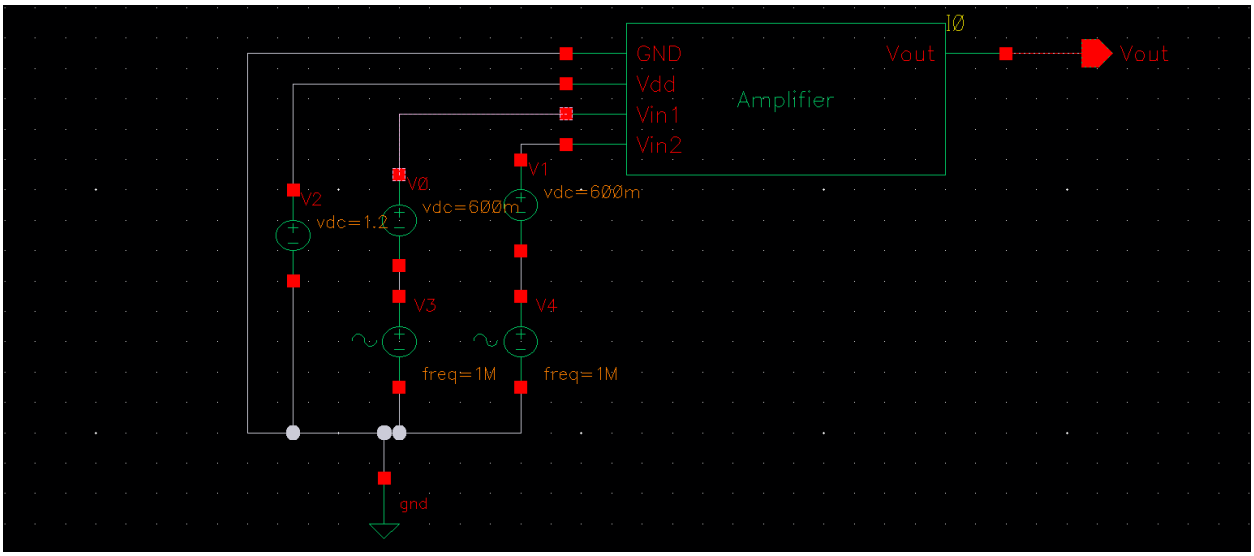

Figure 15

The prelayout simulation results are matched with the initial ones.