```
//  Precision RTL Synthesis 2011a.61 (Production Release) Fri May 20 13:37:48 PDT 201
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//
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//
//  Running on Windows 7 dell@DELL-PC Service Pack 1 6.01.7601 x86
//
//  Start time Thu Oct 02 20:01:50 2014

*****************************************************************
Device Utilization for 3S50ATQ144
*****************************************************************
Resource                          Used    Avail   Utilization
-----------------------------------------------------------------
IOs                               52      108      48.15%
Global Buffers                    1       24        4.17%
LUTs                              338     1408     24.01%
CLB Slices                        169     704      24.01%
Dffs or Latches                   42      1624      2.59%
Block RAMs                        0       3         0.00%
Block Multipliers                 1       3        33.33%
-----------------------------------------------------------------

*************************************************************

Library: work    Cell: lc3_microcontroller    View: INTERFACE

*************************************************************

  Cell         Library  References     Total Area

 BUFGP         xis3a         1 x
 Execute       work          1 x      1      1 Block Multipliers
                                      72     72 Block Multiplier Dffs
                                      30     30 MUX CARRYs
                                      93     93 LUTs
                                      93     93 gates
 FDRE          xis3a        16 x      1     16 Dffs or Latches
 IBUF          xis3a        18 x
 LUT1          xis3a         1 x      1      1 LUTs
 LUT2          xis3a        18 x      1     18 LUTs
 LUT3          xis3a        18 x      1     18 LUTs
 LUT4          xis3a        83 x      1     83 LUTs
 OBUF          xis3a        33 x
 controller    work          1 x     18     18 gates
                                      16     16 LUTs
                                      10     10 Dffs or Latches
 decode        work          1 x     30     30 gates
                                      16     16 Dffs or Latches
                                      94     94 LUTs
 inc_16_0      OPERATORS     1 x     15     15 MUX CARRYs
                                      15     15 LUTs

 Number of ports :                    52
 Number of nets :                    323
 Number of instances :               192
 Number of references to this view :   0

Total accumulated area :
 Number of Block Multiplier Dffs :    72
 Number of Block Multipliers :         1
 Number of Dffs or Latches :          42
 Number of LUTs :                    338
```

```
 Number of MUX CARRYs :                 45
 Number of gates :                     261
 Number of accumulated instances :     506


****************************
 IO Register Mapping Report
****************************
Design: work.lc3_microcontroller.INTERFACE
```

Port	Direction	INFF	OUTFF	TRIFF
rd	Output			
addr(15)	Output			
addr(14)	Output			
addr(13)	Output			
addr(12)	Output			
addr(11)	Output			
addr(10)	Output			
addr(9)	Output			
addr(8)	Output			
addr(7)	Output			
addr(6)	Output			
addr(5)	Output			
addr(4)	Output			
addr(3)	Output			
addr(2)	Output			
addr(1)	Output			
addr(0)	Output			
din(15)	Output			
din(14)	Output			
din(13)	Output			
din(12)	Output			
din(11)	Output			
din(10)	Output			
din(9)	Output			
din(8)	Output			
din(7)	Output			
din(6)	Output			

din(5)	Output			
din(4)	Output			
din(3)	Output			
din(2)	Output			
din(1)	Output			
din(0)	Output			
clock	Input			
reset	Input			
dout(15)	Input			
dout(14)	Input			
dout(13)	Input			
dout(12)	Input			
dout(11)	Input			
dout(10)	Input			
dout(9)	Input			
dout(8)	Input			
dout(7)	Input			
dout(6)	Input			
dout(5)	Input			
dout(4)	Input			
dout(3)	Input			
dout(2)	Input			
dout(1)	Input			
dout(0)	Input			
complete	Input			

Total registers mapped: 0