```
//  Precision RTL Synthesis 2011a.61 (Production Release) Fri May 20 13:37:48 PDT 201
1
//
//  Copyright (c) Mentor Graphics Corporation, 1996-2011, All Rights Reserved.
//              Portions copyright 1991-2008 Compuware Corporation
//                        UNPUBLISHED, LICENSED SOFTWARE.
//             CONFIDENTIAL AND PROPRIETARY INFORMATION WHICH IS THE
//           PROPERTY OF MENTOR GRAPHICS CORPORATION OR ITS LICENSORS
//
//  Running on Windows 7 dell@DELL-PC Service Pack 1 6.01.7601 x86
//
//  Start time Thu Oct 02 20:01:50 2014

-- Device: Xilinx - SPARTAN3A : 3S50ATQ144 : 5
-- CTE report summary..
-- POST-SYNTHESIS TIMING REPORTS ARE ESTIMATES AND SHOULD NOT BE RELIED ON TO MAKE Qo
R DECISIONS. For accurate timing information, please run place-and-route (P&R) and re
view P&R generated timing reports.

================================================================================
===========
                    Clock Frequency Report

        Domain                  Clock Name                              Min Period (Fre
q)              Required Period (Freq)
        ------                  ----------                              ---------------
--              ----------------------
        ClockDomain0            clock                                   13.961 (71.628
MHz)            14.286 (70.000 MHz)


================================================================================
===========
Setup Timing Analysis of clock

Setup Slack Path Summary

               Data
                Data
       Setup    Path   Source  Dest.
                End
Index  Slack   Delay    Clock   Clock       Data Start Pin                    Data End P
in              Edge
-----  -----  ------  ------  -----  ------------------------  ----------------------
--------------  ----
  1    0.325  14.262  clock   clock  decode_unit/reg_IR(12)/C  decode_unit/reg_file/i
x16878z41717/D  Rise
  2    0.546  14.041  clock   clock  decode_unit/reg_IR(13)/C  decode_unit/reg_file/i
x16878z41717/D  Rise
  3    0.618  13.969  clock   clock  decode_unit/reg_IR(14)/C  decode_unit/reg_file/i
x16878z41717/D  Rise
  4    0.619  13.968  clock   clock  decode_unit/reg_IR(15)/C  decode_unit/reg_file/i
x16878z41717/D  Rise
  5    2.254  12.333  clock   clock  decode_unit/reg_IR(11)/C  decode_unit/reg_file/i
x16878z41717/D  Rise
  6    2.264  12.323  clock   clock  decode_unit/reg_IR(0)/C   decode_unit/reg_file/i
x16878z41717/D  Rise
  7    2.264  12.323  clock   clock  decode_unit/reg_IR(1)/C   decode_unit/reg_file/i
x16878z41717/D  Rise
  8    2.264  12.323  clock   clock  decode_unit/reg_IR(2)/C   decode_unit/reg_file/i
x16878z41717/D  Rise
  9    2.265  12.322  clock   clock  decode_unit/reg_IR(9)/C   decode_unit/reg_file/i
x16878z41717/D  Rise
 10    2.265  12.322  clock   clock  decode_unit/reg_IR(10)/C  decode_unit/reg_file/i
x16878z41717/D  Rise

                  CTE Path Report
```

```
Critical path #1, (path slack = 0.325):

SOURCE CLOCK: name: clock period: 14.285710
     Times are relative to the 1st rising edge
  DEST CLOCK: name: clock period: 14.285710
     Times are relative to the 2nd rising edge

NAME                                                                GATE
DELAY    ARRIVAL DIR  FANOUT
decode_unit/reg_IR(12)/C                                            FDE
         0.000   up
decode_unit/reg_IR(12)/Q                                            FDE             0
.495     0.495   up
decode_unit/D_Data(44)                                              (net)           1
.354                 15
decode_unit/ix759z38182/I3                                          LUT4
         1.849   up
decode_unit/ix759z38182/O                                           LUT4            0
.561     2.410   up
decode_unit/nx759z5                                                 (net)           0
.273                  6
decode_unit/ix759z1524/I2                                           LUT3
         2.683   up
decode_unit/ix759z1524/O                                            LUT3            0
.561     3.244   up
decode_unit/nx759z8                                                 (net)           1
.440                 16
decode_unit/reg_file/ix25297z41717/DPRA2                            RAM16X1D
         4.684   up
decode_unit/reg_file/ix25297z41717/DPO                              RAM16X1D        0
.601     5.285   up
decode_unit/reg_file/rd_data3(0)                                    (net)           0
.253                  2
exc_unit/ix64854z1545/I2                                            LUT3
         5.538   up
exc_unit/ix64854z1545/O                                             LUT3            0
.561     6.099   up
exc_unit/aluin2(0)                                                  (net)           0
.243                  3
exc_unit/A1/aluout_multu16_0i1/ix2247z43854/B(0)                    MULT18X18SIO
         6.342   up
exc_unit/A1/aluout_multu16_0i1/ix2247z43854/P(0)                    MULT18X18SIO    4
.332    10.674   up
exc_unit/A1/aluout_multu16_0i1/nx37973z1                            (net)           0
.272                  1
exc_unit/A1/ix64769z59751/I1                                        LUT4
        10.946   up
exc_unit/A1/ix64769z59751/O                                         LUT4            0
.562    11.508   up
exc_unit/A1/nx64769z1                                               (net)           0
.272                  1
exc_unit/A1/ix64769z1530/I1                                         LUT3
        11.780   up
exc_unit/A1/ix64769z1530/O                                          LUT3            0
.562    12.342   up
exc_unit/A1/aluout(0)                                               (net)           0
.272                  1
ix30593z42332/I1                                                    LUT4
        12.614   up
ix30593z42332/O                                                     LUT4            0
.562    13.176   up
nx30593z31                                                          (net)           0
.272                  1
ix30593z1373/I0                                                     LUT2
        13.448   up
```

```
ix30593z1373/O                                                  LUT2              0
.561    14.009   up
DR_in(0)                                                        (net)             0
.253                  2
decode_unit/reg_file/ix16878z41717/D                            RAM16X1D
        14.262   up

                Initial edge separation:     14.286
                Source clock delay:      -    2.785
                Dest clock delay:        +    2.785
                                          -----------
                Edge separation:             14.286
                Setup constraint:         -  -0.301
                                          -----------
                Data required time:          14.587
                Data arrival time:        -  14.262   ( 65.61% cell delay, 34.39% net
 delay )
                                          -----------
                Slack:                        0.325


================================================================================
===========
                    Input Delay Report

        Input                   Clock Name                          Slack (ns)
        -----                   ----------                          ----------
        No input delay constraints.


================================================================================
===========
                    Output Delay Report

        Output                  Clock Name                          Slack (ns)
        ------                  ----------                          ----------
        No output delay constraints.
```