Part 1

The design explanation:

My design is a digital calendar which display (day , month , year) in base-19 on 7-segment

Using CD4024 - 7-Bit Binary Counter and

With digital clock generator of period " 24hours "

And Settable digits for each element

Special case in February ends at 28

Correction circuit :

Which are the blocks {DAY DIGIT1, DAY DIGIT2, MONTH , YEAR DIGIT1 , YEAR DIGIT2 , YEAR DIGIT3}

They're all -binary-to-base 19 ' seven segment decoders

- First digit of day "check the value 19 (Bin 10010) and reset and increase second digit of day
- Check 30 day which means (1B) in base-19 and then reset both digits and increase month first digit by 1
- Special case on February (check month value 2) & check value of day with value 28 (19 in base-19) then reset both the days digits
- Same thing at year digits it resets every 19 "I" (10010)

The design main functions :

First function is the clock "pulse generator " and every day "24 hours " gives a signa

Second is to read and count these pulses then decode it to binary

after that step there are two steps in parallel :

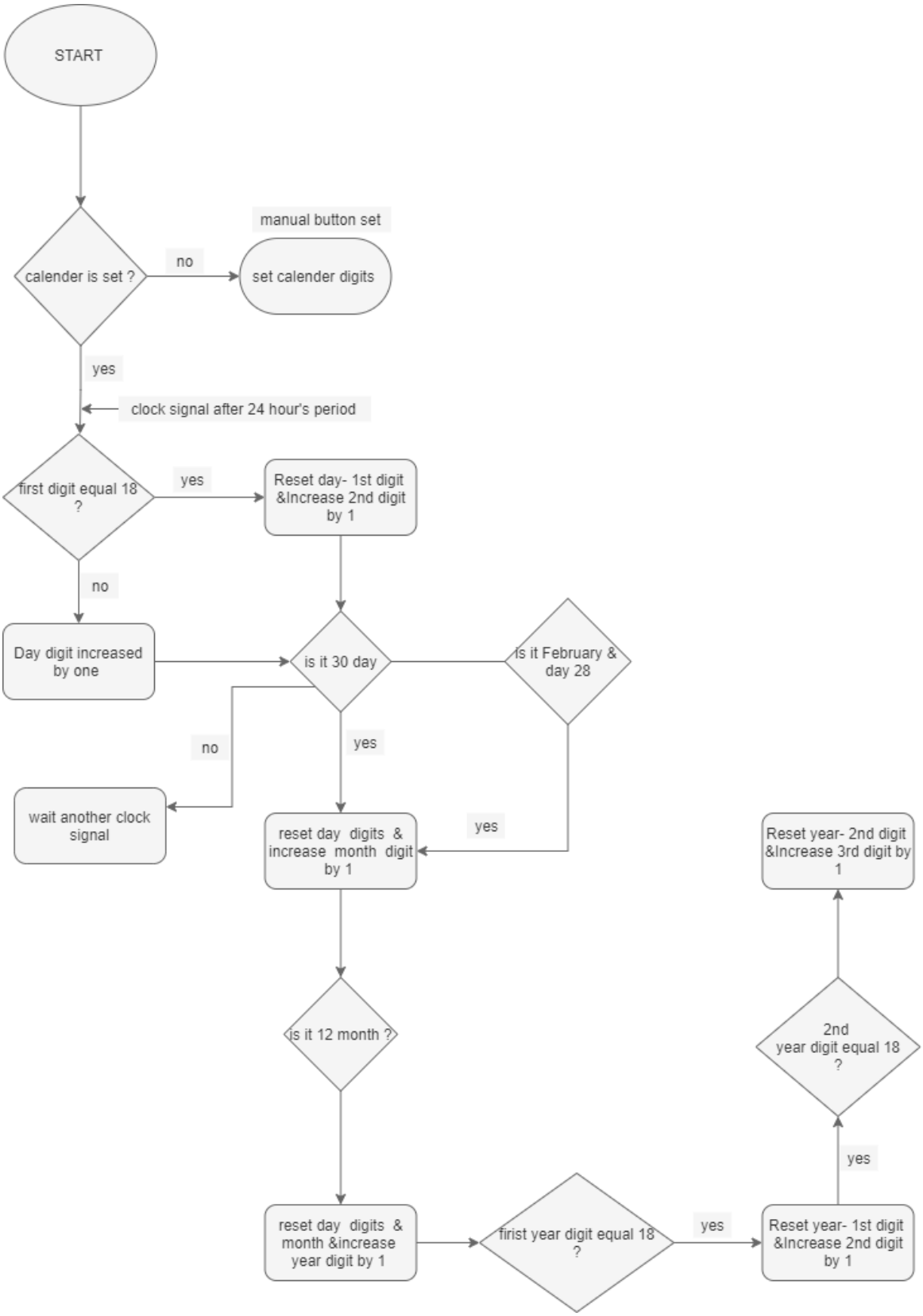
1. encoding the binary input to output coded 7 segment code
2. checking the value of the binary code to reset the first digit and give signal to increase the 2nd digit by 1

then check the both digits of value of 30 days which is (1b) in base-19 system which is displayed on the 7-segments

the increase the month digits by 1 .

same process goes to the month digit until it's 12 months which is (C) in base-19 system displayed on 7-segment and then increase year digits by 1 etc.…

Use case of the design :



List of components used in design :

Active components :

Dc generator 5v	To supply my manual set of digits for each day , month and year
Digital clock generator with period 86,400 second	To represent my clock of da 24 hours
Logic gates (OR"7432" , AND" 74ls08",NOT" 7404")	For the logical design and Equations representation
CD4024 - 7-Bit Binary Counter	To count my clock signals and the o/p is easier to be handled
7-segment	To display the output

passive components :

1n4007 diode	To prevent the flow of current in the reverse direction
Resistors (330 , 10k) ohm	Circuit requirement
Ground	
Buttons	To manual set and connect a pulse as a manual clock

General idea

Each block of blocks {DAY DIGIT1, DAY DIGIT2, MONTH , YEAR DIGIT1 , YEAR DIGIT2 , YEAR DIGIT3}

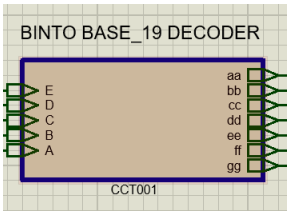
Are same design which means same input and same output :
inputs are the numbers in 5 bits in binary : <<< **I1 I2 I3 I4 I5** >>>

Outputs are the encoded 7-segment code portable for **base-19** : **<<< A B C D E F G >>>**

*note : in design for design issues I had to change names

Inputs to A -B-C-D-E

Outputs to aa-bb-cc-dd-ee-ff-gg



Binary Input i_1>i_5		Decimal	A o/p_1	B o/p_2	C o/p_3	D o/p_4	E o/p_5	F o/p_6	G o/p_7
00000	0	0	1	1	1	1	1	1	0
00001	1	1	0	1	1	0	0	0	0
00010	2	2	1	1	0	1	1	0	1
00011	3	3	1	1	1	1	0	0	1
00100	4	4	0	1	1	0	0	1	1
00101	5	5	1	0	1	1	0	1	1
00110	6	6	1	0	1	1	1	1	1
00111	7	7	1	1	1	0	0	0	0
01000	8	8	1	1	1	1	1	1	1
01001	9	9	1	1	1	1	0	1	1
01010	a	10	1	1	1	1	1	0	1
01011	b	11	0	0	1	1	1	1	1
01100	c	12	1	0	0	1	1	1	0
01101	d	13	0	1	1	1	1	0	1
01110	e	14	1	1	0	1	1	1	1
01111	f	15	1	0	0	0	1	1	1
10000	g	16	1	1	1	1	0	1	1
10001	h	17	0	0	1	0	1	1	1
10010	I	18	0	0	0	0	1	1	0

“A” K map of design:

A	$i_2'.\ i_1'$	$i_2'\ .\ i_1$	$i_2.i_1$	$i_2\ .i_1'$
$i_5'.\ i_4\ .\ i_3$	1	1	1	*1*
$i_5'.i_4'\ .i_3$	1	0	1	*0*
$i_5'.i_4\ .i_3$	0	1	0	*1*
$i_5'.i_4\ .\ i_3'$	1	1	0	*1*
$i_5.i_4'\ .i_3'$	1	0	x	*0*
$i_5.i_4'\ .i_3$	x	x	x	*x*
$i_5.i_4\ .i_3$	x	x	x	*x*
$i_5.i_4\ .i_3'$	x	x	x	*x*

The equation of A:

A= $i_1'\ i_2'\ i_3'$ + $i_1'\ i_3'\ i_4'$ + $i_2'\ i_4'\ i_5'$ + $i_2'\ i_4\ i_5$ + $i_2\ i_4'\ i_5$ + $i_2\ i_4\ i_5'$

K map of design:

B	$i_2'.\ i_1'$	$i_2'\ .\ i_1$	$i_2.i_1$	$i_2\ .i_1'$
$i_5'.\ i_4\ .\ i_3$	1	1	1	*1*
I5'.i4' .i3	1	0	1	*0*
I5'.i4 .i3	0	1	0	*1*
I5'.i4 . i3'	1	1	0	*1*
I5.i4' .i3'	1	0	x	*0*
I5.i4' .i3	x	x	x	*x*
I5.i4 .i3	x	x	x	*x*
I5.i4 .i3'	x	x	x	*x*

The equation of B:

B= $i_5'.i_4.'i_3'$ + $i_5'.i_3'.i_2'$ + $i_2'.i_2'.i_1'$ + $i_4'.i_2.i_1$ + $i_4.i_2'.i_1$ + $i_4.i_2.i_1'$

“C” K map of design:

C	$I_4'.\ I_5'$	$I_4'\ .\ i_5$	$I_4.i_5$	$I_4\ .i_5'$
$I_1'.\ I_2'\ .\ i_3'$	1	1	1	*0*
$I_1'.i_2'\ .i_3$	1	1	1	*1*
$I_1'.i_2\ .i_3$	0	1	0	*0*
$I_1'.i_2\ .\ i_3'$	1	1	1	*1*
$I_1.i_2'\ .i_3'$	1	1	x	*0*
$I_1.i_2'\ .i_3$	x	x	x	*x*
$I_1.i_2\ .i_3$	x	x	x	*x*
$I_1.i_2\ .i_3'$	x	x	x	*x*

The equation of C:

C= $I_2'\ I_4' + I_2'\ I_5 + I_4'\ I_5 + I_2'\ I_3 + I_2\ I_3'$

“D” K map of design:

D	$I_4'.\ I_5'$	$I_4'\ .\ i_5$	$I_4.i_5$	$I_4\ .i_5'$
$I_1'.\ I_2'\ .\ i_3'$	1	0	1	*1*
$I_1'.i_2'\ .i_3$	0	1	0	*1*
$I_1'.i_2\ .i_3$	1	1	0	*1*
$I_1'.i_2\ .\ i_3'$	1	1	1	*1*
$I_1.i_2'\ .i_3'$	1	0	x	*0*
$I_1.i_2'\ .i_3$	x	x	x	*x*
$I_1.i_2.i_3$	x	x	x	*x*
$I_1.i_2\ .i_3'$	x	x	x	*x*

The equation of D:

D= $I_2\ I_4' + I_1'\ I_3'\ I_4` + I_1'\ I_4\ I_5' + I_3'\ I_4'\ I_5' + I_3\ I_4'\ I_5$

“E” K map of design:

E	$I_4'.\ I_5'$	$I_4'\ .\ i_5$	$I_4.i_5$	$I_4\ .i_5'$
$I_1'.\ I_2'\ .\ i_3'$	1	0	0	*1*
$I_1'.i_2'\ .i_3$	0	0	0	*1*
$I_1'.i_2\ .i_3$	1	1	1	*1*
$I_1'.i_2\ .\ i_3'$	1	0	1	*0*
$I_1.i_2'\ .i_3'$	0	1	x	*0*
$I_1.i_2'\ .i_3$	x	x	x	*x*
$I_1.i_2\ .i_3$	x	x	x	*x*
$I_1.i_2\ .i_3'$	x	x	x	*x*

The equation of E:

$E= I_2\ I_3 + I_1\ I_5 + I_2'\ I_4\ I_5' + I_2\ I_4\ I_5 + I_1'\ I_3'\ I_4'\ I_5'$

“F” K map of design:

F	$I_4'.\ I_5'$	$I_4'\ .\ i_5$	$I_4.i_5$	$I_4\ .i_5'$
$I_1'.\ I_2'\ .\ i_3'$	1	0	0	*0*
$I_1'.i_2'\ .i_3$	1	1	0	*1*
$I_1'.i_2\ .i_3$	1	0	1	*1*
$I_1'.i_2\ .\ i_3'$	1	1	1	*1*
$I_1.i_2'\ .i_3'$	1	1	x	*1*
$I_1.i_2'\ .i_3$	x	x	x	*x*
$I_1.i_2\ .i_3$	x	x	x	*x*
$I_1.i_2\ .i_3'$	x	x	x	*x*

The equation of F:

$F= I_1 + I_4'\ I_5' + I_3\ I_5' + I_2\ I_3' + I_2\ I_4 + I_2'\ I_3\ I_4'$

“G” K map of design:

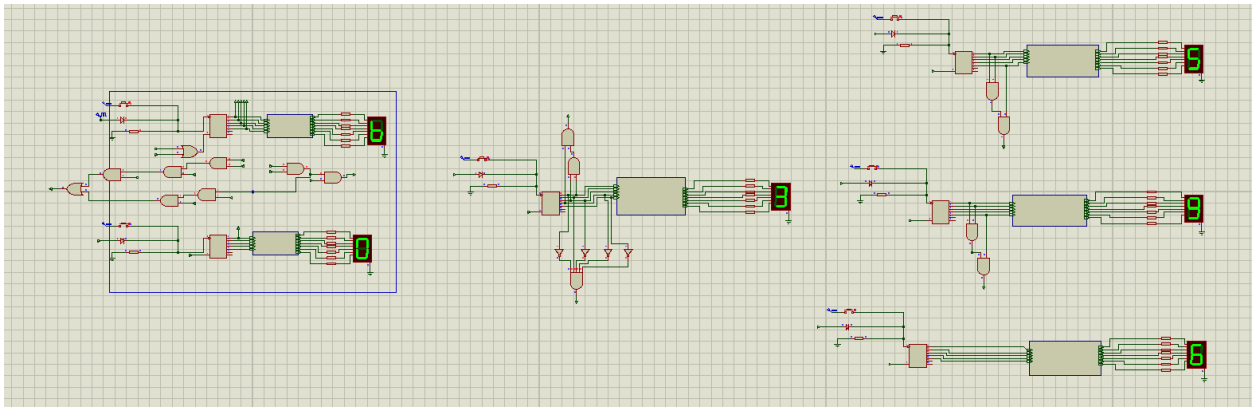
G	$I_4'.\ I_5'$	$I_4'\ .\ i_5$	$I_4.i_5$	$I_4\ .i_5'$
$I_1'.\ I_2'\ .\ i_3'$	0	0	1	*1*
$I_1'.i_2'\ .i_3$	1	1	0	*1*
$I_1'.i_2\ .i_3$	0	1	1	*1*
$I_1'.i_2\ .\ i_3'$	1	1	1	*1*
$I_1.i_2'\ .i_3'$	1	1	x	*0*
$I_1.i_2'\ .i_3$	x	x	x	*x*
$I_1.i_2.i_3$	x	x	x	*x*
$I_1.i_2\ .i_3'$	x	x	x	*x*

The equation of G:

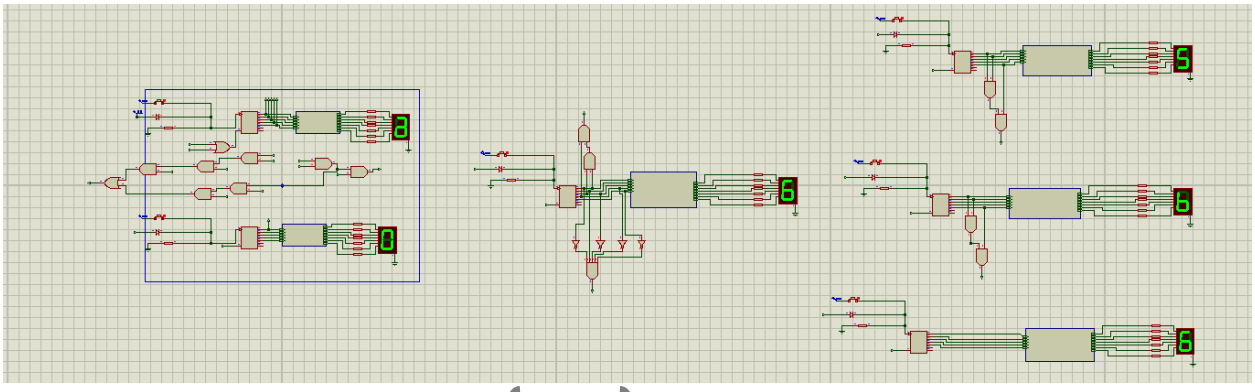
$G = I_2\ I_3' + I_2\ I_5 + I_1\ I_4' + I_1'\ I_3'\ I_4 + I_1'\ I_4\ I_5' + I_2'\ I_3\ I_4'$

EXAMPLES

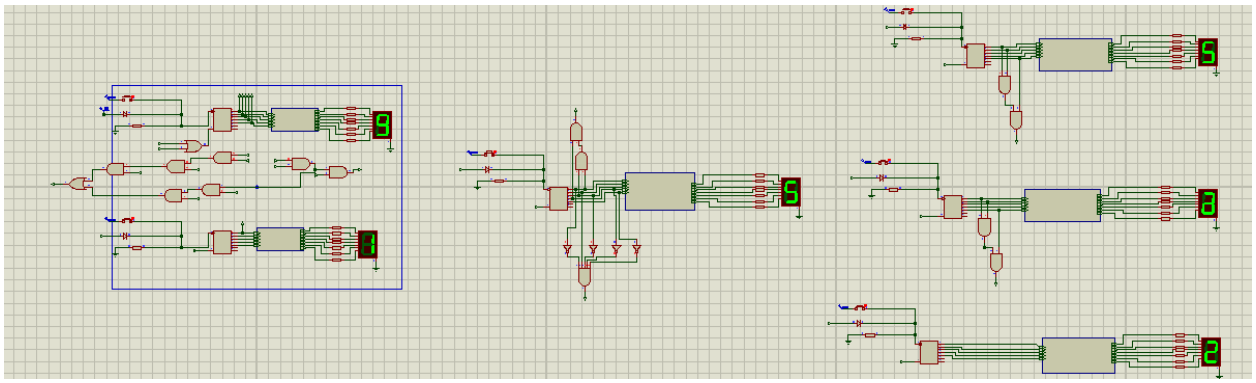
Example (1) : >>12/3/ 1982 --------> b/3/596



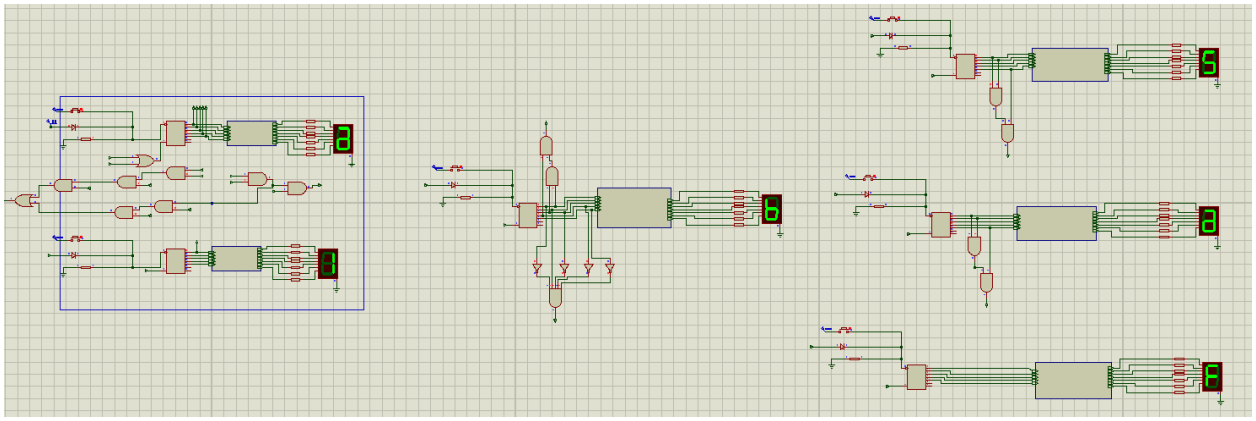
Example (2) : >>10/6/ 2020 --------> a/6/5b6



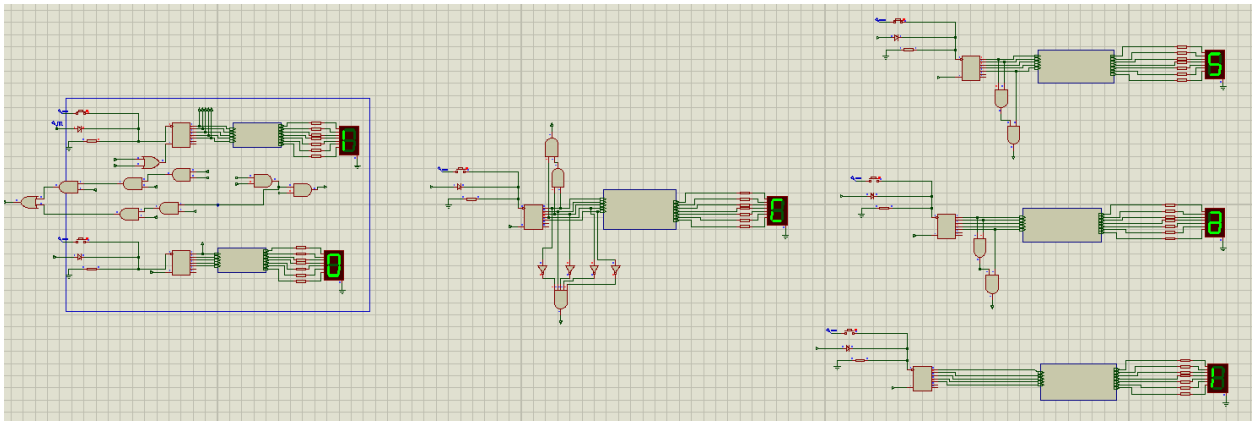
Example (3) : >>28/5/ 1997 --------> 19/5/ 5a2



Example (4) : >>29/11/ 2019 --------> 1a/b/ 5af



Example (5) : >>18/12/ 2013 --------> I0/b/ 5aI



***NOTE:**

I ➔ 18	1 ➔ 1