label	description	stimulus generated	checkers
randomization sequence 1	In this sequence we will randomize the first control module to make sure that the overall functionality of the top design and the connection between the two I2C modules is correct	randomization for all the inputs with constraining the reset to be on 5% of the time and no restert request for 95% of the time	we check the functionality of the outputs using checkers comparing the output with the reference output from golden model
randomization sequence 2	In this sequence we will randomize the second control module to make sure that the overall functionality of the top design and the connection between the two I2C modules is correct	randomization for all the inputs with constraining the reset to be on 5% of the time and no restert request for 95% of the time	we check the functionality of the outputs using checkers comparing the output with the reference output from golden model
start read sequence 1	this is a directed seequence to check the starting of a read transaction and detection of the target in the same transaction	directed	we check the functionality of the outputs using checkers comparing the output with the reference output from golden model we use an assertion to check the detection of the address and operation in the target
start write sequence 1	this is a directed seequence to check the starting of a write transaction and detection of the target in the same transaction	directed	we check the functionality of the outputs using checkers comparing the output with the reference output from golden model we use an assertion to check the detection of the address and operation in the target
NACK feature 1	this is a directed sequence where we check the target bahavior with the error respond and NACK response	directed	we check the functionality of the outputs using checkers comparing the output with the reference output from golden model we use an assertion to check the generation of the NACK.
valid feaure 1	this is a directed sequence where we held the valid to low to check the termination of the transaction based on the valid signal	directed	we check the functionality of the outputs using checkers comparing the output with the reference output from golden model
restart feature 1	this is a directed sequence where we held the restart request to 1 to check the restarting feature of the control module	directed	we check the functionality of the outputs using checkers comparing the output with the reference output from golden model
start read sequence 2	this is a directed seequence to check the starting of a read transaction and detection of the target in the same transaction	directed	we check the functionality of the outputs using checkers comparing the output with the reference output from golden model we use an assertion to check the detection of the address and operation in the target
start write sequence 2	this is a directed seequence to check the starting of a write transaction and detection of the target in the same transaction	directed	we check the functionality of the outputs using checkers comparing the output with the reference output from golden model we use an assertion to check the detection of the address and operation in the target
NACK feature 2	this is a directed sequence where we check the target behavior with the error respond and NACK response	directed	we check the functionality of the outputs using checkers comparing the output with the reference output from golden model we use an assertion to check the generation of the NACK.
valid feaure 2	this is a directed sequence where we held the valid to low to check the termination of the transaction based on the valid signal	directed	we check the functionality of the outputs using checkers comparing the output with the reference output from golden model
restart feature 2	this is a directed sequence where we held the restart request to 1 to check the restarting feature of the control module	directed	we check the functionality of the outputs using checkers comparing the output with the reference output from golden model
data transmition feature	we check the data transmition in all previous condition between the first I2C module and the I2C tareet module	directed / randomized	we check the functionality of the outputs using an assertion to check the received data in the I2C tareet module