FREQUENCY RATIO Block

Sponsored by: Si-Vision

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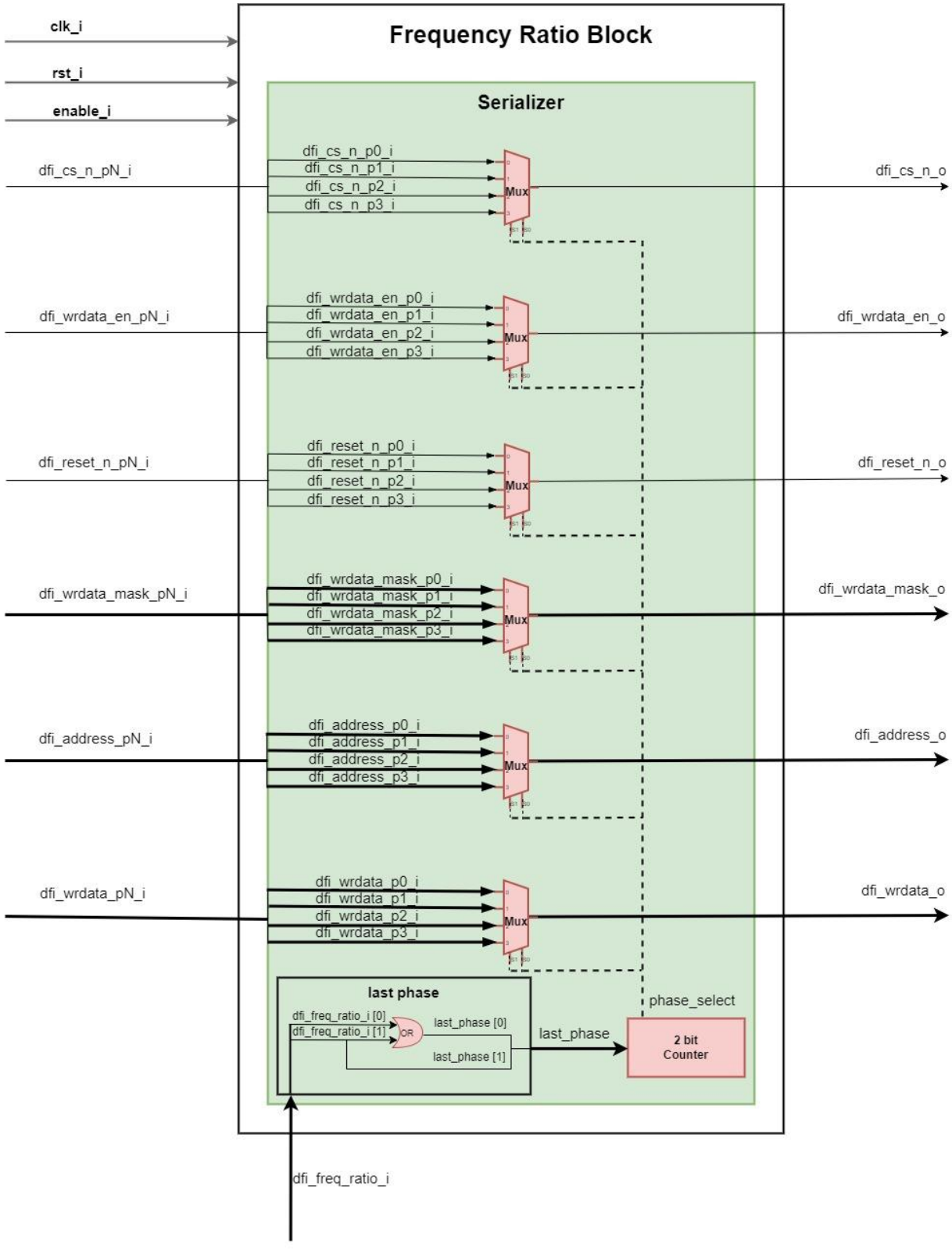
1- Block Diagram



2- I/O Ports Description

Port	Direction	Size	Description
clk_i	Input	1 bit	Input clock signal.
rst_i	Input	1 bit	Input active low asynchronous reset.
enable_i	Input	1 bit	Input enable signal.
dfi_cs_n_pN_i	Input	pNUM_RANK bits	Input pin to select targeted rank on the DIMM, this signal is sent on 4 phases, each phase size is equal to the number of ranks.
dfi_reset_n_pN_i	Input	pNUM_RANK bits	Input pin to reset the targeted rank, this signal is sent on 4 phases, each phase size is equal to the number of ranks.
dfi_address_pN_i	Input	14 bits	Input bus which carries the command sent from the memory controller to the DRAM, this signal is sent on 4 phases, each phase size is 14 bits.
dfi_wrdata_en_pN_i	Input	1 bit	Input signal sent on 4 phases, each phase is 1 bit.
dfi_wrdata_pN_i	Input	2 * pDRAM_SIZE bits	Input bus which carries the data to be stored in the DRAM, this signal is sent on 4 phases, each phase size is double the size of DQ bus(which carries the data to the DRAM from the output of PHY).
dfi_wrdata_mask_pN_i	Input	dfi_wrdata_pN_i / 8 bits	Input bus to mask the sent data, this signal is sent on 4 phases, each bit of this signal is a mask for 8 bits of data, so each phase size is equal to the number of write data bits/8.
dfi_freq_ratio_i	Input	3 bits	Input bus whose value shows if the frequency ratio is 1:1 or 1:2 or 1:4, we will use this signal to determine the number of phases that should be mapped to the output of FREQUENCY RATIO block. This signal has a size of 3 bits.

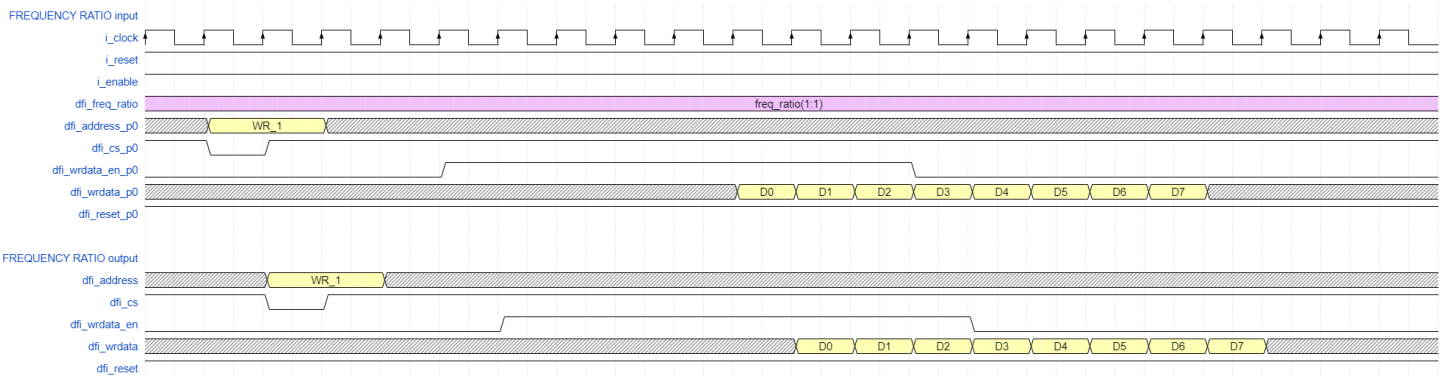
Port	Direction	Size	Description
dfi_cs_n_o	Output	pNUM_RANK bits	Output pin to select targeted rank on the DIMM, this signal is the result of mapping the phases of **dfi_cs_n_pN_i** signal at the input into one signal. Its size is equal to the number of ranks.
dfi_reset_n_o	Output	pNUM_RANK bits	Output pin to reset the targeted rank, this signal is the result of mapping the phases of **dfi_reset_n_pN_i** signal at the input into one signal. Its size is equal to the number of ranks.
dfi_address_o	Output	14 bits	Output bus which carries the command sent from the memory controller to the DRAM, this signal is the result of mapping the phases of **dfi_address_pN_i** signal at the input into one signal. Its size is 14 bits.
dfi_wrdata_en_o	Output	1 bit	Output signal of a size equal to 1 bit. This signal is the result of mapping the phases of **dfi_wrdata_en_pN_i** signal at the input into one signal.
dfi_wrdata_o	Output	2 * pDRAM_SIZE bits	Output bus which carries the data to be stored in the DRAM, this signal is the result of mapping the phases of **dfi_wrdata_pN_i** signal at the input into one signal. Its size is double the size of DQ bus(which carries the data to the DRAM from the output of PHY).
dfi_wrdata_mask_o	Output	dfi_wrdata_pN _i / 8 bits	Output bus to mask the data sent, this signal is the result of mapping the phases of **dfi_wrdata_mask_pN_i** signal at the input into one signal. Each bit of this signal is a mask for 8 bits of data, so its size is equal to the number of write data bits/8.

3- Internal Signals

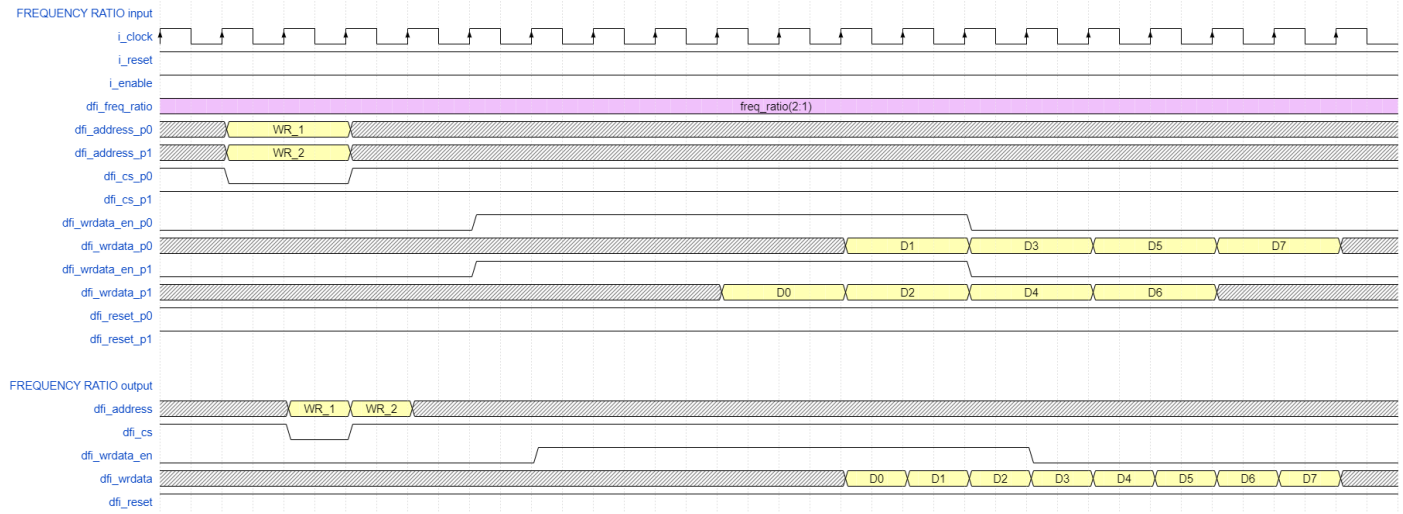
Signal	Size	Description
last_phase	2 bits	This signal represents the last phase that should be mapped to the output. Its size is 2 bits. If the frequency ratio is 1:1, then **last_phase** is 00 and if frequency ratio is 1:2, then **last_phase** is 01 and if frequency ratio is 1:4, then **last_phase** is 11.
phase_select	2 bits	The output of the counter, it is also the MUX selector, it selects the phase that should be mapped from the MUX input to the output. This signal is compared with **last_phase** signal and when they are equal the counter will be reset.

4- Timing Diagrams

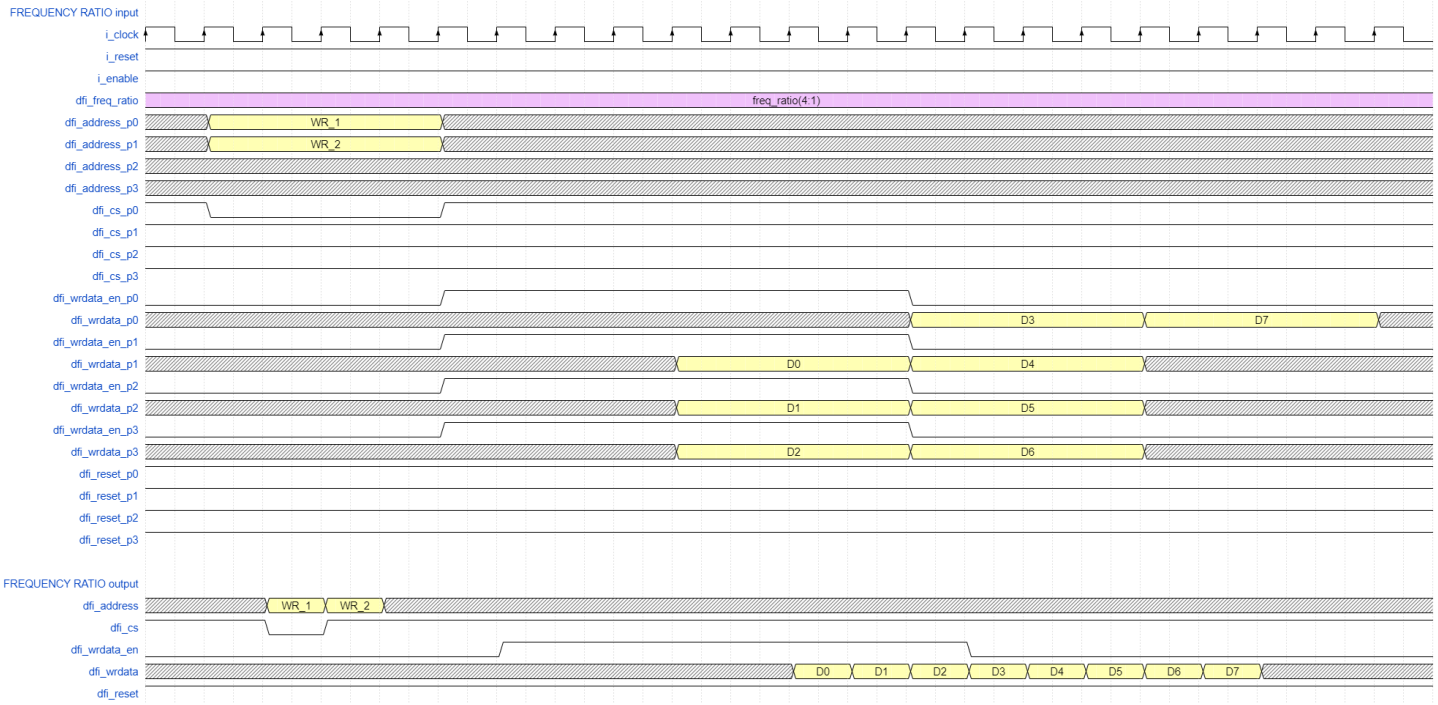
- 1:1 Frequency Ratio



- 1:2 Frequency Ratio



- 1:4 Frequency Ratio

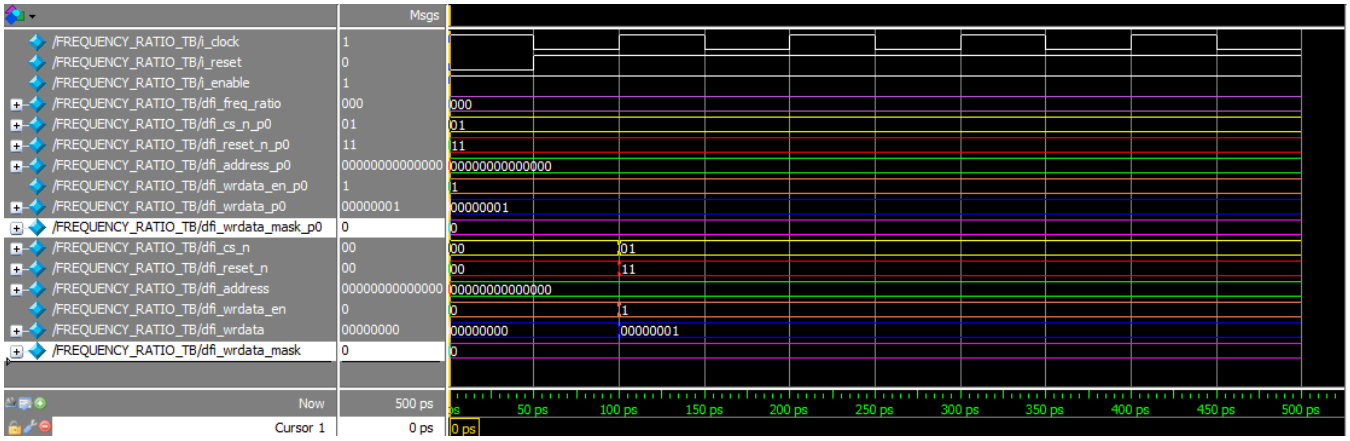


5- Block Implementation

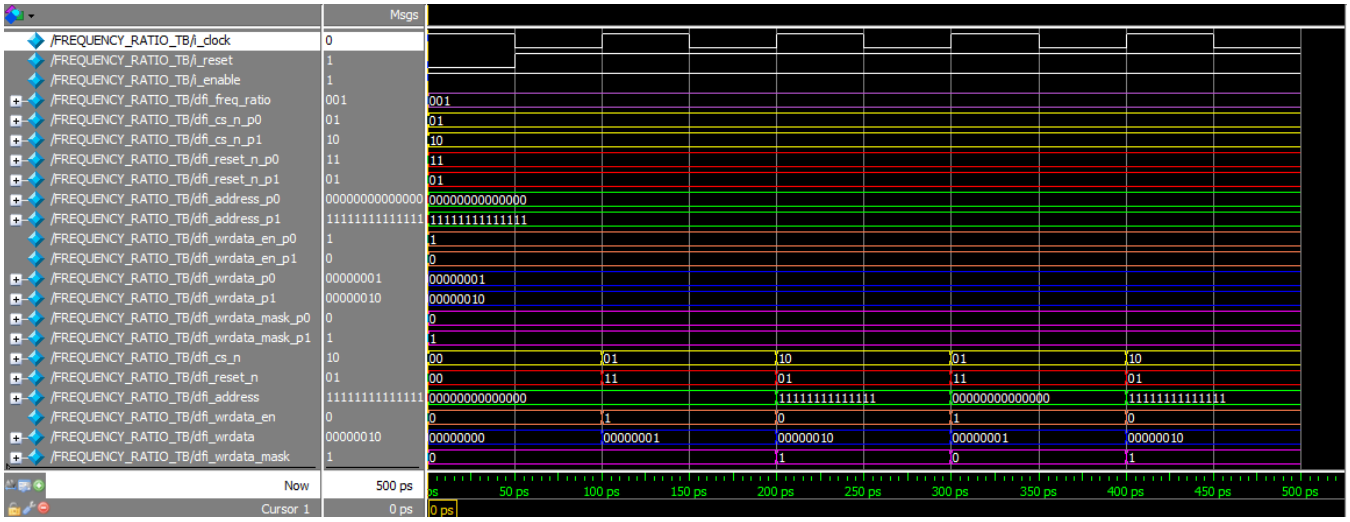
- All signals sent from MC to PHY should pass through this block.
- Frequency Ratio Block converts the signals from MC interface to PHY interface.
- At initialization before any operation, this block should read an input from the register file called dfi_freq_ratio_i.
- Each signal is sent from MC to PHY on maximum 4 different phases, Frequency Ratio Block should out all these signals on one phase only.
- dfi_freq_ratio_i signal determines the number of phases where each signal come on to this block, for example:
    - dfi_freq_ratio_i = 000 → each signal is sent on 1 phase.
    - dfi_freq_ratio_i = 001 → each signal is sent on 2 phases.
    - dfi_freq_ratio_i = 010 → each signal is sent on 4 phases.
- This block is a serializer block.

6- Simulation Results

- 1:1 Frequency Ratio



- 1:2 Frequency Ratio



- 1:4 Frequency Ratio