



# FREQUENCY RATIO Block

Sponsored by: Si-Vision

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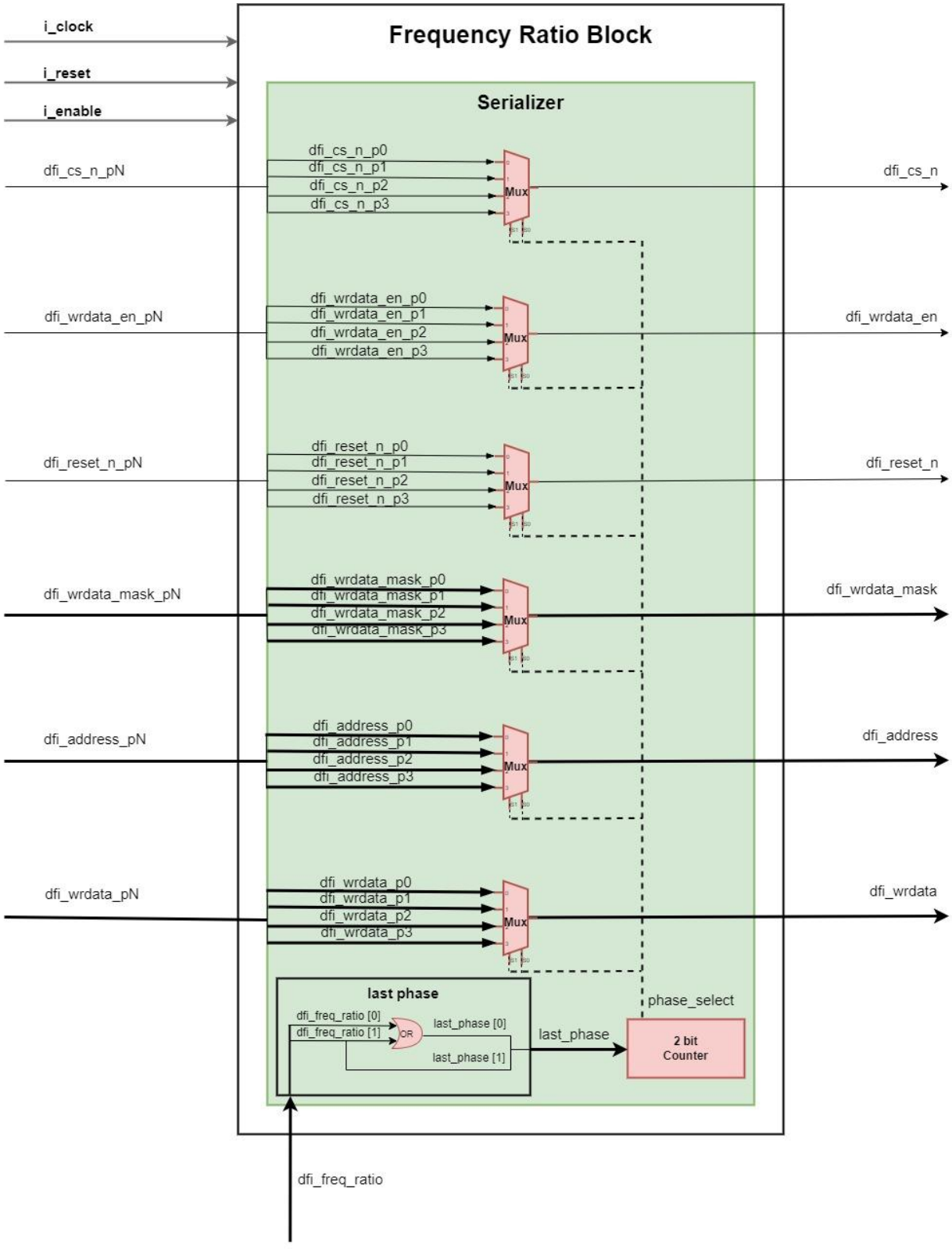
# 1- Block Diagram



## 2- I/O ports description

| Port | Type | Size |
|---|---|---|
| i_clock | Input | 1 bit |
| i_reset | Input | 1 bit |
| i_enable | Input | 1 bit |
| dfi_cs_n_pN | Input | NUM_RANK bits |
| dfi_wrdata_en_pN | Input | 1 bit |
| dfi_reset_n_pN | Input | NUM_RANK bits |
| dfi_wrdata_mask_pN | Input | dfi_wrdata_pN / 8 bits |
| dfi_address_pN | Input | 14 bits |
| dfi_wrdata_pN | Input | 2 * DEVICE_TYPE bits |
| dfi_freq_ratio | Input | 3 bits |
| dfi_cs_n | Output | NUM_RANK bits |
| dfi_wrdata_en | Output | 1 bit |
| dfi_reset_n | Output | NUM_RANK bits |
| dfi_wrdata_mask | Output | dfi_wrdata_pN / 8 bits |
| dfi_address | Output | 14 bits |
| dfi_wrdata | Output | 2 * DEVICE_TYPE bits |

- Input ports:
  - **i_clock:** input clock signal.
  - **i_reset:** input active low asynchronous reset.
  - **i_enable:** input enable signal.
  - **dfi_cs_n_pN:** input pin to select targeted rank on the DIMM, this signal is sent on 4 phases, each phase size is equal to the number of ranks.
  - **dfi_wrdata_en_pN:** input signal sent on 4 phases, each phase is 1 bit.
  - **dfi_reset_n_pN:** input pin to reset the targeted rank, this signal is sent on 4 phases, each phase size is equal to the number of ranks.
  - **dfi_wrdata_mask_pN:** input bus to mask the sent data, this signal is sent on 4 phases, each bit of this signal is a mask for 8 bits of data, so each phase size is equal to the number of write data bits/8.
  - **dfi_address_pN:** input bus which carries the command sent from the memory controller to the DRAM, this signal is sent on 4 phases, each phase size is 14 bits.
  - **dfi_wrdata_pN:** input bus which carries the data to be stored in the DRAM, this signal is sent on 4 phases, each phase size is double the size of DQ bus(which carries the data to the DRAM from the output of PHY).

- **dfi_freq_ratio:** input bus whose value shows if the frequency ratio is 1:1 or 1:2 or 1:4, we will use this signal to determine the number of phases that should be mapped to the output of FREQUENCY RATIO block. This signal has a size of 3 bits.

## Output ports:

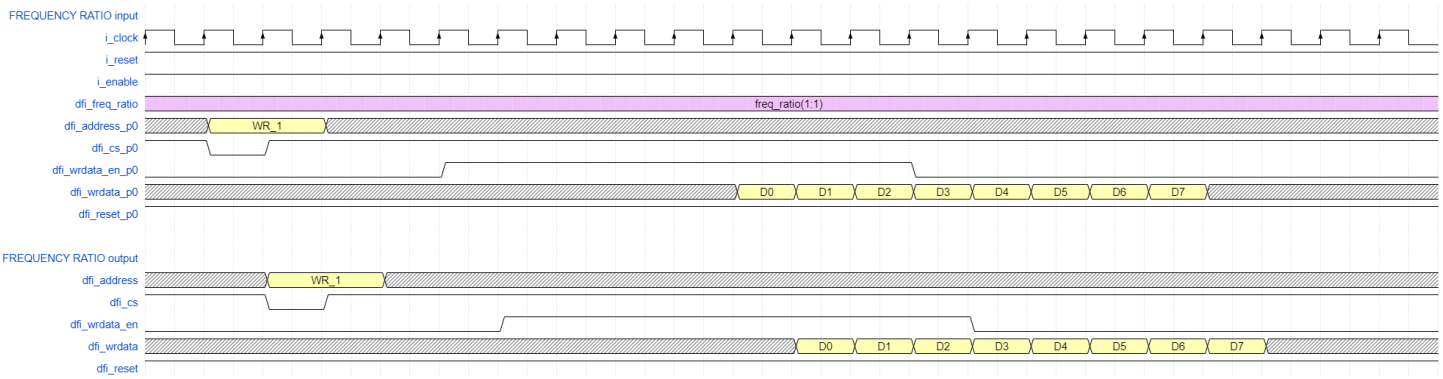
- **dfi_cs_n:** output pin to select targeted rank on the DIMM, this signal is result of mapping the phases of **dfi_cs_n_pN** signal at the input into one signal. Its size is equal to the number of ranks.
- **dfi_wrdata_en:** output signal of a size equal to 1 bit. this signal is result of mapping the phases of **dfi_wrdata_en_pN** signal at the input into one signal.
- **dfi_reset_n:** output pin to reset the targeted rank, this signal is result of mapping the phases of **dfi_reset_n_pN** signal at the input into one signal. Its size is equal to the number of ranks.
- **dfi_wrdata_mask:** output bus to mask the sent data, this signal is result of mapping the phases of **dfi_wrdata_mask_pN** signal at the input into one signal. each bit of this signal is a mask for 8 bits of data, so its size is equal to the number of write data bits/8.
- **dfi_address:** output bus which carries the command sent from the memory controller to the DRAM, this signal is result of mapping the phases of **dfi_address_pN** signal at the input into one signal. Its size is 14 bits.
- **dfi_wrdata:** output bus which carries the data to be stored in the DRAM, this signal is result of mapping the phases of **dfi_wrdata_pN** signal at the input into one signal. Its size is double the size of DQ bus(which carries the data to the DRAM from the output of PHY).

## Internal signals:

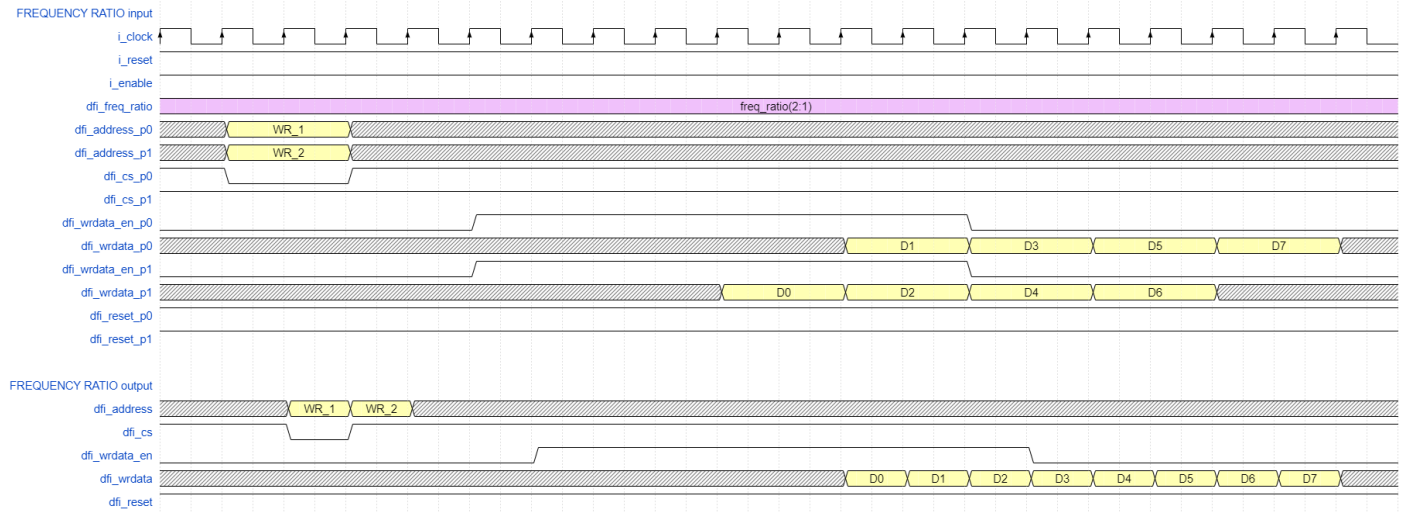
- **last_phase:** this signal represents the last phase that should be mapped to the output. Its size is 2 bits. If the frequency ratio is 1:1, then **last_phase** is 00 and if frequency ratio is 1:2, then **last_phase** is 01 and if frequency ratio is 1:4, then **last_phase** is 11.
- **phase_select:** the output of the counter, it is also the MUX selector, it selects the phase that should be mapped from the MUX input to the output. This signal is compared with **last_phase** signal and when they are equal the counter will be reset.

# 3- Timing Diagrams

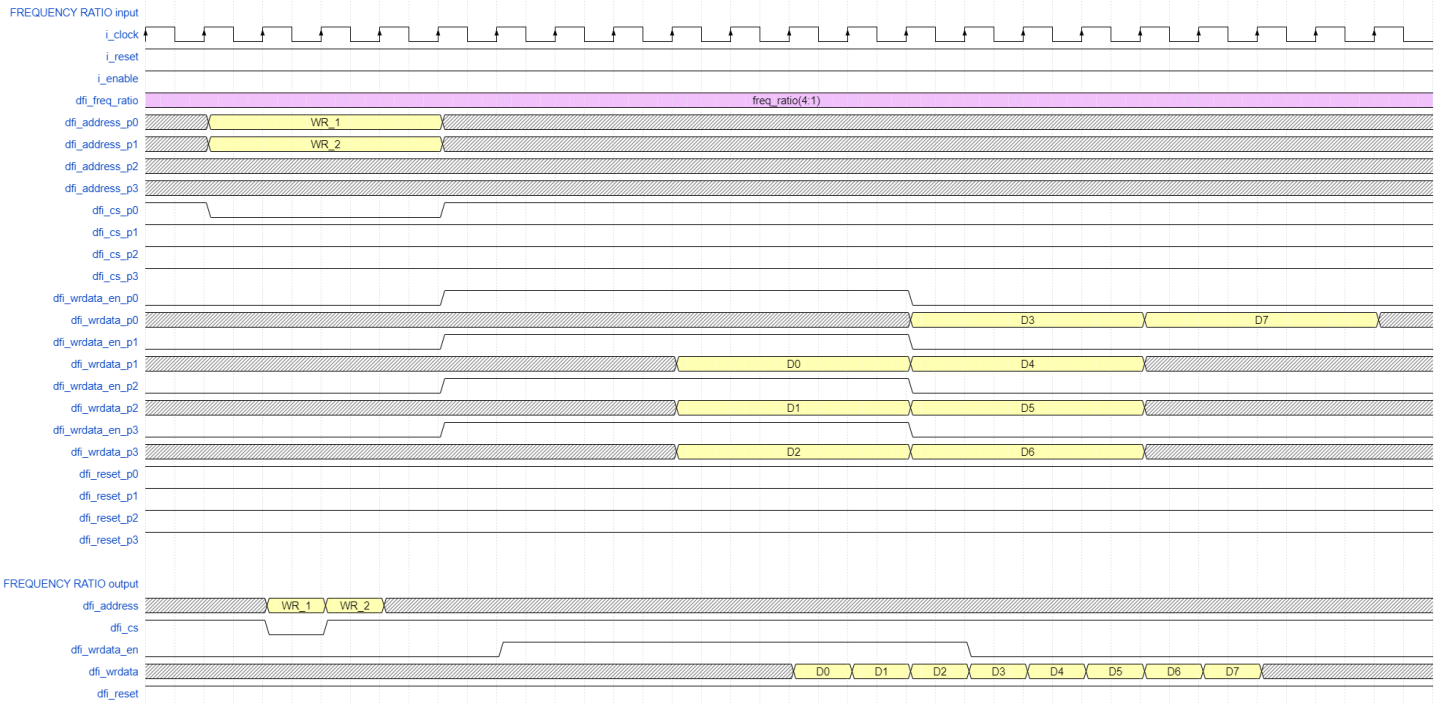
- 1:1 Frequency Ratio




- 1:2 Frequency Ratio



- 1:4 Frequency Ratio

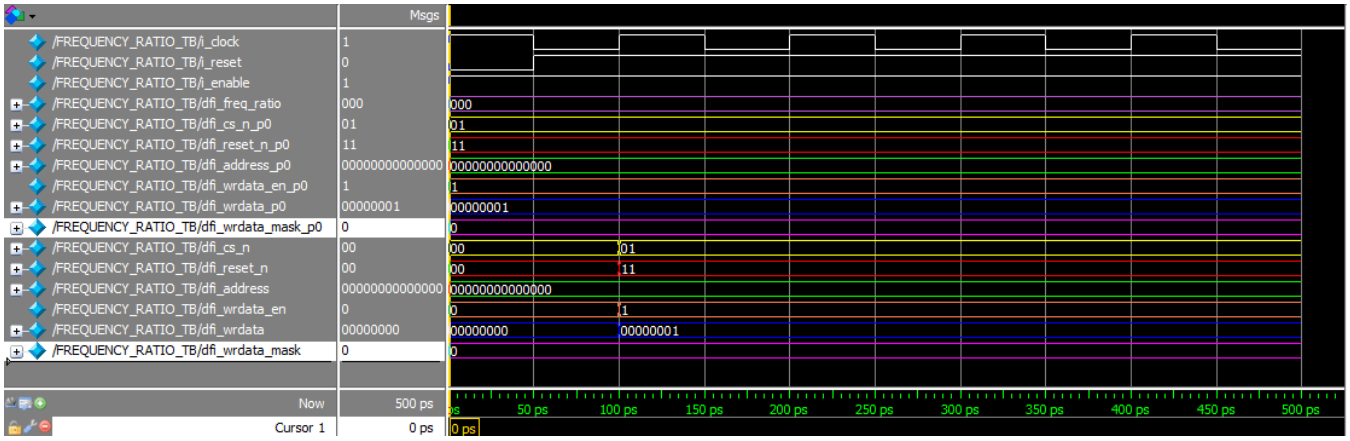



# 4- Block implementation

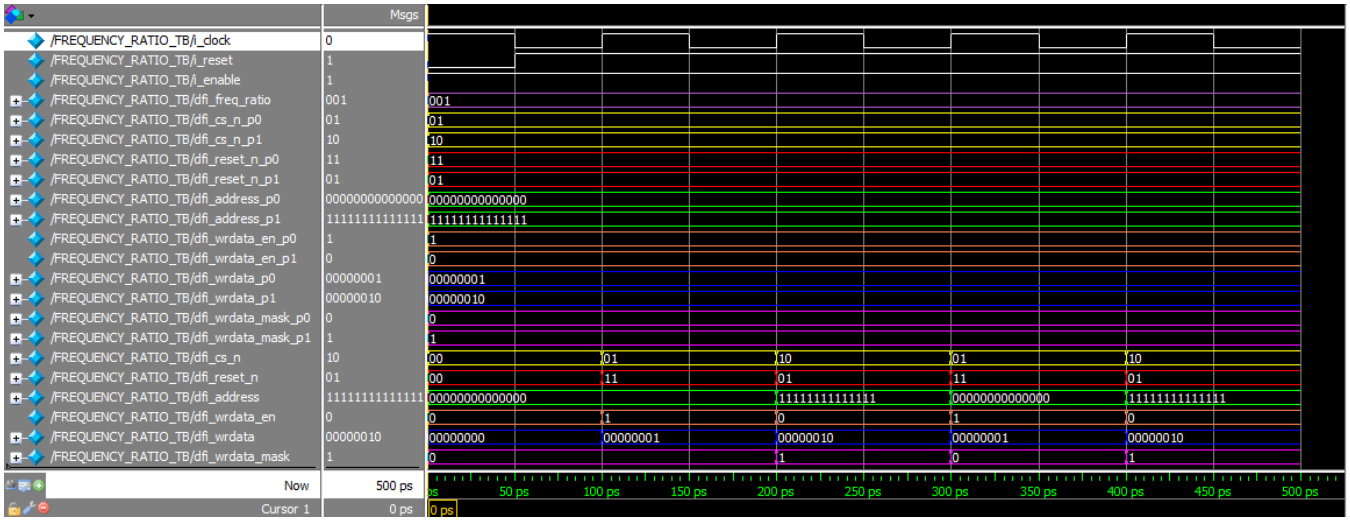
- All signals sent from MC to PHY should pass through this block.
- Frequency Ratio Block converts the signals from MC interface to PHY interface.
- At initialization before any operation, this block should read an input from the register file called dfi_freq_ratio.
- Each signal is sent from MC to PHY on maximum 4 different phases, Frequency Ratio Block should out all these signals on one phase only.
- dfi_freq_ratio signal determines the number of phases where each signal come on to this block, for example:
    - dfi_freq_ratio = 000 → each signal is sent on 1 phase.
    - dfi_freq_ratio = 001 → each signal is sent on 2 phases.
    - dfi_freq_ratio = 010 → each signal is sent on 4 phases.
- This block is a serializer block.

# 5- Simulation Results

- 1:1 Frequency Ratio




- 1:2 Frequency Ratio



- 1:4 Frequency Ratio