

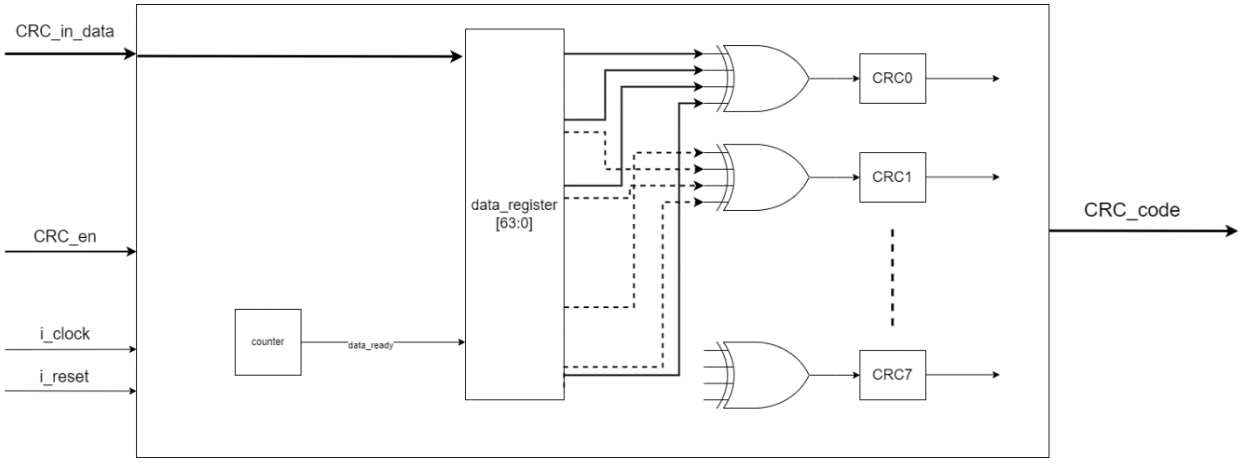


# CRC Block

Sponsored by: Si-Vision

# Contents

# 1- Block diagram.




# 2- I/O ports description.

| Port | Type | Size | From | To |
|---|---|---|---|---|
| i_clock | Input | 1 bit | System | CRC |
| i_reset | Input | 1 bit | System | CRC |
| CRC_in_data | Input | 8* (N/4) bits | Write_data | CRC |
| CRC_en | Input | 1 bit | Write_data | CRC |
| CRC_code | Output | 8* (N/4) bits | CRC | Write_data |

N : parameter indicate the device size (X4, X8, X16)

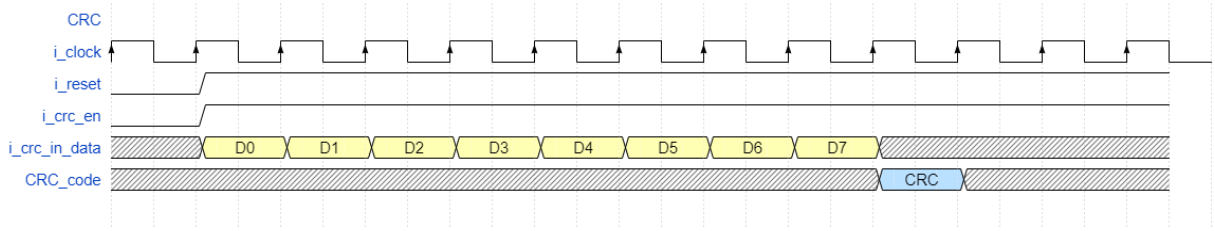
## Input ports:

- **i_clock**: clock signal.
- **i_reset**: active low asynchronous reset.
- **CRC_en**: input enable signal to enable the block comes from write data block
- **CRC_in_data**: input data bus from write data block that required to generate crc bits for it.

## Output ports:

- **CRC_code**: output bus that carry crc bits to write block.

## 3- Timing diagram.




## 4- Block implementation

- this block responsible for generating CRC bits to protect the required data
- The block consists of
  - shift register (64 bit) to store input data
  - 8 xor gates to take input data and generate the correct CRC bits (CRC_code(7:0))

- For each clock cycle the data will be stored in data_register.
- After 8 clock cycles the data will be ready to calculate the CRC from it.
- At the $9_{th}$ clock cycle the CRC code will be ready to be fetched (8bits CRC for 64bits of data).
- This block will be duplicated according to the device size.

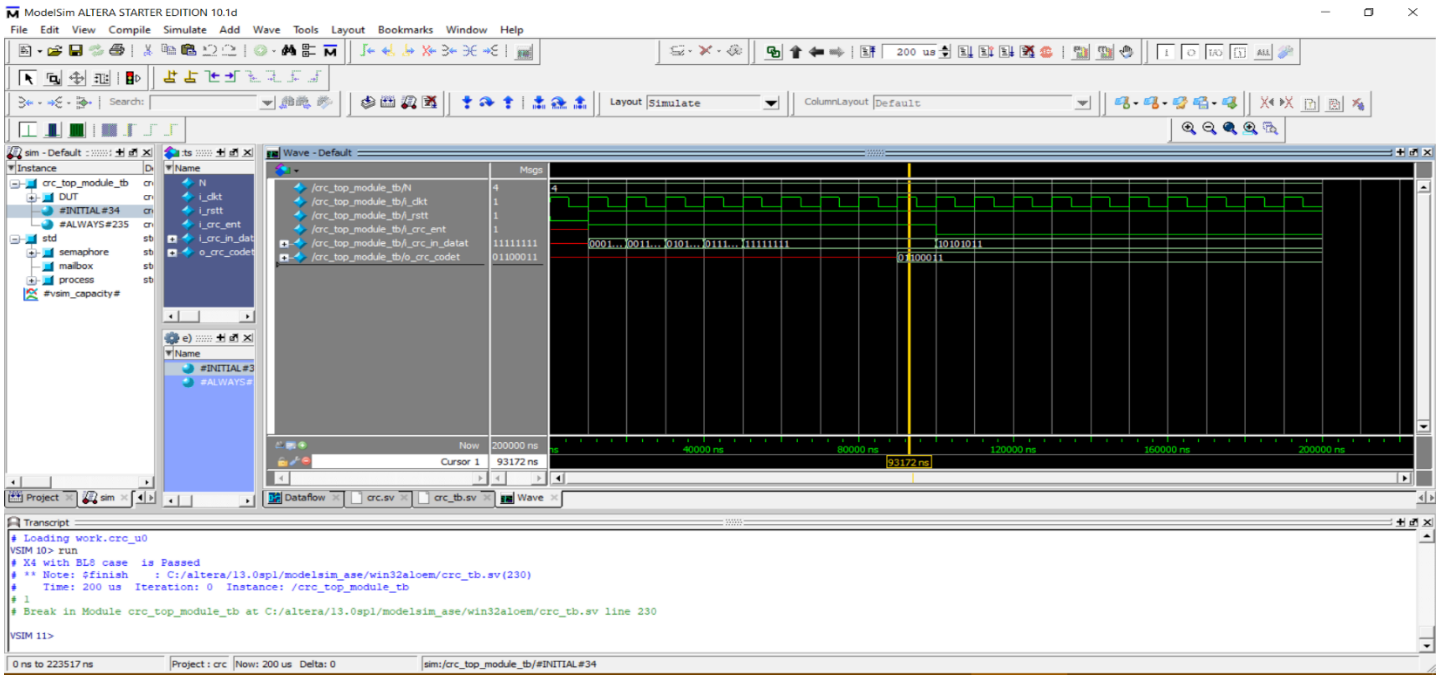
## 5- simulation results

### 1. Device size = 4 (x4) , burst length = 8 (BL8)

CRC_in_data = 64'b b1111_1111_b1111_1111_b1111_1111_b1111_1111_
0111_0110_0101_0100_0011_0010_0001_0000

The correct CRC_code should be = 8'b 0110_0011

The simulation result:

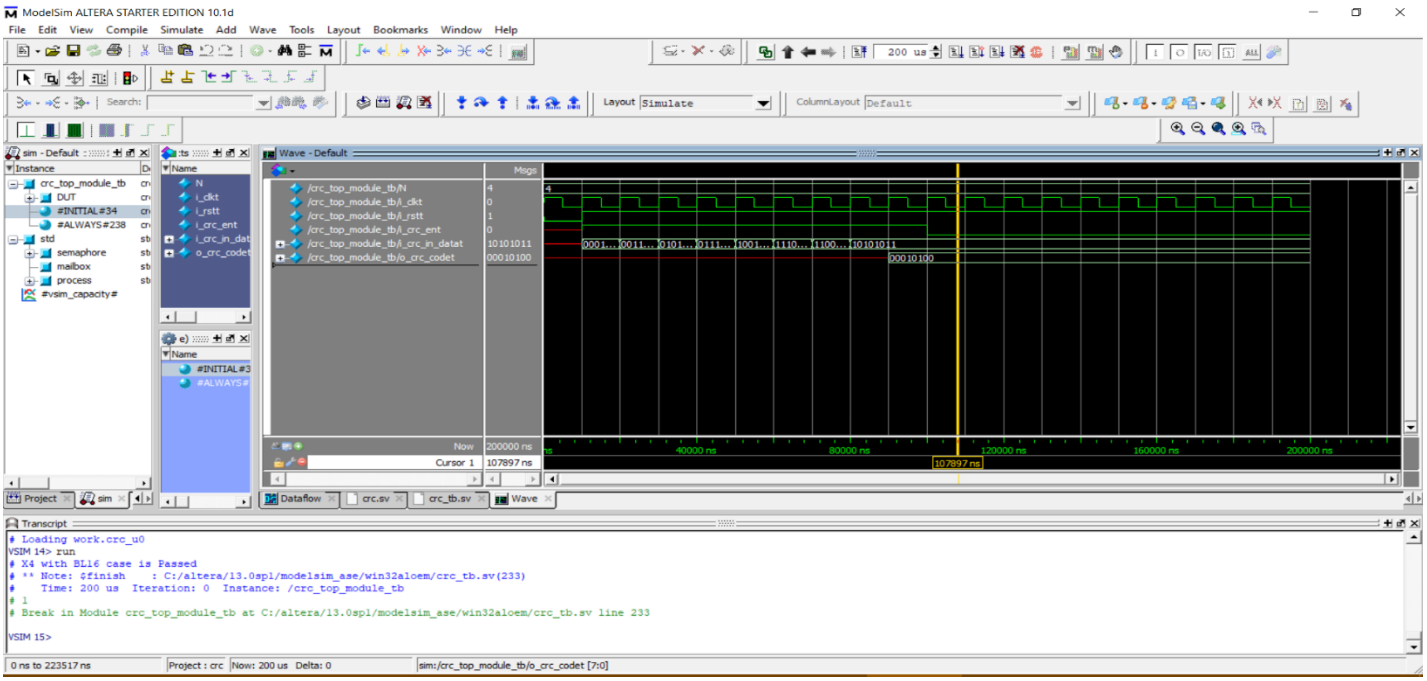


## 2. Device size = 4 (x4) , burst length = 16 (BL16)

CRC_in_data = 64’b 1010_1011_ 1100_1101_ 1110_1111_ 1001_1000
0111_0110_ 0101_0100_ 0011_0010_ 0001_0000

The correct CRC_code should be = 8’b 0001_0100

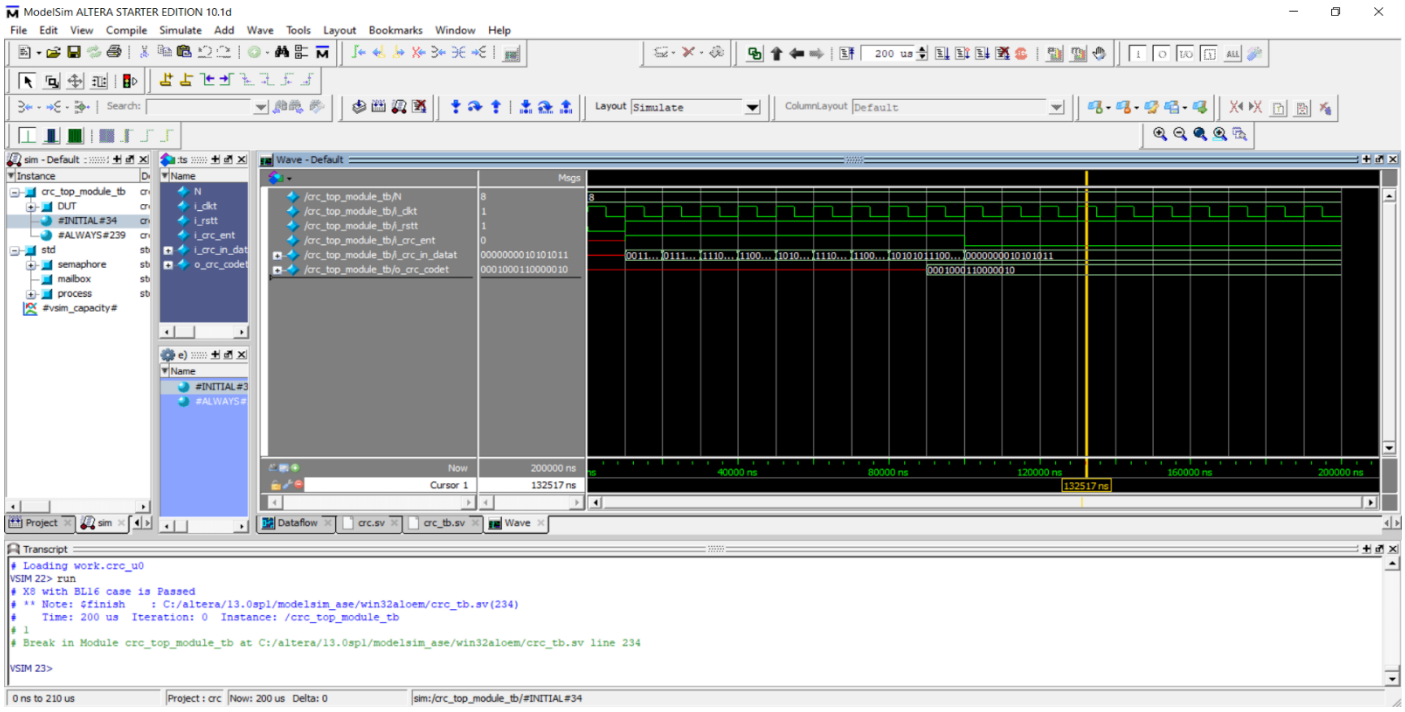
The simulation result:



## 3. Device size = 8 (x8) , burst length = 16 (BL16)

CRC_in_data = 128’b 1010_1011_1001_1000_ 1100_1101_0111_0110
1110_1111_0101_0100_ 1010_1011_0011_0010
1100_1101_0001_0000_ 1110_1111_1001_1000
0111_0110_0101_0100_ 0011_0010_0001_0000

The correct CRC_code should be = 16’b 0001_0001_1000_0010
The simulation result:



## 4. Device size = 16 (x16) , burst length = 16 (BL16)

The correct CRC_code should be = 32’b 0110_0101_0110_0101
0110_0101_ 0110_0101

The simulation result: