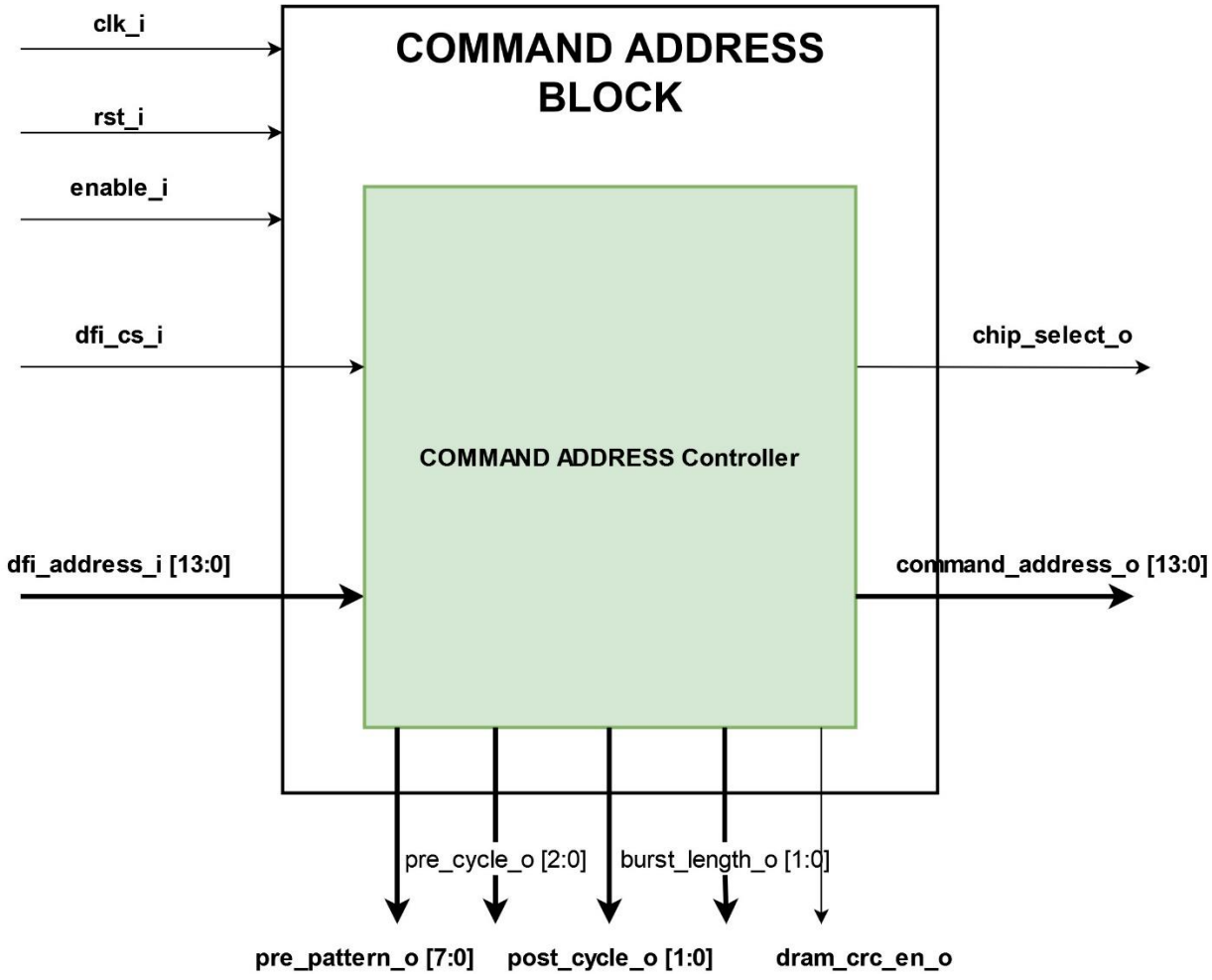
COMMAND ADDRESS Block

Sponsored by: Si-Vision

Contents

1- Block diagram.

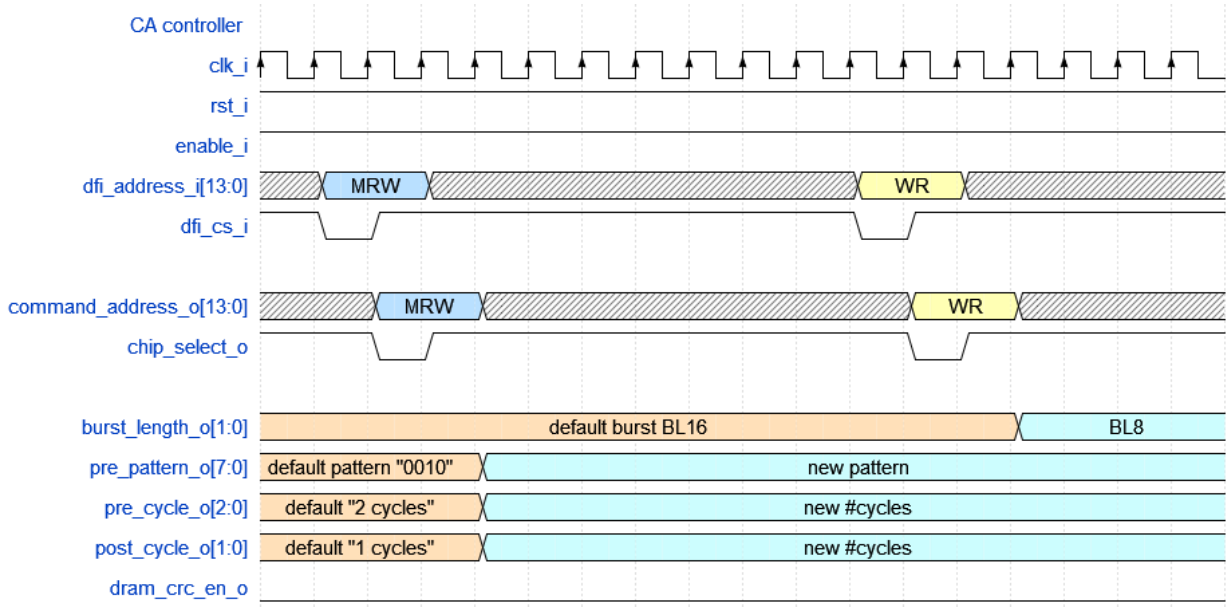


2- I/O ports description.

Port	Direction	Size	Description
clk_i	Input	1 bit	From system to command address (CA) controller, input clock signal.
rst_i	Input	1 bit	From system to CA controller, input active low asynchronous reset.
enable_i	Input	1 bit	From system to CA controller, input enable signal to enable the block.
dfi_address_i	Input	14 bits	From frequency ratio block to CA controller, input bus holds the command sent from the memory controller (MC) to the DRAM, the width of this bus is equal 14 bits as it mapped to CA bus on JEDEC interface.
dfi_cs_i	Input	NUM_RANK bits	From frequency ratio block to CA controller, input pin chip select to select the target rank on the DIMM, the size of this signal is equal to the number of ranks.
command_address_o	Output	14 bits	From CA controller to write data (WR) block, output bus holds the command to the DRAM, the width is 14 bits, and the description of the different combination of this bus is mentioned in JEDEC as CA truth table.
chip_select_o	Output	NUM_RANK bits	From CA controller to WR block, output pin chip select to select the target rank on DIMM.
burst_length_o	Output	2 bits	From CA controller to WR block, output bus holds the value of the burst of the coming data. 00: BL16 01: BC8 OTF 10: BL32 (Optional) 11: BL32 OTF (Optional)
pre_pattern_o	Output	8 bits	From CA controller to WR block, output bus holds the pre-amble pattern, the width of this bus is 8 bits equals to the maximum pattern of pre-amble, the default value “00000010”.
pre_cycle_o	Output	3 bits	From CA controller to WR block, output bus holds the number of cycles of the pre-amble pattern, the width of this bus is 3bits. 000: reserved. 010: 2 cycles (default). 011: 3 cycles. 100: 4 cycles.

post_cycle_o	Output	2 bits	From CA controller to WR block, output signal holds the number of cycles of the post-amble pattern. 01: 0.5 cycle. 10: 1.5 cycles.
dram_crc_en_o	Output	1 bit	From CA controller to WR block, output enable signal indicates if DRAM needs CRC or not, the width of this signal is 1 bit, default value “00”. DRAM_CRC_en = 1 CRC enable. DRAM_CRC_en = 0 CRC disable.

3- Timing diagram.



4- Block implementation.

- This block is consist of command address controller.
- The FSM of the controller has 4 different states.
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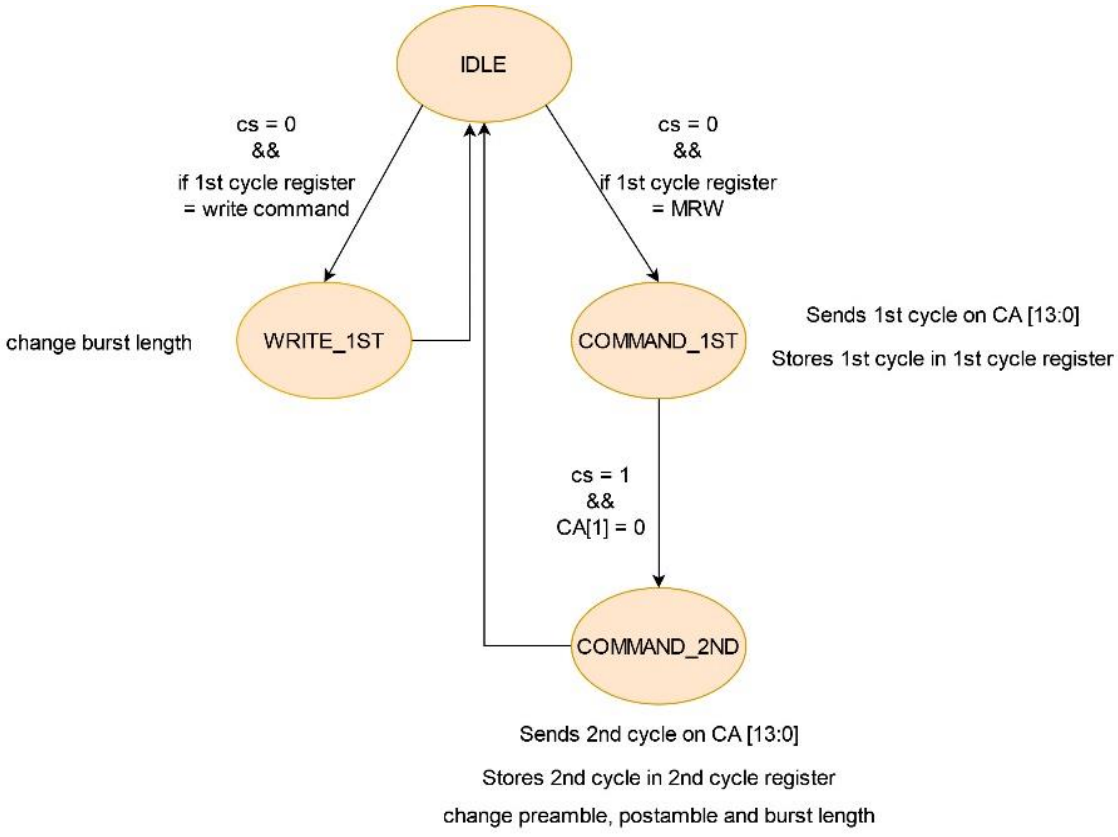
  - COMMAND_1ST: The 1st cycle of the command will be stored and then sent on CA bus.
  - COMMAND_2ND: The 2nd cycle of the command will be stored and then sent on CA bus, the preamble, the postamble, and the CRC enable will be fetched in this state.
  - WRITE_1ST: is optional state, when the block supports the burst length feature, this state extract the burst info from the write command.
- The following figure shows FSM states.

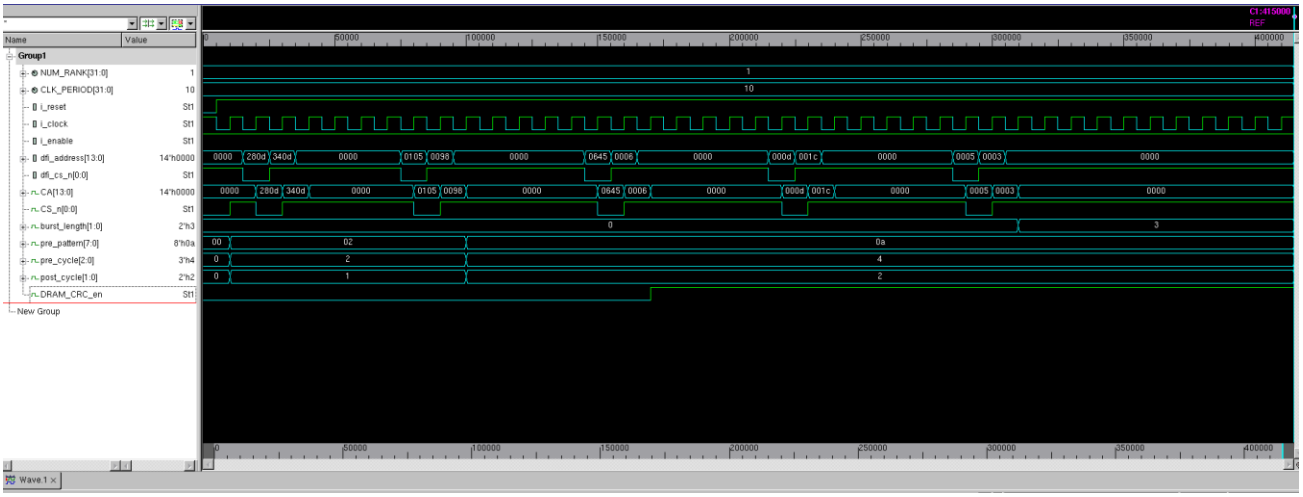


5- Design edits.

In this version of the RTL, the block is able to get the burst length form the mode register write (MWR) command and send it to the write data block through burst_length signal.

This define in the RTL " `define BURST_LENGTH_ENABLE " is used when it is needed to calculate the burst from the command address block, if we don't need this feature, we can just comment this define and the compiler will remove the burst length form the RTL.

6- Test bench Result.



The test bench tests three different scenarios:

1- Single write operation and the latency was 1 clock cycle.
2- Mode register write command to change the pre-amble and post-amble.
3- Mode register write command to change the CRC enable settings.
4- Mode register write command to change the burst length.
5- Single write operation and changing the burst length from default to the alternative setting.