Write operation flow

Sponsored by: Si-Vision

Contents

The subsystem point of view

Figure 21 shows the signals between MC, PHY, and DRAM related to write operation.

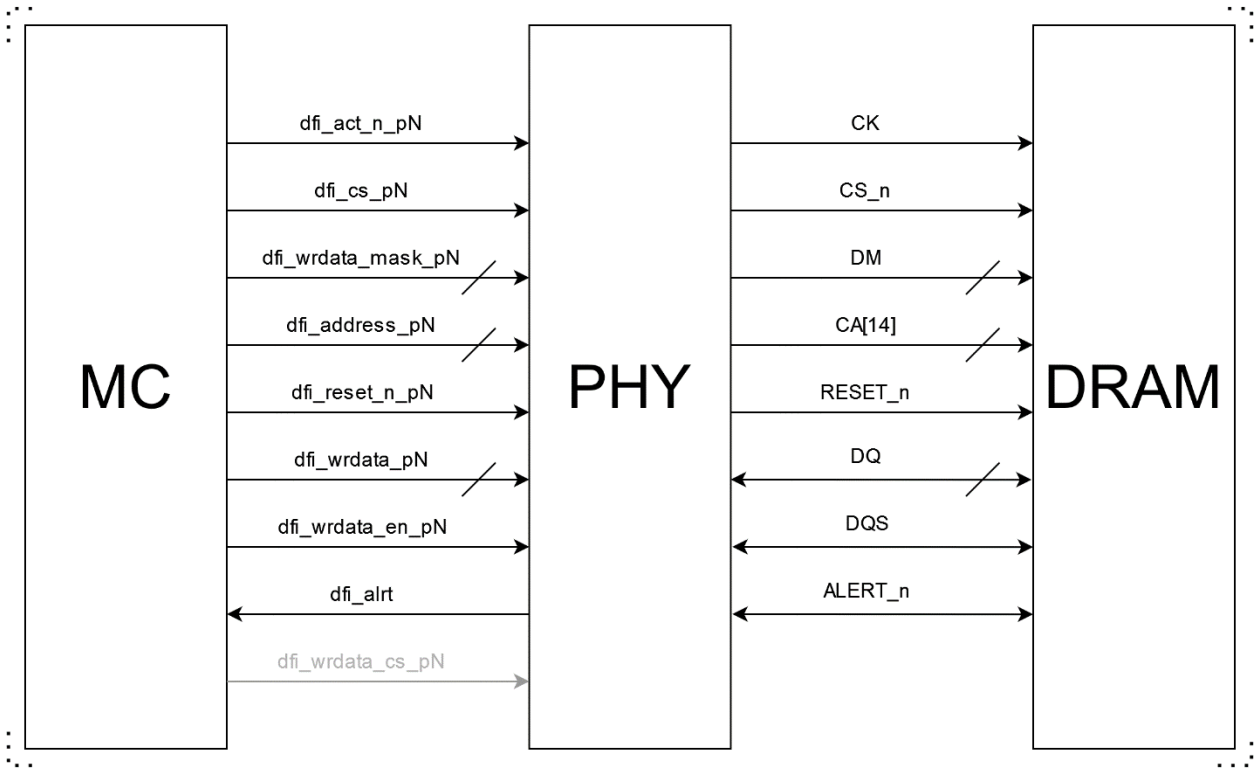

Figure 1 Subsystem

Signal mapping:

1- Dfi_address -> CA [13:0].
2- Dfi_cs_n -> CS.
3- Dfi_wrdata -> DQ.
4- Dfi_wrdata_mask -> DM.
5- Dfi_alrt -> ALERT_n.
6- Dfi_reset_n -> RESET_n.

The Write operation flow

Case (1): Matched System

- Write data enable, write data and dfi command has only single phase.
- Write data enable indicates to PHY that write data will be transmitted in t_{PHY_wrdata} DFI PHY clock cycles.
- Number of cycles Write data enable is activated defines the data burst sent.
- The DFI write data bus width is generally twice the width of the DRAM data bus.

a. Matched System "without timing"

Write operation from MC to PHY:

1. Memory Controller sends the Activate command on the dfi_address bus.
2. Memory Controller sends the chip select signal to encode the Activate command.
3. Memory Controller sends the Write command on the dfi_address bus.
4. Memory Controller sends the chip select signal to encode the Write command.
5. Memory Controller sends the write data enable after sending the write command with certain delay.
6. Memory Controller Sends the write data.
7. Memory Controller disables the write data enable signal, so the PHY stops sending data.

Write operation from PHY to DRAM:

1. PHY sends the chip select signal to DRAM.
2. PHY sends the Activate command on CA[13:0] to DRAM.
3. PHY sends the chip select signal to DRAM.
4. PHY sends the Write command on CA[13:0] to DRAM.
5. PHY sends the DQS before the DQ with Pre-amble time (tWPRE).
6. PHY sends the data to the DRAM.
7. DQS is de asserted after its last valid data is transferred with post-amble time (tWPST).

b. Matched System "with timing"

Write operation from MC to PHY:

1. Memory Controller sends the Activate command on the dfi_address bus.
2. After time called ($t_{PHY\_wrcslat}$) from sending command: MC sends the activate signal to sample the command.
3. Memory Controller sends the Activate command on the dfi_address bus.
4. After time called ($t_{PHY\_wrcslat}$) from sending command: MC sends the activate signal to sample the command.
5. After time called (t_{PHY_wrlat}) from sending command: MC sends the wr_data_en to allow the PHY to send the data.
6. After time called (t_{PHY_wrdata}) from sending command: MC sends the write_data.

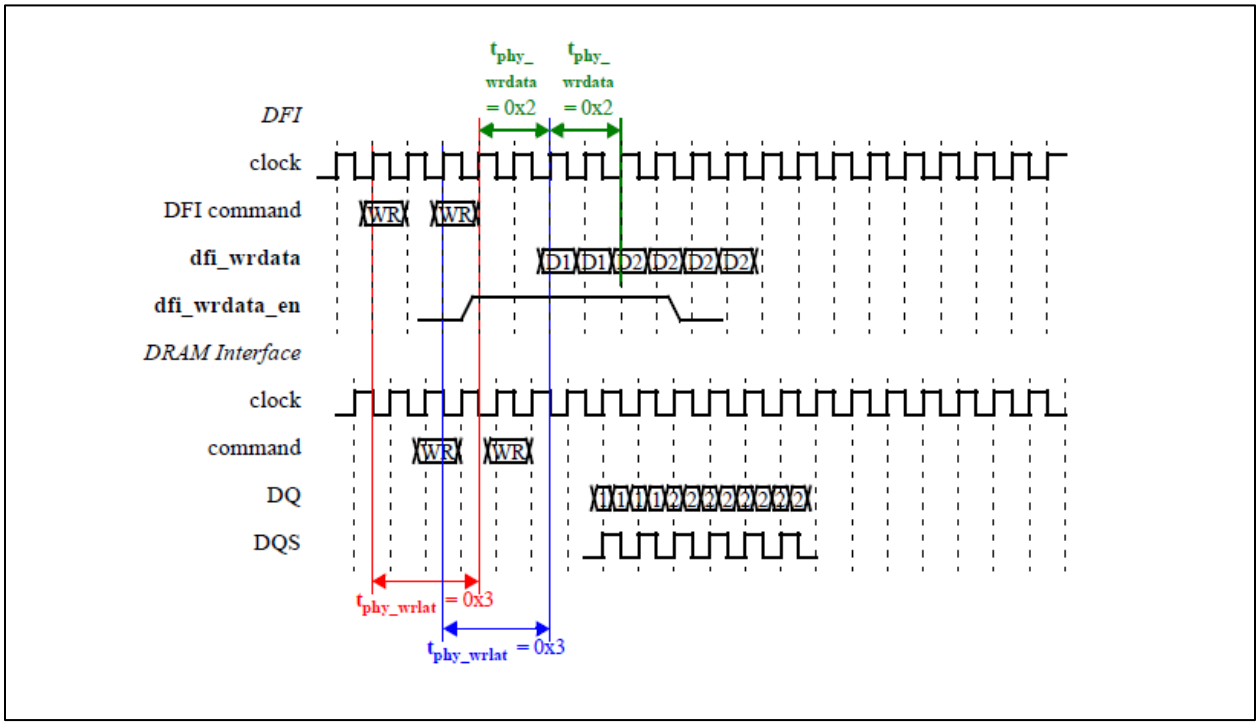

Figure 2:BL8_first_Command_interrupted

Write operation from PHY to DRAM:

1. chip select signal reaches the DRAM.
2. At the first rising edge after activating the chip select, the Activate command is sampled.
3. chip select signal reaches the DRAM.
4. At the first rising edge after activating the chip select, the Write command is sampled.
5. Data reached DRAM after time called write latency.
6. DQS reaches DRAM before the Data with Pre-amble time (tWPRE).
7. DQS is de asserted after its last valid data is transferred with post-amble time (tWPST).

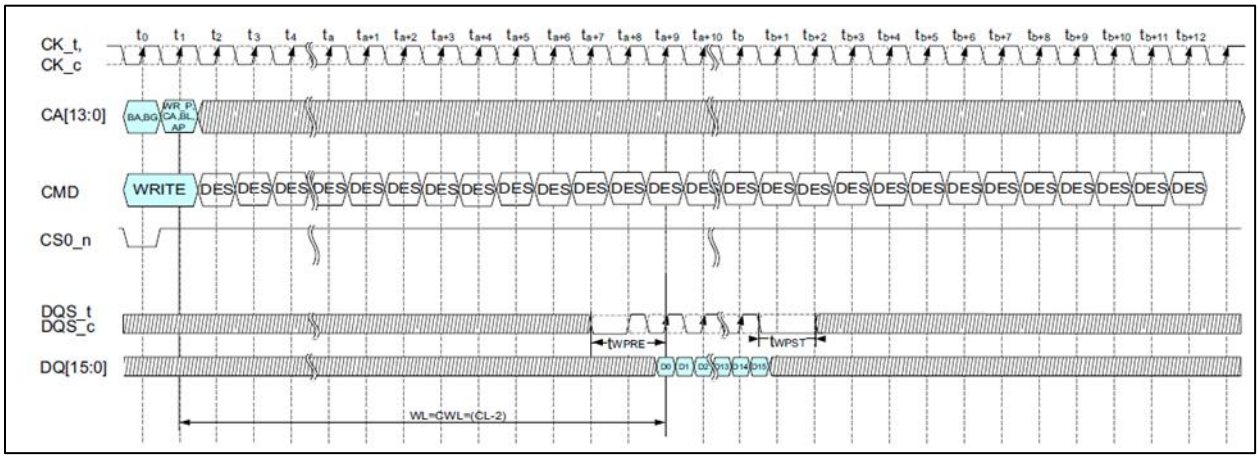

Figure 3:Write Flow in DDR5

Case (2): Frequency Ratio System

- Write data enable, write data and dfi command is duplicated into phases according to the frequency ratio.
- Write data enable indicates to PHY that write data will be transmitted in t_{PHY_wrdata} DFI PHY clock cycles.
- Number of cycles Write data enable is activated defines the data burst sent.
- DFI write data bus width is proportional to the frequency ratio to allow all of the write data that the memory requires to be sent in a single DFI clock cycle.

Timing Parameters

1.Memory Controller to PHY

Timing Parameter	Defined by	Function
$T_{PHY\_wrcslat}$	PHY	○ Defines the number of clock cycles final rising edge of command and its chip select.
T_{PHY_wrlat}	PHY	○ Defines the number of clock cycles between write command and write data enable.
T_{PHY_wrdata}	PHY	○ Defines the number of clock cycles between write data enable signal and write data to be driven on write data signal.
$T_{PHY\_wrcsgap}$	PHY	○ Specify additional delay between consecutive commands that target different chips.
T_{CMD_Lat}	MC	○ Defines the number of cycles between dfi_chip select and command on the MC clock.

2. PHY delay

Timing Parameter	Defined by	Function
T_{ctrl_delay}	Implementation Specific	○ Defines the delay when the PHY receives the signals and exiting signals

CRC FLOW

▪ CRC can be generated by MC or PHY “default MC”

▪ PHY defines the value of PHY crc_mode and according to this value CRC is handled

1. PHY crc_mode = 0 → CRC generation is handled in the MC
2. PHY crc_mode = 1 → CRC generation is handled in the PHY

Case (1): CRC is generated by MC

- MC Sends the CRC Code in the last 2 bits after sending the data.
- MC extends the write data enable to accommodate the data and its CRC Code.

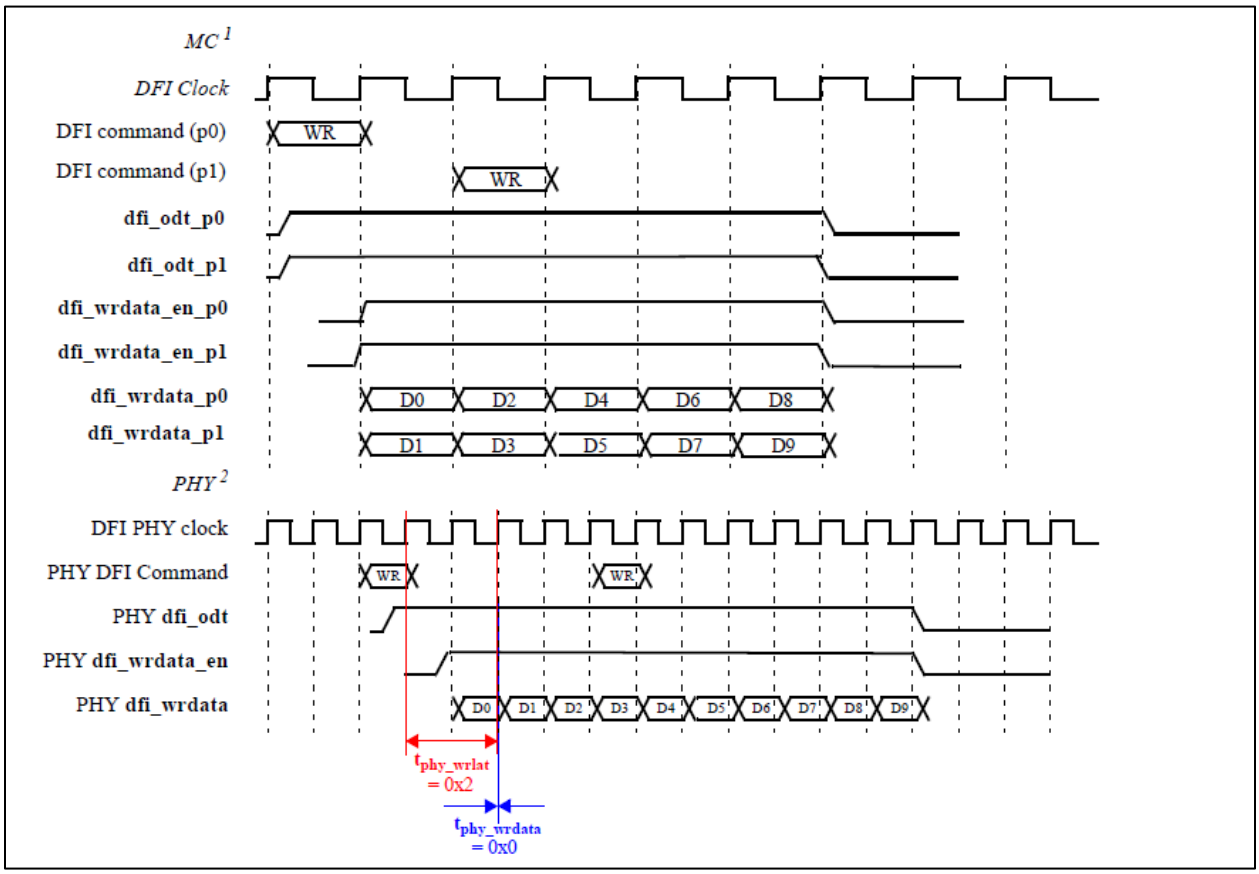

Figure 4: Write Operation Frequency Ratio System

Case (2): CRC is generated by PHY

- PHY is responsible for adding CRC Code after each data.
- MC will not adjust the write data enable to accommodate the CRC as it is not responsible for generating or adding the CRC Code after the data.
- PHY will determine both the burst length and when to generate and add the CRC Code from the width of the write data enable signal.
- When the data enable is not activated PHY will interpret this as to generate and put the CRC Code just for the received burst of data.
- In the case of BC, MC suddenly stops the burst at certain value, so PHY will extend the received BC to its known burst length by ones (1's) then generate the CRC Code for the whole burst.

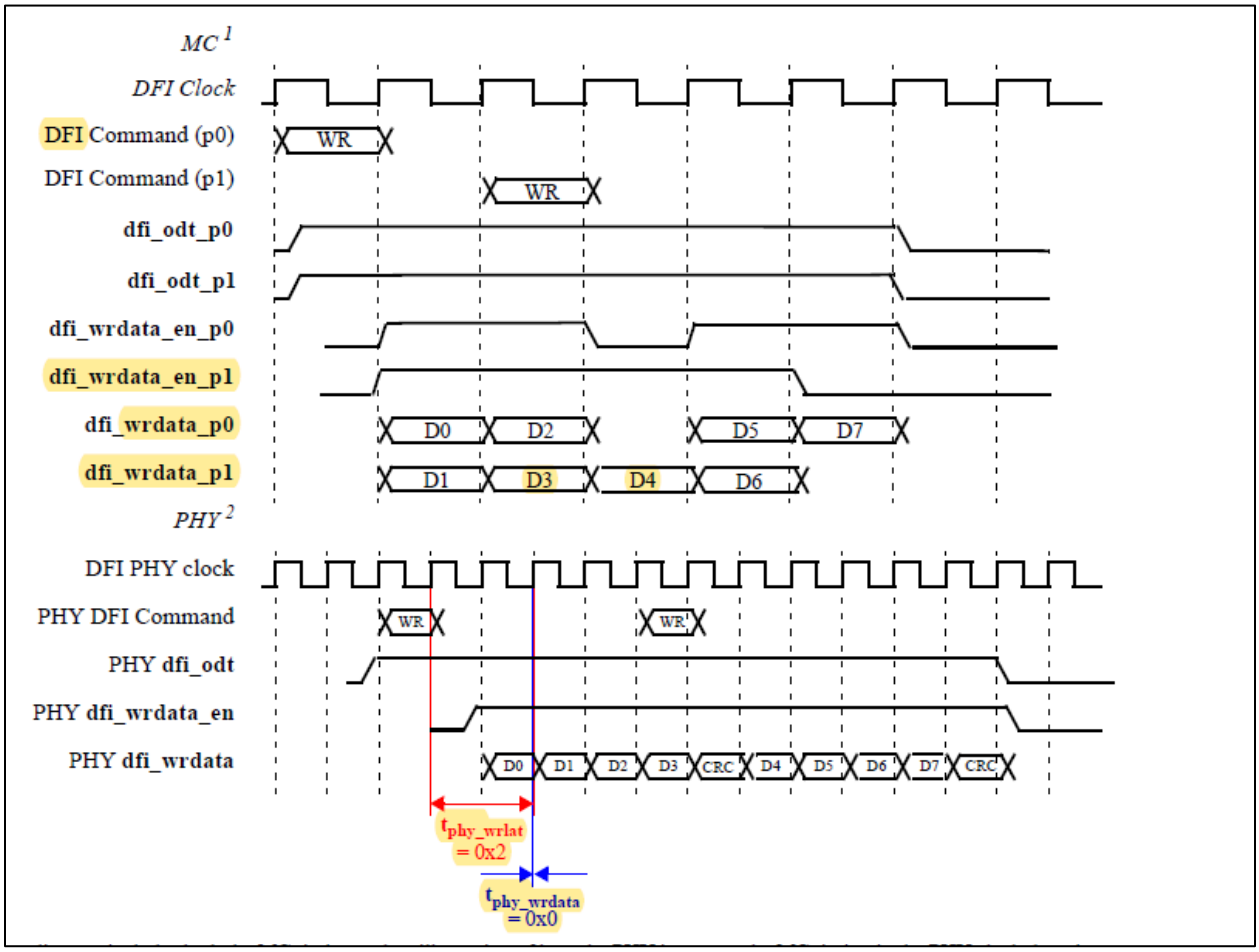

Figure 5: Frequency Ratio including CRC

Whole operation from MC to DRAM

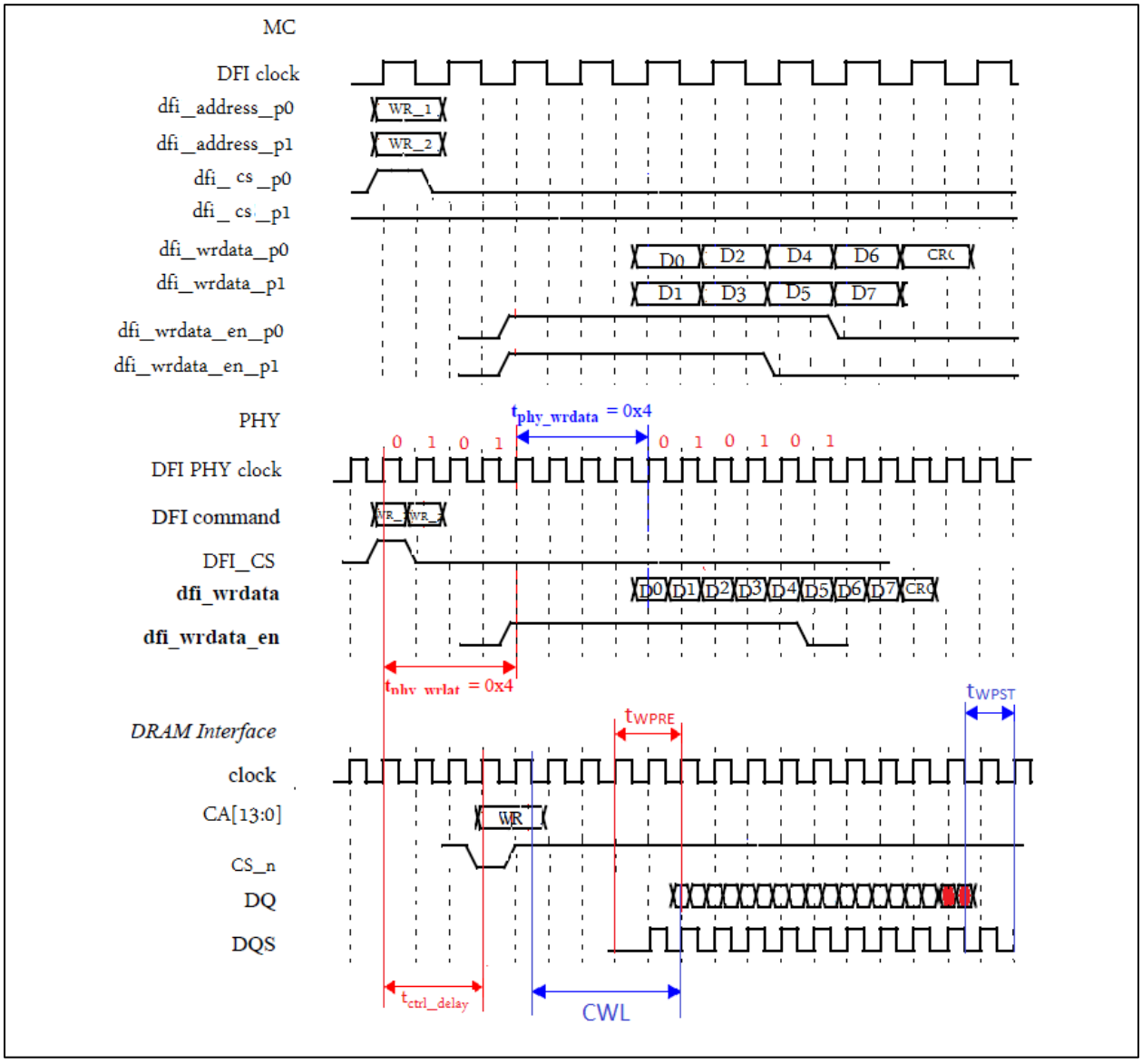

Figure 6: Whole Write Flow

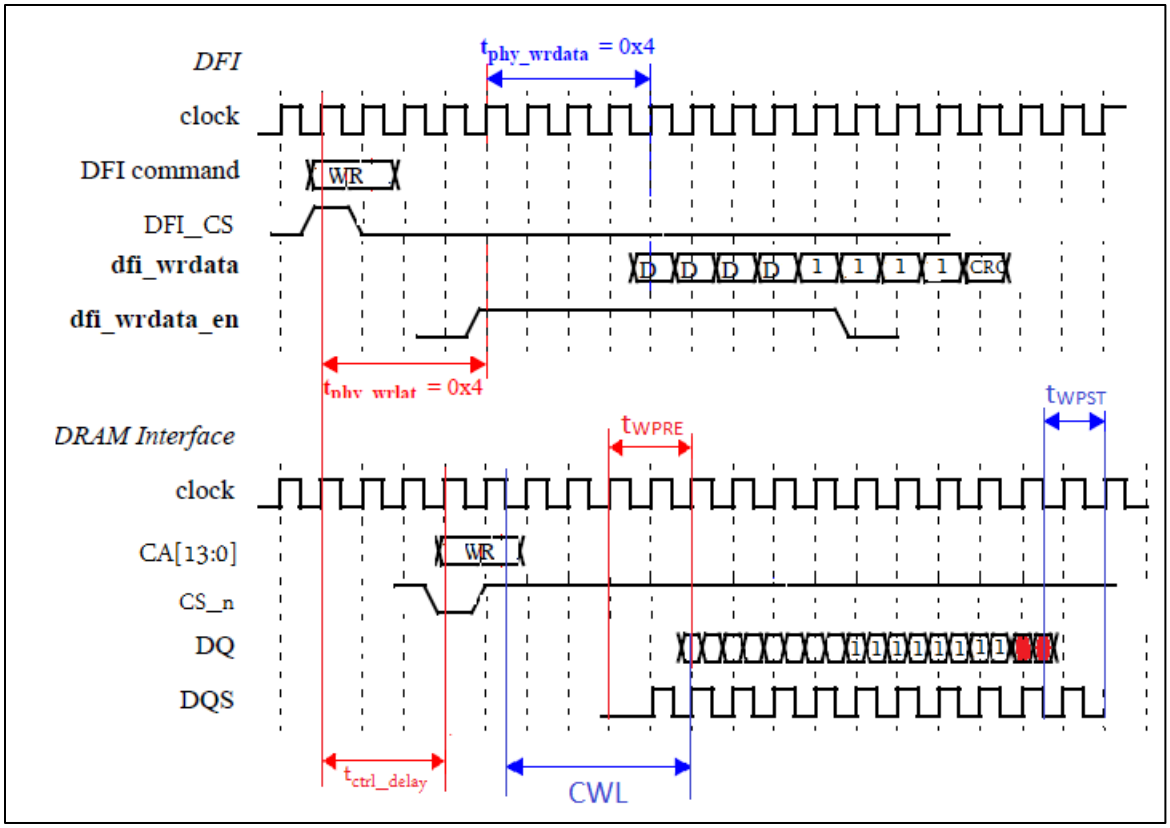

Figure 7:BC8_ CRC Generated From MC

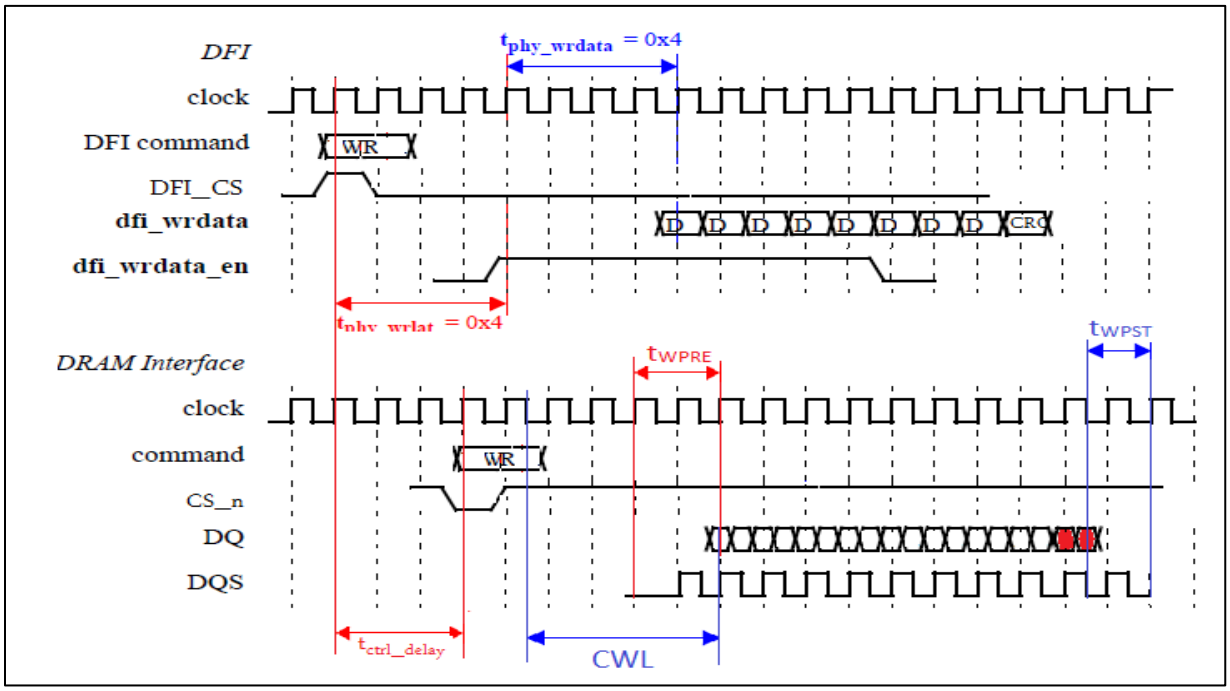

Figure 8:BL16_CRC_Generated from MC

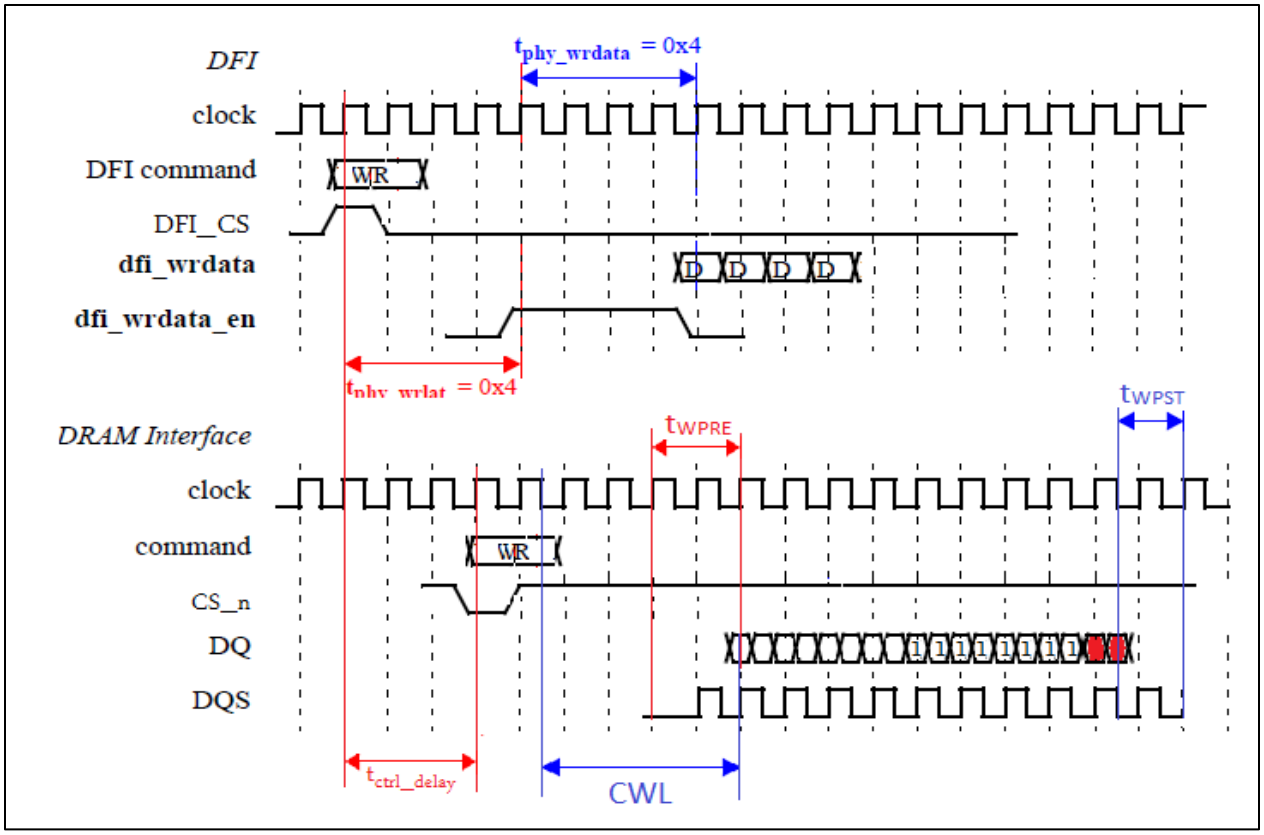

Figure 9:BL8 CRC Generated From PHY