

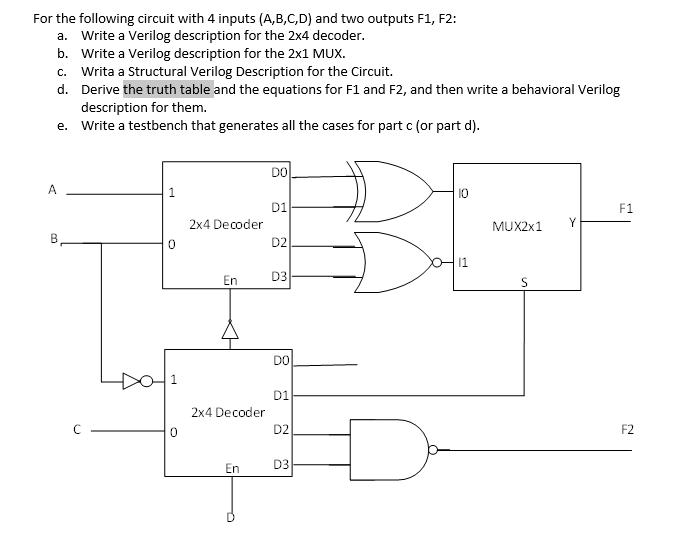
Faculty of Engineering and Technology

Electrical and Computer Engineering Department

Advanced Digital Design ENCS3310

HW#1

* **Abdelrhman Abed . 1193191**
* **INSTRUCTOR: Dr. Abdallatif Abuissa**
* **Section : 2.**
* **Date : 16/8/2023 .**



-The Truth Table:

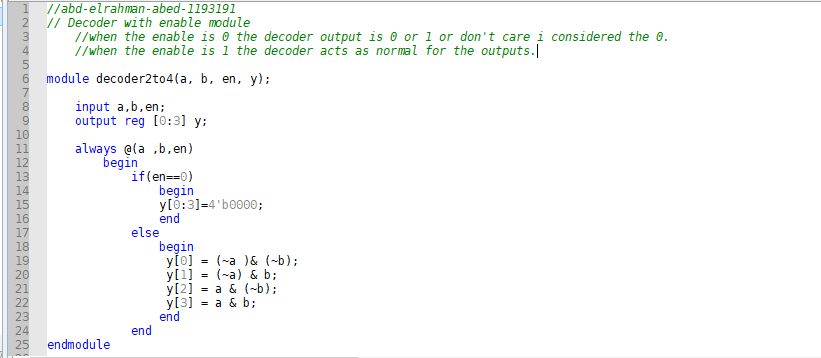
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A | b | c | D | F1 | F2 |
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 |

The output descriptions :

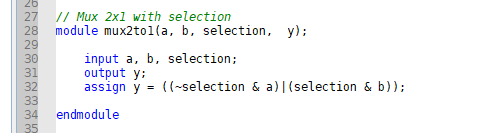
F1 = (~decoderout[2]&I0)|(decoderout[2]& I1 0);

F2 = ~(decoderout2[2] & decoderout2[3]);

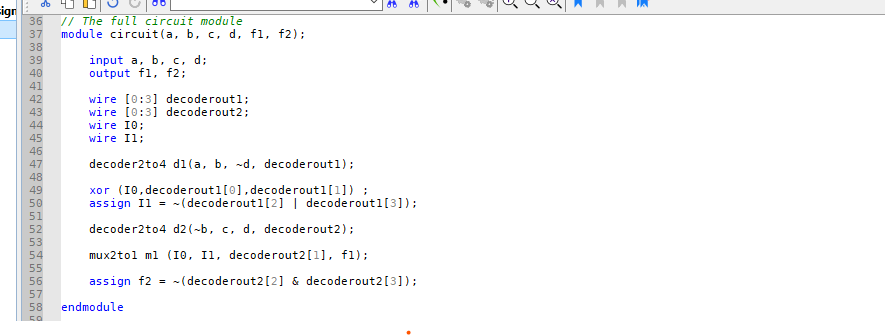
-Verilog module of decoder2to4:



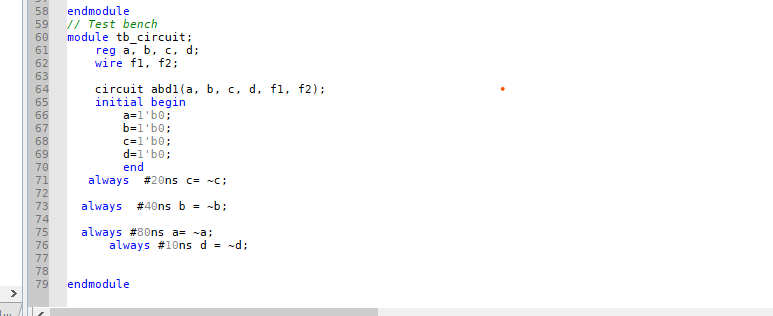
-Verilog module of Mux 2x1 with selection:



-Verilog module of The full circuit module:



-Verilog module of Test Bench:



-test bench simulation wave form :

I considered (a) as the most significant bit by then the simulation became as follows :

