

Digital Clock Project

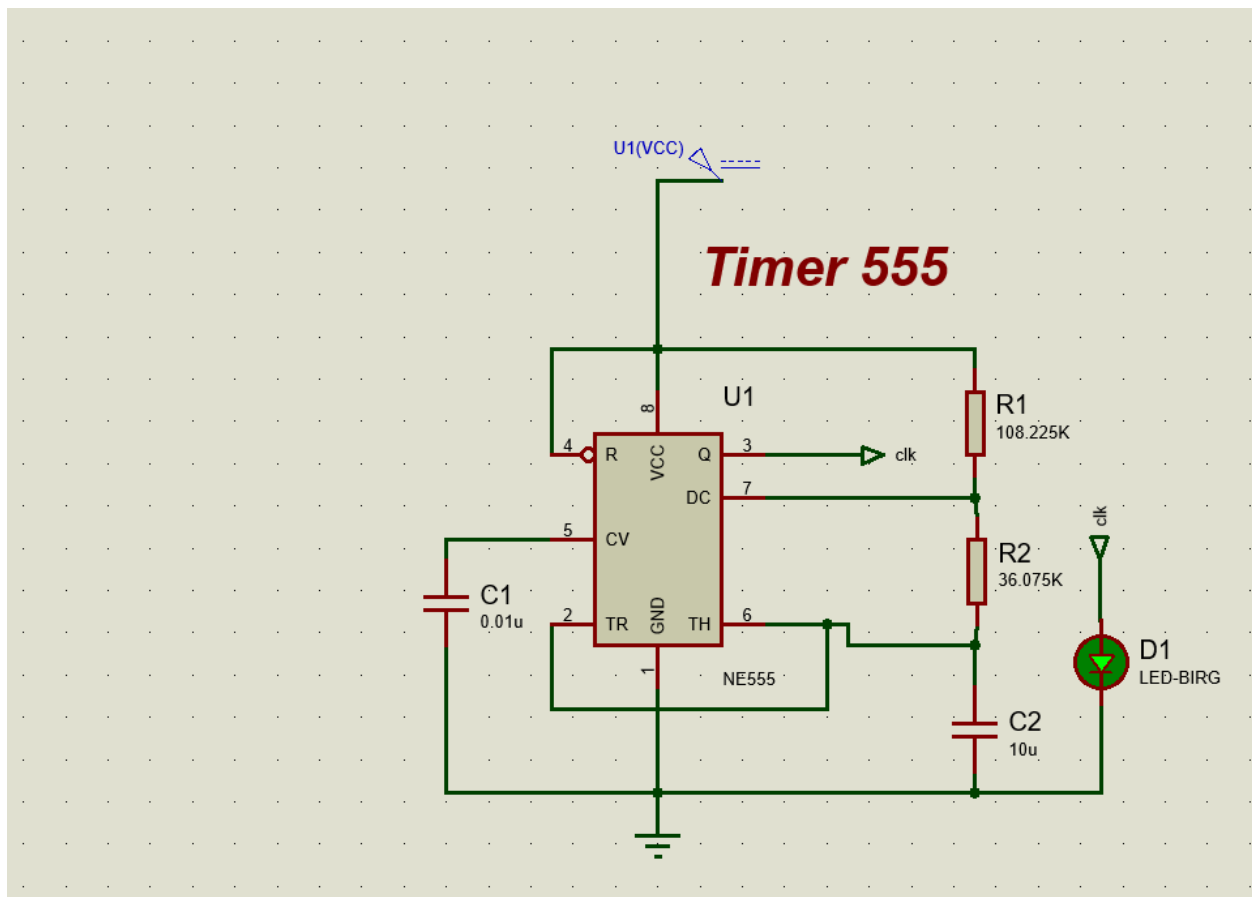
Problem statement: Creating a digital clock with an AM/PM display using logic gates and components involves several essential steps and connections.

Solution:

The clock Have Four things to discuss

1-clock,

- I used Time 555 in a stable mode with the design shown.
- I used $R1=108.225k$ and $R2=36.075$ to ensure that every cycle is 1hz.



2-circuit for count seconds from 0 to 59

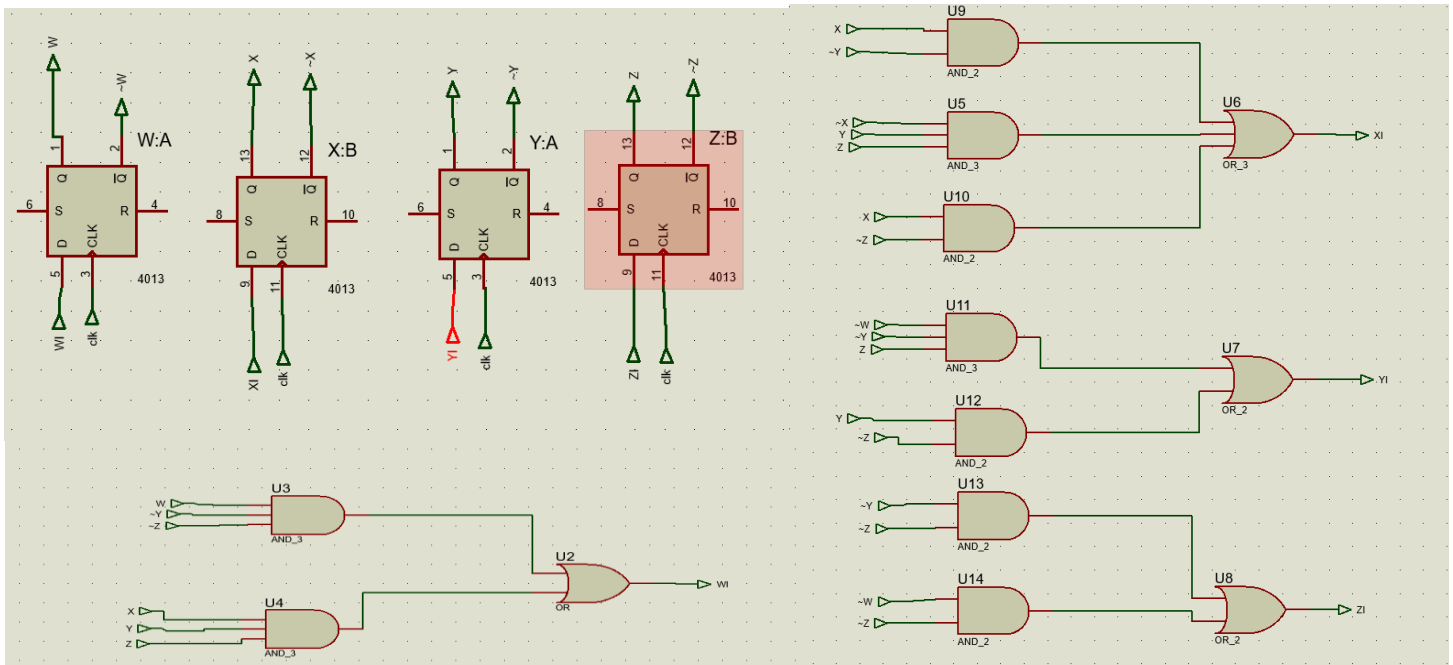
My solution is to make two counters one counting from 0 to 9 and the other count from 0 to 5 with the clock of tens depending on reaching 9 and flipping to zero.

In all counters, I used a D flip-flop

The first one is a counter from 0 to 9 and has the design as shown:

output (WXYZ) W is MSB and Z is LSB

The design is shown in the photo, I concluded the next state equation using the ps-ns table and extracted the equation from the Karno map



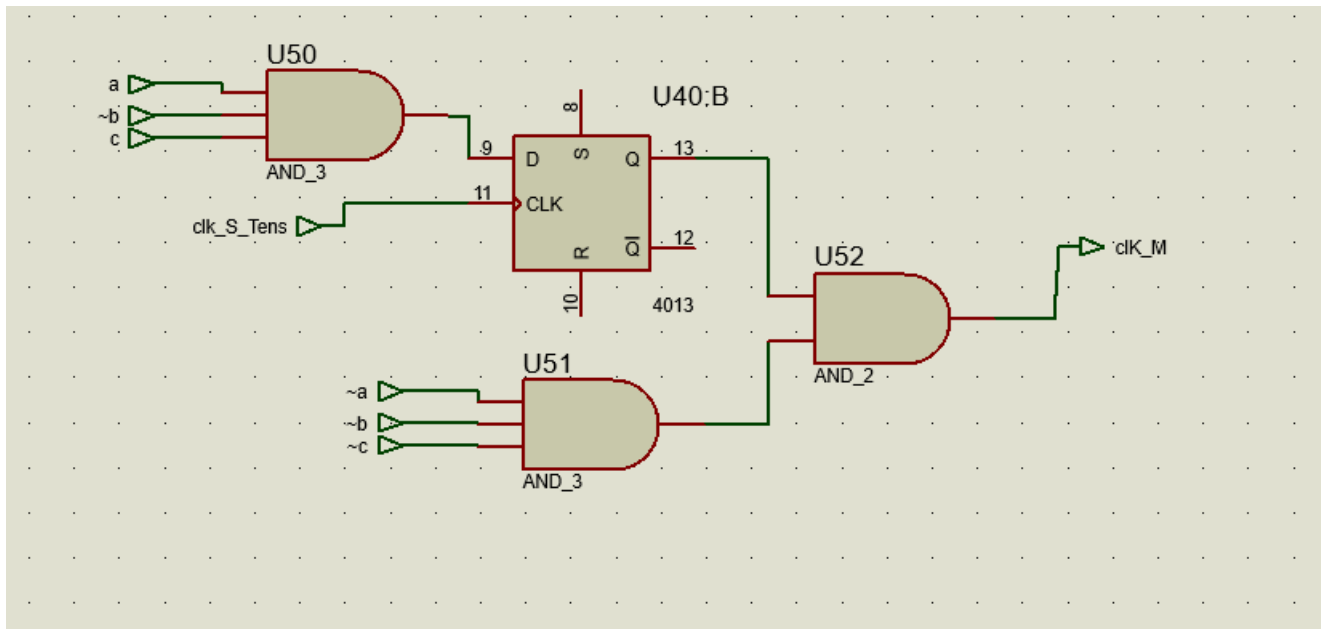
The image shows three circuit diagrams of 4013 dual monostable multivibrators (U15:A, U15:B, U16:A) connected to a 5V supply and ground. Each chip has pins 1, 2, 3, 4, 5, 6, 9, 10, 11, 12, 13, 14, 15, and 16. Pin 1 is connected to 5V, pin 2 to ground, pin 3 to 5V, pin 4 to ground, pin 5 to 5V, pin 6 to ground, pin 9 to 5V, pin 10 to ground, pin 11 to 5V, pin 12 to ground, pin 13 to 5V, pin 14 to ground, pin 15 to 5V, and pin 16 to ground. The output of each chip is connected to a 5V supply and ground.

The top diagram shows the logic for the 'ai' (Adder Input) signal. It consists of two AND gates, U17 and U22, and one OR gate, U20. U17 is an AND gate with inputs 'b' and 'c', and output 'AND_2'. U22 is an AND gate with inputs 'a' and '¬c', and output 'AND_2'. The outputs of U17 and U22 are connected to the inputs of U20, which is an OR gate with output 'OR_2'. The output of U20 is the 'ai' signal.

The bottom diagram shows the logic for the 'bi' (Adder Input) signal. It consists of two AND gates, U19 and U21, and one OR gate, U18. U19 is an AND gate with inputs 'b' and '¬c', and output 'AND_2'. U21 is an AND gate with inputs '¬a', '¬b', and 'c', and output 'AND_3'. The outputs of U19 and U21 are connected to the inputs of U18, which is an OR gate with output 'OR_2'. The output of U18 is the 'bi' signal.

[illegible]

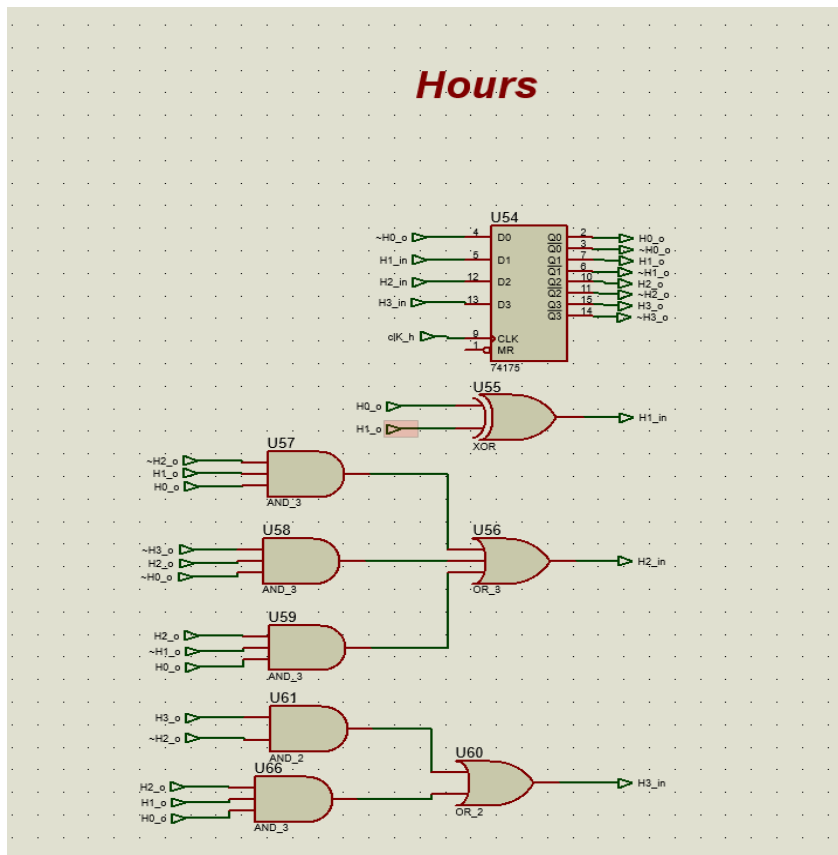
3- minutes: the circuit of minutes is the same as seconds one except the clock enters the minutes it depends on that seconds reach 59 and flip to zero to increase minutes by one as the shown design and tens of minutes clock like seconds but depend on minutes clock not seconds clock.



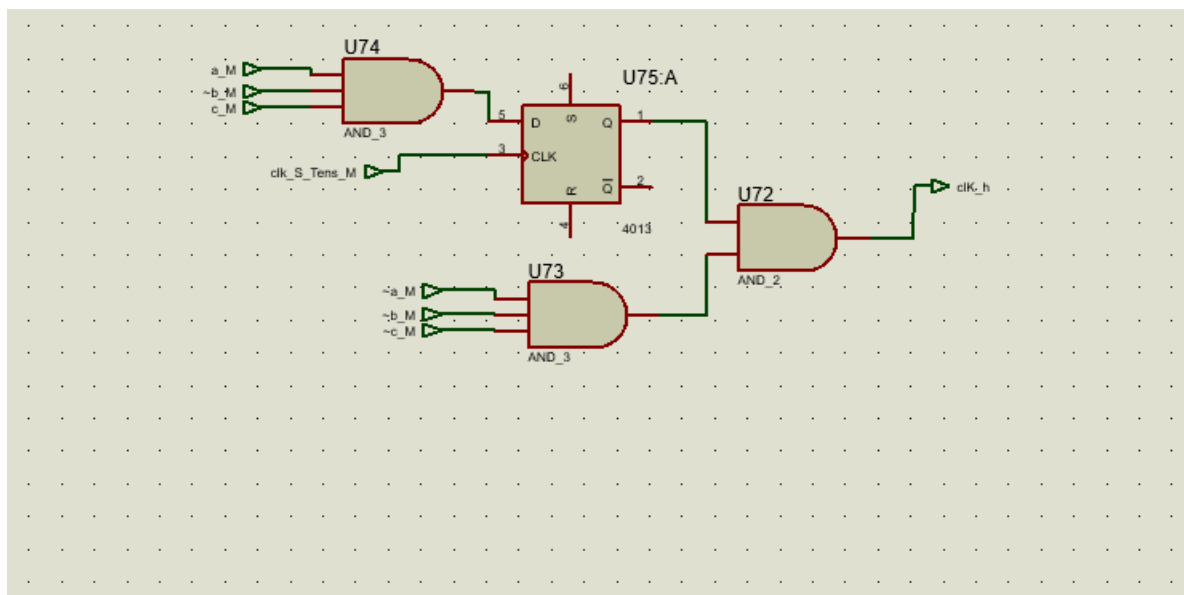
4- hours counter

The design of the hour counter depends on the counter count from 1 to 12 and the 4-bit output goes to the correction circuit to make one the four-bit and tens in one bit to make it easy to show it on two 7segmentst Also there is a circuit to check to flip from AM to PM and vice versa the final output of the circuit is (f5f4f3f2f1f0)

Design of hours counter :

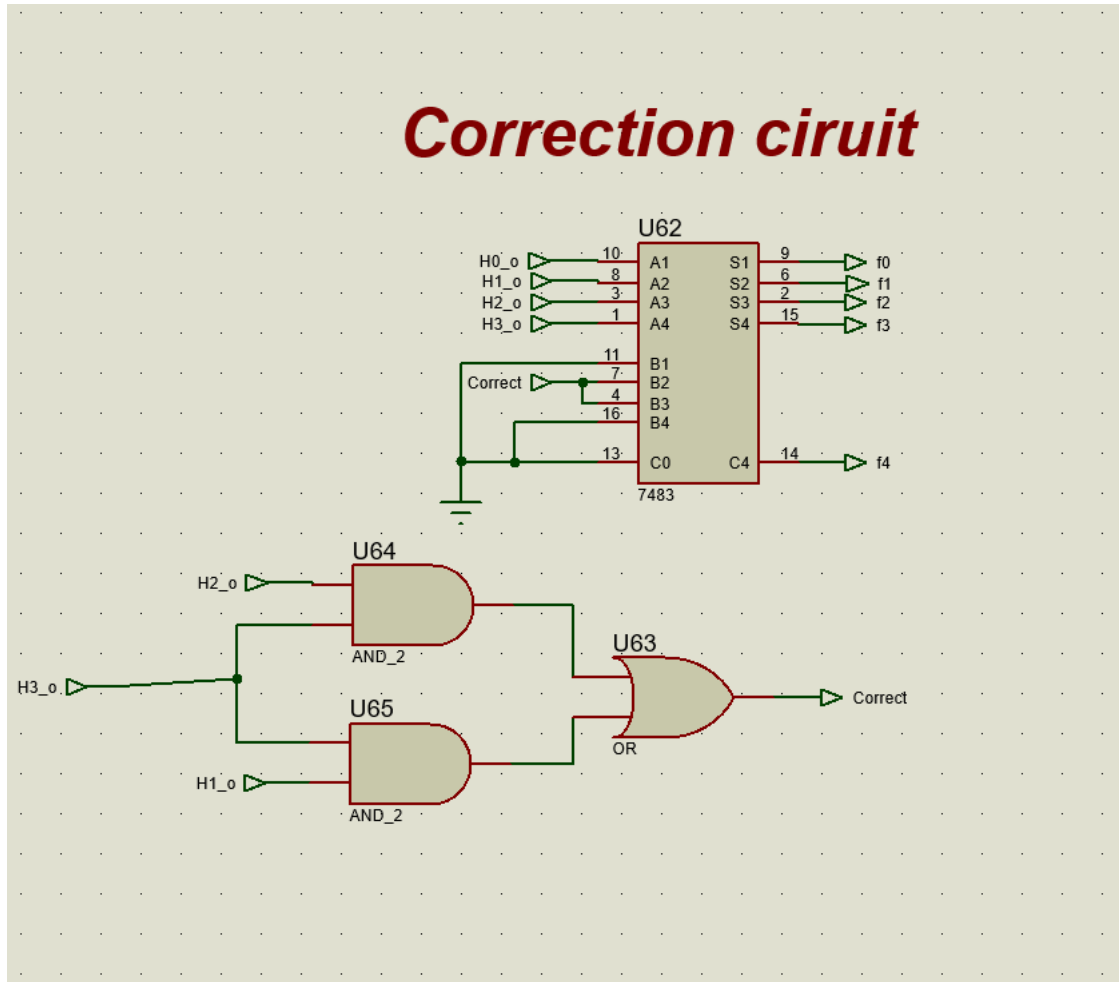


The design of the hours clock depends on the minutes clock :



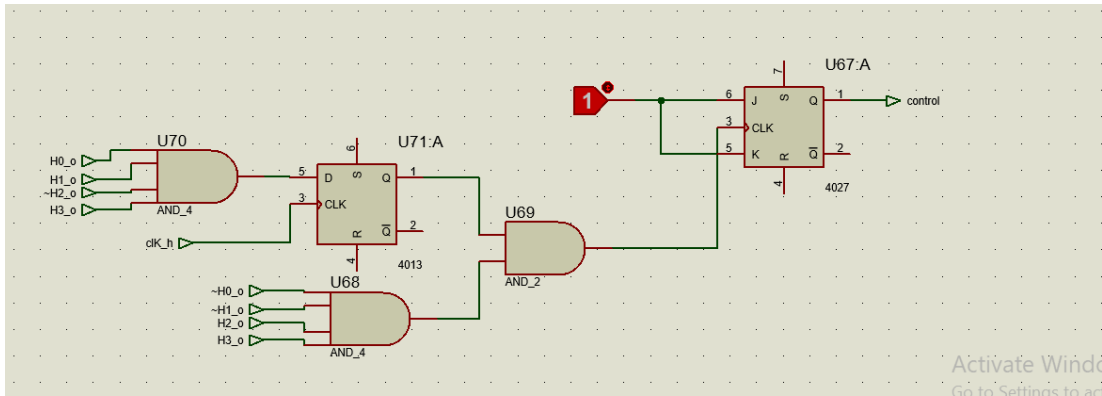
Design of correction circuit:

It depends that check if the number is greater than 9 to add 6 to the original 4-bit and put one in a separate 4 bit and tens in one bit



The final circuit is the circuit used to flip between Am and pm :

The circuit use JKflip flip in toggle situation and make toggle pulse when it comes to it a clock that ensure that hours reach 11:59 and flip to 12 to change between AM and PM



All of the outputs are put to 7-segment display :

