CSE4372/5392 (Spring 2025)
Lab #6

This lab is due by March 28, with a 20% penalty per week day for being late.

In this lab, you will begin to resolve data hazards by forwarding data from the ALU before it is written to the register.

The following steps will guide you through this process:

1. Start with the project from Lab 5. The program you used required 3 NOPs between instructions to prevent data hazards from affecting the correctness of the results.

2. Add these signals to the rv32_id_top port list:

```
// data hazard: df from ex
input       df_ex_enable,
input [4:0]  df_ex_reg,
input [31:0] df_ex_data,

 // data hazard: df from mem
input       df_mem_enable,
input [4:0]  df_mem_reg,
input [31:0] df_mem_data,

// data hazard: df from wb
input       df_wb_enable,
input [4:0]  df_wb_reg,
input [31:0] df_wb_data,
```

3. In the EX, MEM, and WB stages, add un-registered output ports to send the data back to the ID stage. Connect them at the project top.

4. In the ID stage, determine whether or not data forwarding is needed. If data forwarding is needed, make sure that you prioritize which data source to use (from EX, MEM, or WB).

5. Write, assemble, and load a simple assembly language program that writes and reads registers. You should be able to do this without any NOPs between the register operations.

6. Demonstrate operation of the instructions through the pipeline showing the expected register results to the TA. Send your Verilog source .v or .sv files (don't send the entire project) to the TA for credit.