

Министерство образования и науки Российской Федерации
Федеральное государственное бюджетное образовательное учреждение
высшего профессионального образования
«Владимирский государственный университет
имени Александра Григорьевича и Николая Григорьевича Столетовых»
(ВлГУ)

Кафедра «Вычислительная техника»

Лабораторная работа № 3
по дисциплине
«САПР ПЛИС и ИМС»

Выполнил:

ст. гр. ВТм - 112

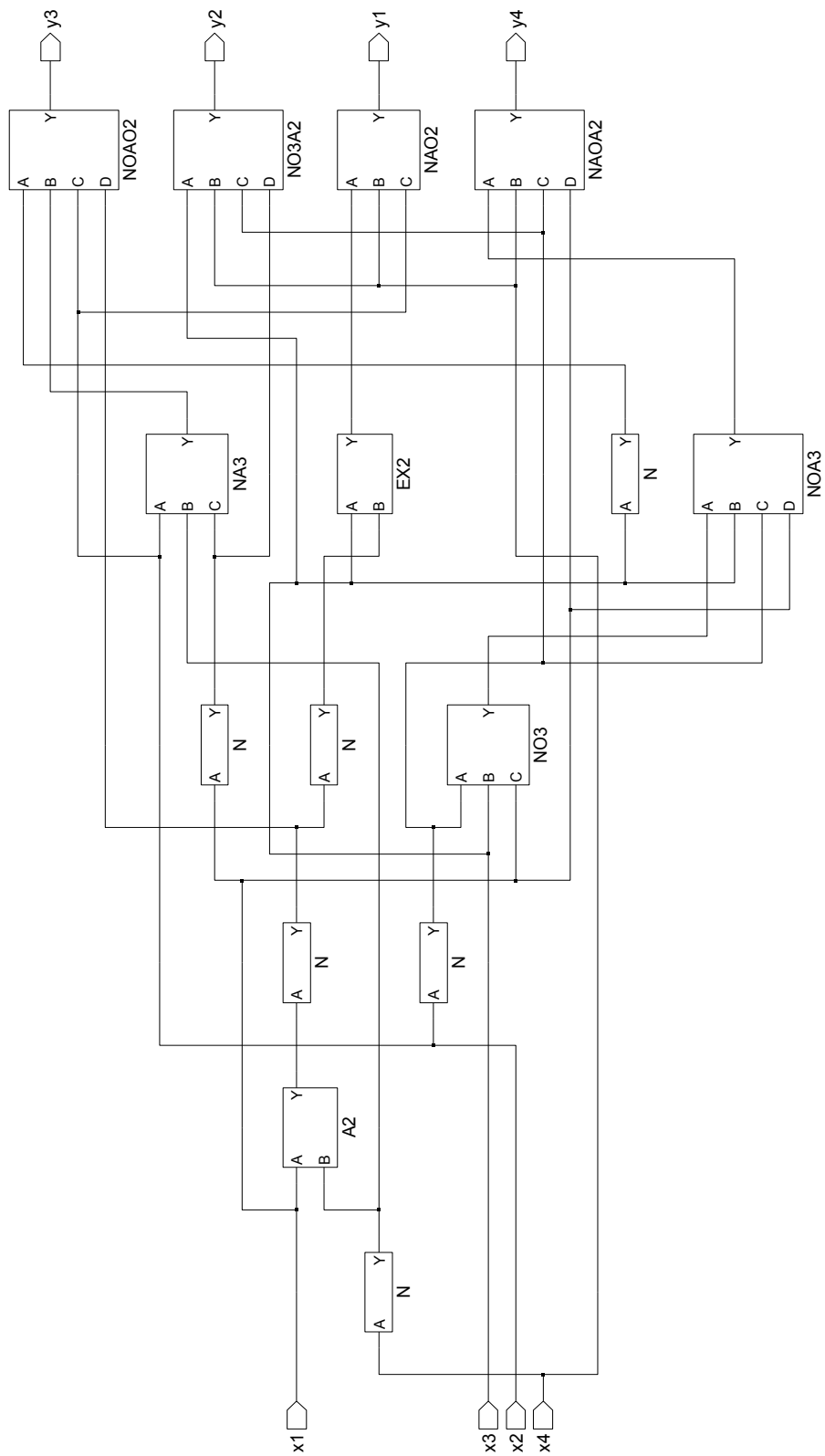
А.Х. Муна

Принял:

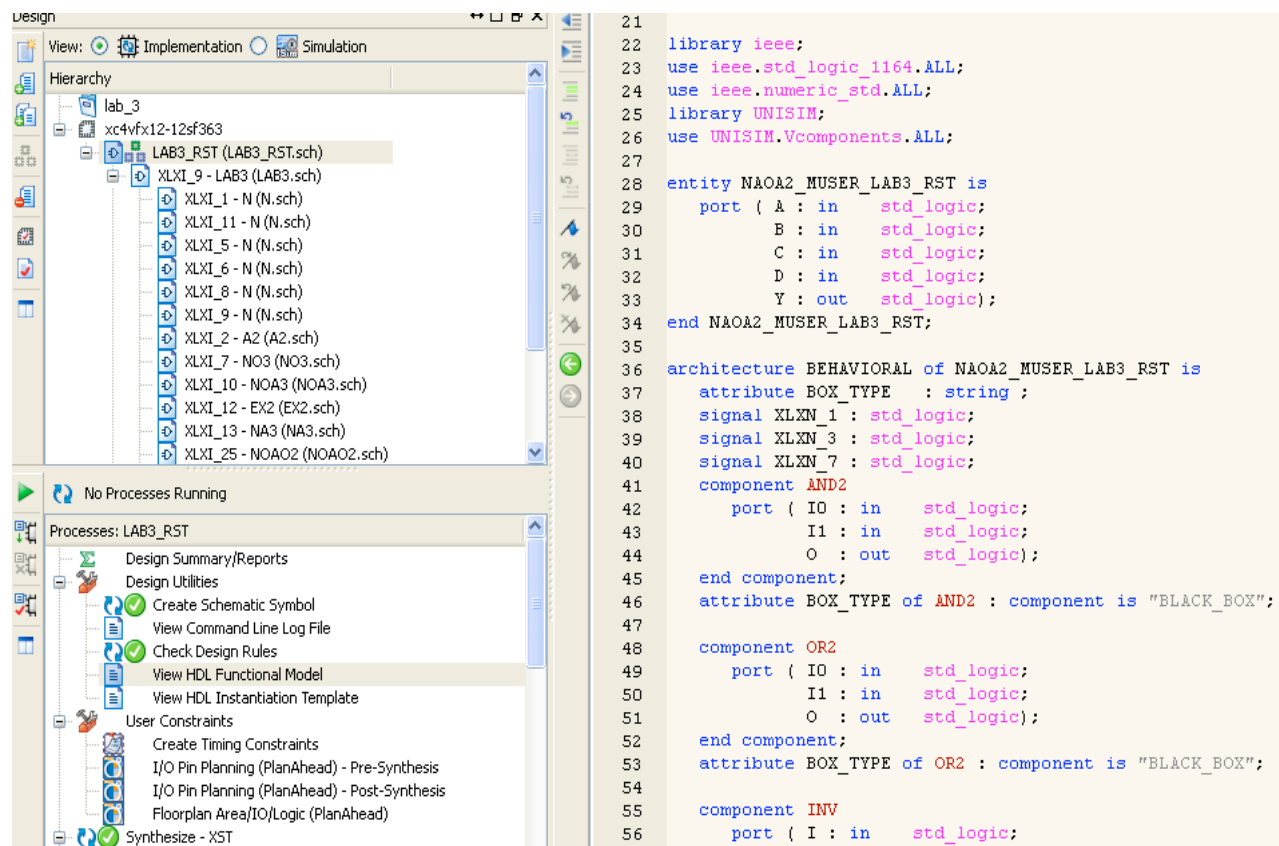
С.С. Гладьо

Владимир 2012

Вариант No. 2



Сгенерированной VHDL файл. (VHDL Functional Model)



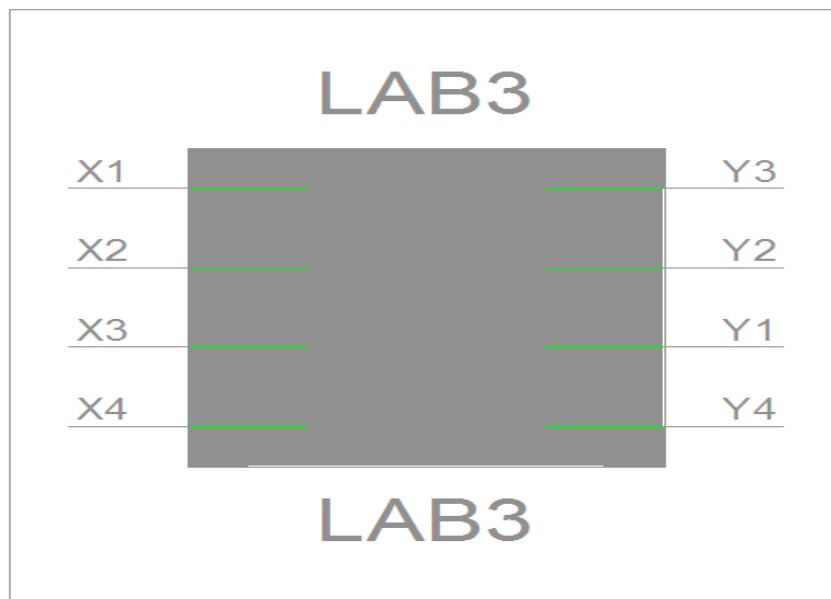
The screenshot displays the Xilinx ISE Design Suite interface. The **Hierarchy** window on the left shows the project structure: **lab_3** contains **xc4vfx12-12sf363**, which contains **LAB3_RST (LAB3_RST.sch)**. This block contains several sub-blocks: **XLXI_9 - LAB3 (LAB3.sch)**, **XLXI_1 - N (N.sch)**, **XLXI_11 - N (N.sch)**, **XLXI_5 - N (N.sch)**, **XLXI_6 - N (N.sch)**, **XLXI_8 - N (N.sch)**, **XLXI_9 - N (N.sch)**, **XLXI_2 - A2 (A2.sch)**, **XLXI_7 - NO3 (NO3.sch)**, **XLXI_10 - NOA3 (NOA3.sch)**, **XLXI_12 - EX2 (EX2.sch)**, **XLXI_13 - NA3 (NA3.sch)**, and **XLXI_25 - NOAO2 (NOAO2.sch)**.

The **Processes: LAB3_RST** window shows the following tasks: **Design Summary/Reports**, **Design Utilities** (Create Schematic Symbol, View Command Line Log File, Check Design Rules, View HDL Functional Model, View HDL Instantiation Template), **User Constraints** (Create Timing Constraints, I/O Pin Planning (PlanAhead) - Pre-Synthesis, I/O Pin Planning (PlanAhead) - Post-Synthesis, Floorplan Area/IO/Logic (PlanAhead)), and **Synthesize - XST**.

The VHDL code on the right is as follows:

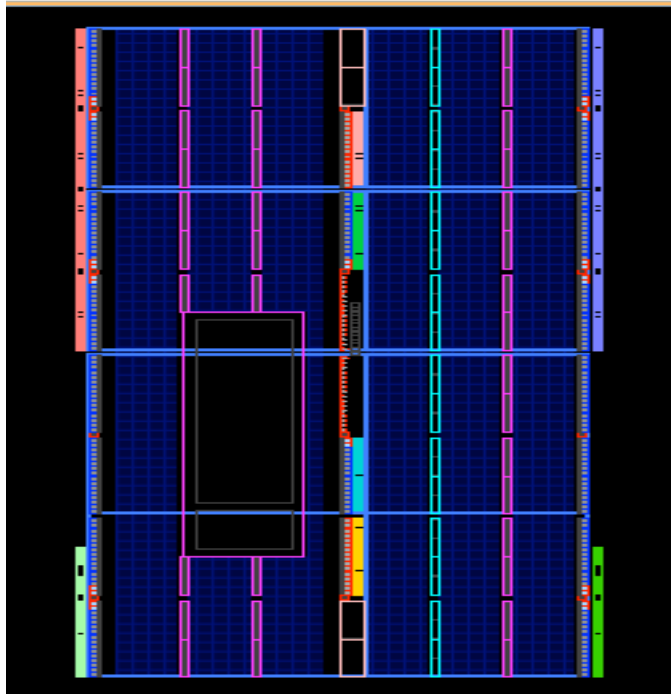
```
21
22 library ieee;
23 use ieee.std_logic_1164.ALL;
24 use ieee.numeric_std.ALL;
25 library UNISIM;
26 use UNISIM.Vcomponents.ALL;
27
28 entity NAOA2_MUSER_LAB3_RST is
29     port ( A : in     std_logic;
30           B : in     std_logic;
31           C : in     std_logic;
32           D : in     std_logic;
33           Y : out    std_logic);
34 end NAOA2_MUSER_LAB3_RST;
35
36 architecture BEHAVIORAL of NAOA2_MUSER_LAB3_RST is
37     attribute BOX_TYPE : string ;
38     signal XLXN_1 : std_logic;
39     signal XLXN_3 : std_logic;
40     signal XLXN_7 : std_logic;
41     component AND2
42     port ( IO : in     std_logic;
43           I1 : in     std_logic;
44           O : out    std_logic);
45 end component;
46     attribute BOX_TYPE of AND2 : component is "BLACK_BOX";
47
48     component OR2
49     port ( IO : in     std_logic;
50           I1 : in     std_logic;
51           O : out    std_logic);
52 end component;
53     attribute BOX_TYPE of OR2 : component is "BLACK_BOX";
54
55     component INV
56     port ( I : in     std_logic;
```

Lab3:



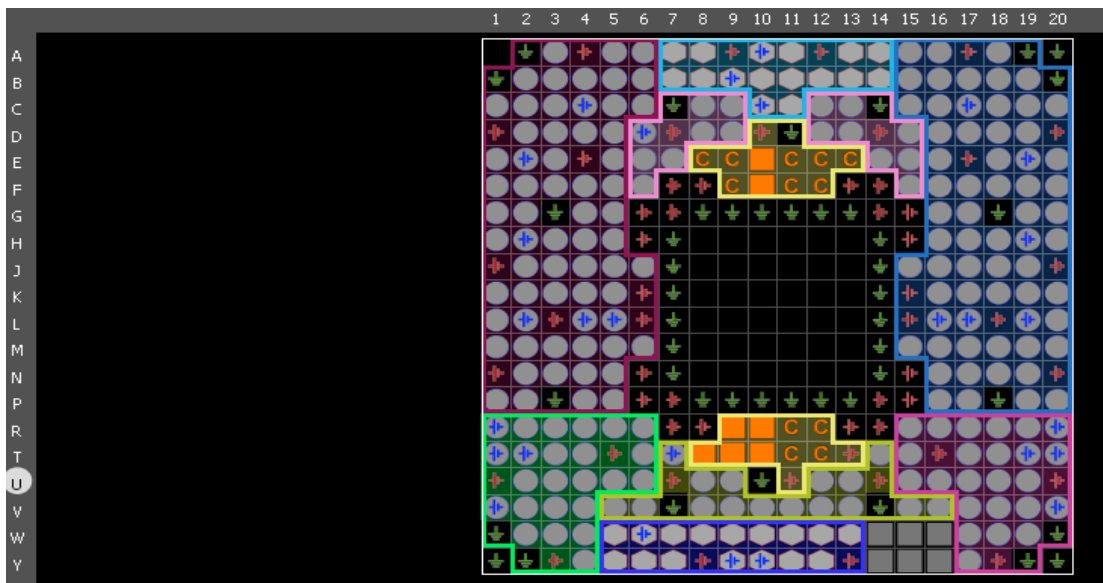
Без RST

I/O Pin planning Pre-Synthesis Device



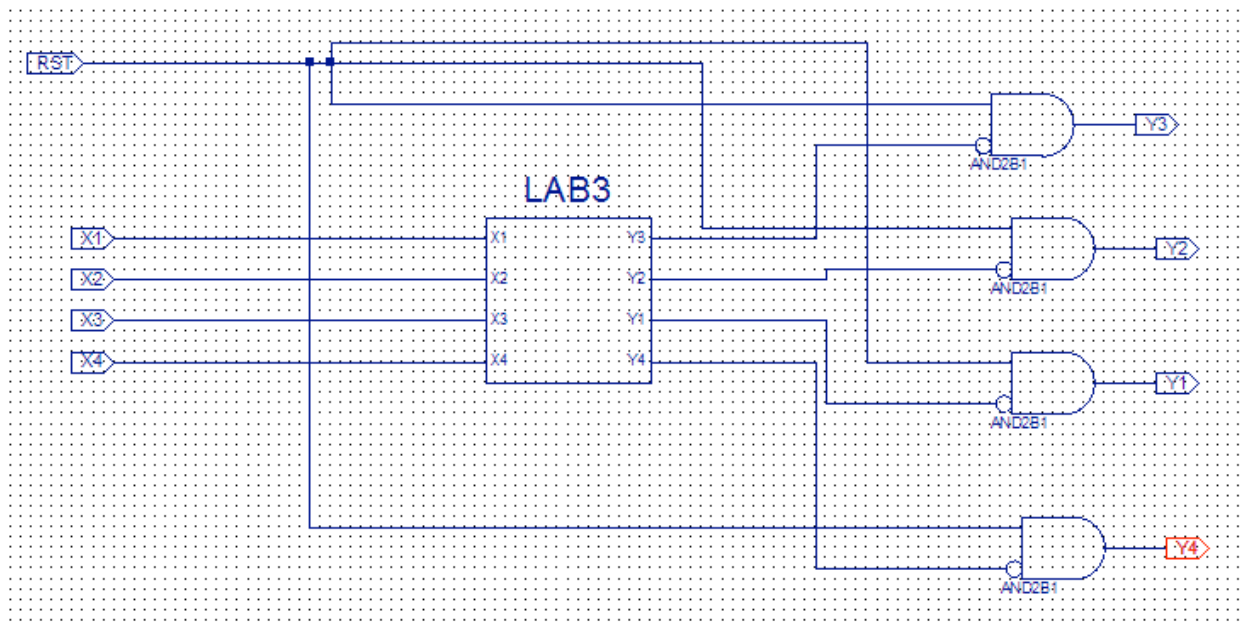
I/O pin planning Pre-Synthesis

Package:

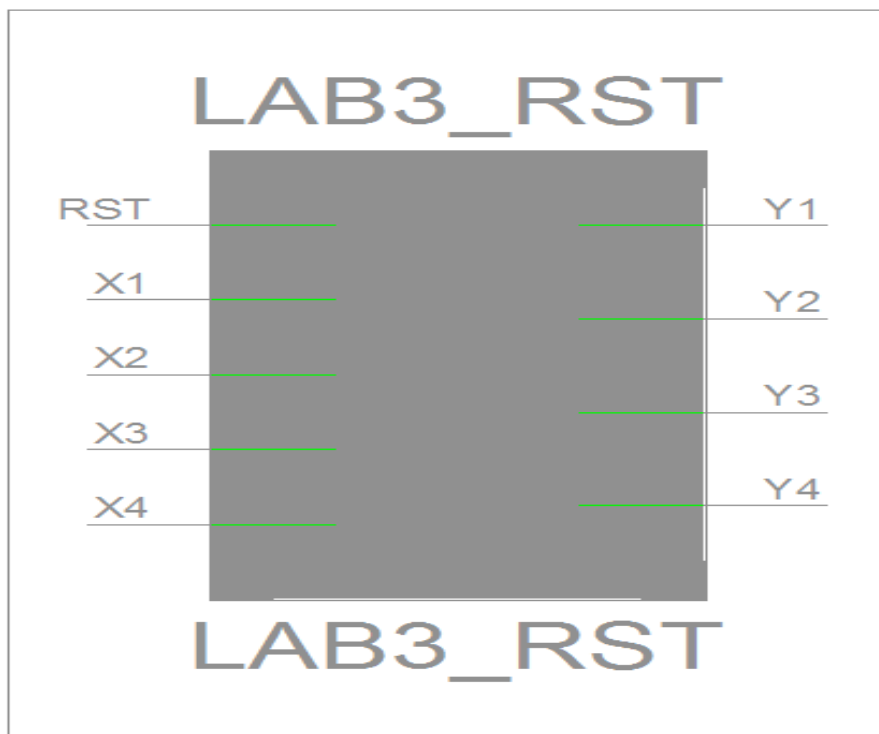


RTL Schematic:

Схема с RST



Lab3: c RST



файл портов схема к реальным портам

Implementation Simulation

archy

LAB3_RST (LAB3_RST.sch)

XLXI_9 - LAB3 (LAB3.sch)

XLXI_1 - N (N.sch)

XLXI_11 - N (N.sch)

XLXI_5 - N (N.sch)

XLXI_6 - N (N.sch)

XLXI_8 - N (N.sch)

XLXI_9 - N (N.sch)

XLXI_2 - A2 (A2.sch)

XLXI_7 - NO3 (NO3.sch)

XLXI_10 - NOA3 (NOA3.sch)

XLXI_12 - EX2 (EX2.sch)

XLXI_13 - NA3 (NA3.sch)

XLXI_25 - NOAO2 (NOAO2.sch)

XLXI_26 - NO3A2 (NO3A2.sch)

XLXI_27 - NAO2 (NAO2.sch)

```

1 NET "X1" LOC = "C5";
2 NET "X2" LOC = "B5";
3 NET "X3" LOC = "A5";
4 NET "X4" LOC = "C6";
5 NET "RST" LOC = "D5";
6 NET "Y1" LOC = "A6";
7 NET "Y2" LOC = "C4";
8 NET "Y3" LOC = "B4";
9 NET "Y4" LOC = "B6";

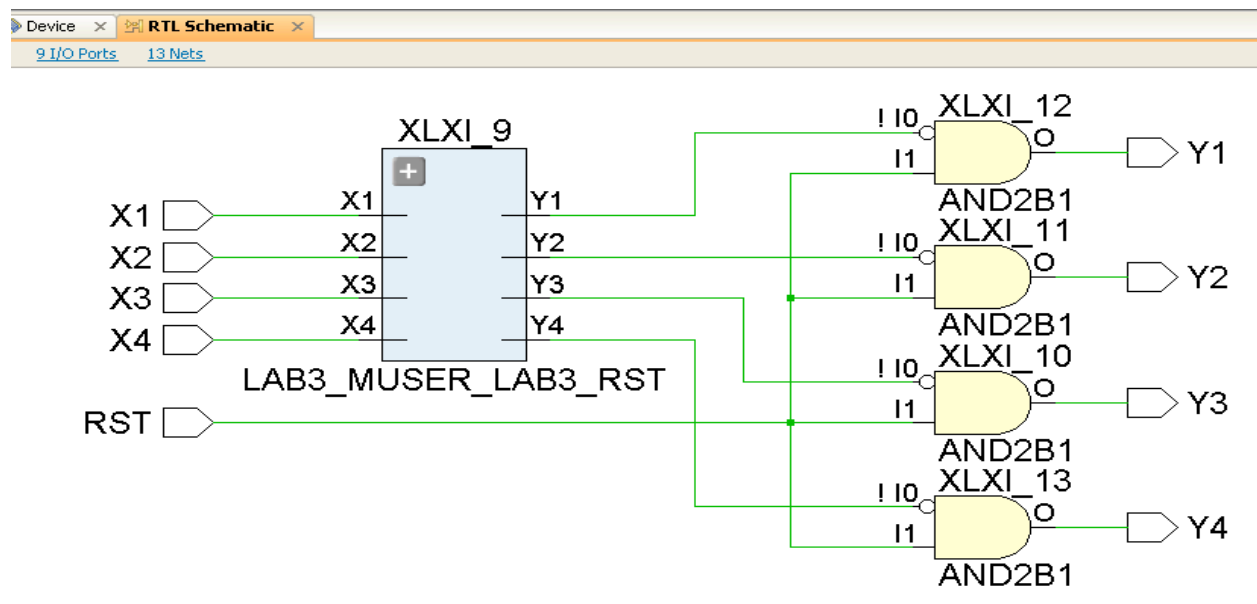
```

I/O Ports

Name	Direction	Neg Diff Pair	Site	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type
All ports (9)											
Scalar ports (9)											
RST	Input		D5	<input checked="" type="checkbox"/>	6	default (LVCMOS25)	2.5		12 SLOW	NONE	
X1	Input		C5	<input checked="" type="checkbox"/>	6	default (LVCMOS25)	2.5		12 SLOW	NONE	
X2	Input		B5	<input checked="" type="checkbox"/>	6	default (LVCMOS25)	2.5		12 SLOW	NONE	
X3	Input		A5	<input checked="" type="checkbox"/>	6	default (LVCMOS25)	2.5		12 SLOW	NONE	
X4	Input		C6	<input checked="" type="checkbox"/>	6	default (LVCMOS25)	2.5		12 SLOW	NONE	
Y1	Output		A6	<input checked="" type="checkbox"/>	6	default (LVCMOS25)	2.5		12 SLOW	NONE	
Y2	Output		C4	<input checked="" type="checkbox"/>	6	default (LVCMOS25)	2.5		12 SLOW	NONE	
Y3	Output		B4	<input checked="" type="checkbox"/>	6	default (LVCMOS25)	2.5		12 SLOW	NONE	
Y4	Output		B6	<input checked="" type="checkbox"/>	6	default (LVCMOS25)	2.5		12 SLOW	NONE	

Tcl Console Package Pins I/O Ports

Реальный устройства с портами





VHDL Шаблон

ab_3
c4vfx12-12sf363

LAB3_RST (LAB3_RST.sch)

XLXI_9 - LAB3 (LAB3.sch)

XLXI_1 - N (N.sch)

XLXI_11 - N (N.sch)

XLXI_5 - N (N.sch)

XLXI_6 - N (N.sch)

XLXI_8 - N (N.sch)

XLXI_9 - N (N.sch)

XLXI_2 - A2 (A2.sch)

XLXI_7 - NO3 (NO3.sch)

XLXI_10 - NOA3 (NOA3.sch)

XLXI_12 - EX2 (EX2.sch)

XLXI_13 - NA3 (NA3.sch)

XLXI_25 - NOAO2 (NOAO2.sch)

Processes Running

s: LAB3_RST

Design Summary/Reports

Design Utilities

Create Schematic Symbol

View Command Line Log File

Check Design Rules

View HDL Functional Model

View HDL Instantiation Template

User Constraints

Create Timing Constraints

```

3  -- Notes:
4  -- 1) This instantiation template has been
5  -- std_logic and std_logic_vector for the
6  -- 2) To use this template to instantiate
7  --
8
9  COMPONENT LAB3_RST
10 PORT ( RST : IN STD_LOGIC;
11        X1  : IN STD_LOGIC;
12        X2  : IN STD_LOGIC;
13        X3  : IN STD_LOGIC;
14        X4  : IN STD_LOGIC;
15        Y3  : OUT STD_LOGIC;
16        Y2  : OUT STD_LOGIC;
17        Y1  : OUT STD_LOGIC;
18        Y4  : OUT STD_LOGIC);
19
20 END COMPONENT;
21
22 UUT: LAB3_RST PORT MAP (
23     RST => ,
24     X1  => ,
25     X2  => ,
26     X3  => ,
27     X4  => ,
28     Y3  => ,
29     Y2  => ,
30     Y1  => ,
31     Y4  =>
32 );

```


Simulation:



Таблица Истинности:

X1	X2	X3	X4	Y1	Y2	Y3	Y4
0	0	0	0	1	0	0	1
0	0	0	1	1	0	0	0
0	0	1	0	1	0	0	1
0	0	1	1	0	0	0	0
0	1	0	0	1	1	0	1
0	1	0	1	1	0	0	1
0	1	1	0	0	0	1	1
0	1	1	1	0	0	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	0	0	0
1	0	1	0	1	0	1	1
1	0	1	1	0	0	0	1
1	1	0	0	0	1	0	1
1	1	0	1	1	0	0	0
1	1	1	0	1	0	0	1
1	1	1	1	0	0	0	0

TestBench Code:

```
LIBRARY ieee;

USE ieee.std_logic_1164.ALL;

USE ieee.numeric_std.ALL;

LIBRARY UNISIM;

USE UNISIM.Vcomponents.ALL;

ENTITY LAB3_LAB3_sch_tb IS

END LAB3_LAB3_sch_tb;

ARCHITECTURE behavioral OF LAB3_LAB3_sch_tb IS


    COMPONENT LAB3

    PORT ( X1      :    IN    STD_LOGIC;

           X2      :    IN    STD_LOGIC;

           X3      :    IN    STD_LOGIC;

           X4      :    IN    STD_LOGIC;

           Y3      :    OUT   STD_LOGIC;

           Y2      :    OUT   STD_LOGIC;

           Y1      :    OUT   STD_LOGIC;

           Y4      :    OUT   STD_LOGIC);

    END COMPONENT;


    SIGNAL X1      :    STD_LOGIC;

    SIGNAL X2      :    STD_LOGIC;

    SIGNAL X3      :    STD_LOGIC;

    SIGNAL X4      :    STD_LOGIC;

    SIGNAL Y3      :    STD_LOGIC;
```

```
SIGNAL Y2      :      STD_LOGIC;

SIGNAL Y1      :      STD_LOGIC;

SIGNAL Y4      :      STD_LOGIC;
```

```
BEGIN
```

```
UUT: LAB3 PORT MAP(
```

```
    X1 => X1,
```

```
    X2 => X2,
```

```
    X3 => X3,
```

```
    X4 => X4,
```

```
    Y3 => Y3,
```

```
    Y2 => Y2,
```

```
    Y1 => Y1,
```

```
    Y4 => Y4
```

```
);
```

```
proces_x1 : PROCESS
```

```
    constant period :time := 20 ns;
```

```
BEGIN
```

```
    X1 <= '0';
```

```
        wait for period;
```

```
    X1 <='1';
```

```
        wait for period;
```

```
END PROCESS;
```

```
proces_x2 : PROCESS
```

```
    constant period :time := 40 ns;
```

```

begin
    X2 <= '0';

    WAIT for period; -- will wait forever

    X2 <='1';

    wait for period;

END PROCESS;

proces_x3 : PROCESS

    constant period :time := 80 ns;

begin

    X3 <= '0';

    WAIT for period; -- will wait forever

    X3 <='1';

    wait for period;

END PROCESS;

proces_x4 : PROCESS

    constant period :time := 160 ns;

BEGIN

    X4 <= '0';

    WAIT for period; -- will wait forever

    X4 <='1';

    wait for period;

END PROCESS;

-- *** End Test Bench - User Defined Section ***

END;
```

Вывод:

В заданном лабораторной был изучен как реализовать FPGA module в среде Xilinx.