Министерство образования и науки Российской Федерации

Федеральное государственное бюджетное образовательное учреждение

высшего профессионального образования

«Владимирский государственный университет

имени Александра Григорьевича и Николая Григорьевича Столетовых»

(ВлГУ)

Кафедра «Вычислительная техника»

Лабораторная работа № 3

по дисциплине

«САПР ПЛИС и ИМС»

Выполнил:

ст. гр. ВТм - 112

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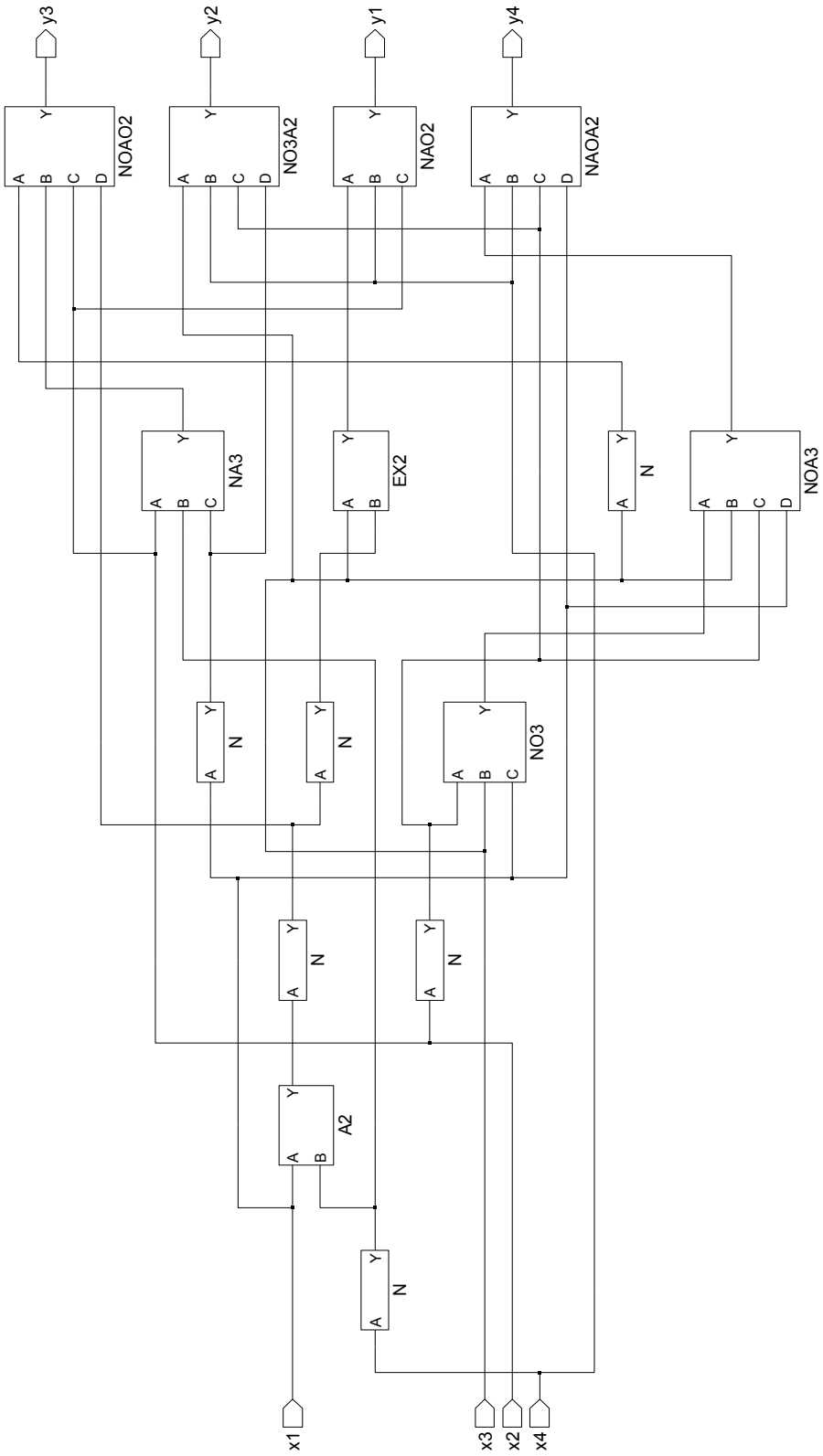
Принял:

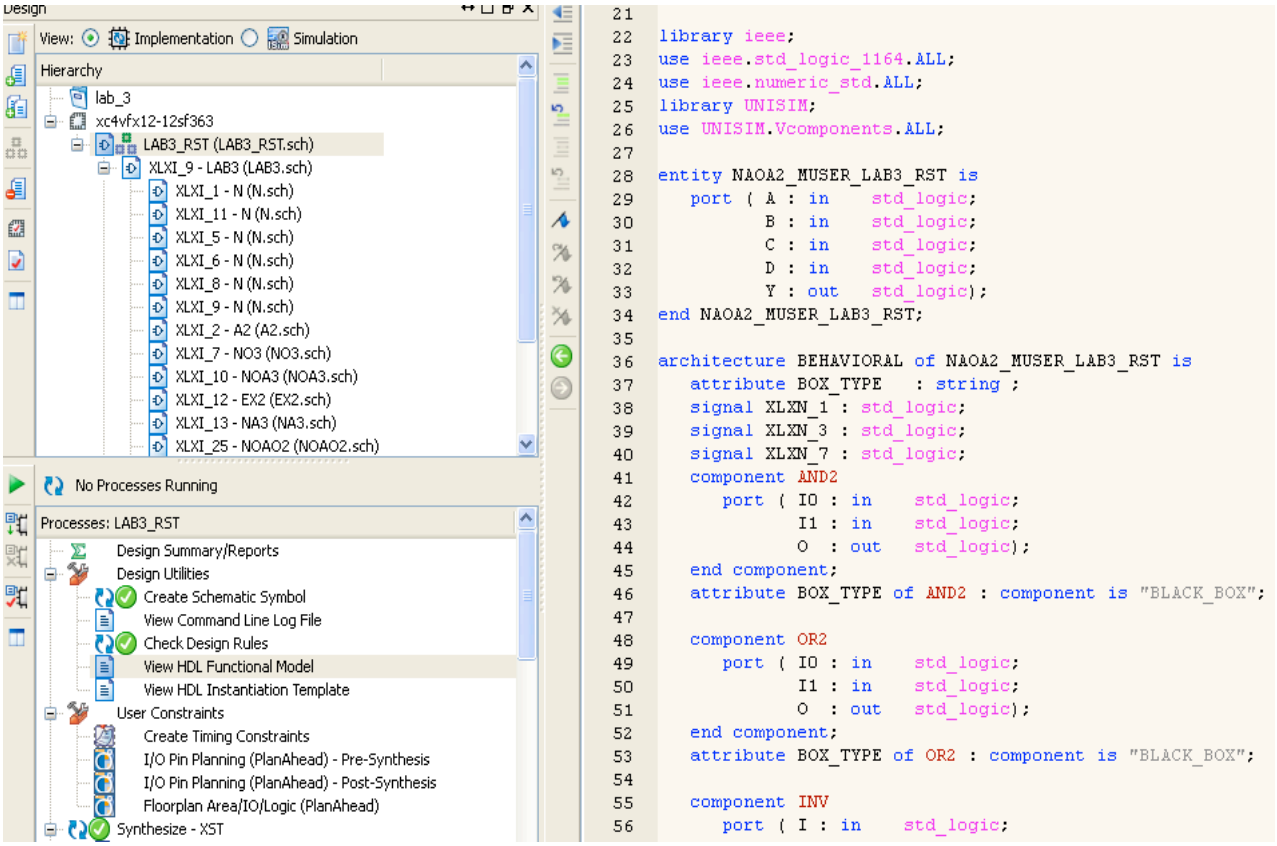
С.С. Гладьо

Владимир 2012

Вариант No. 2

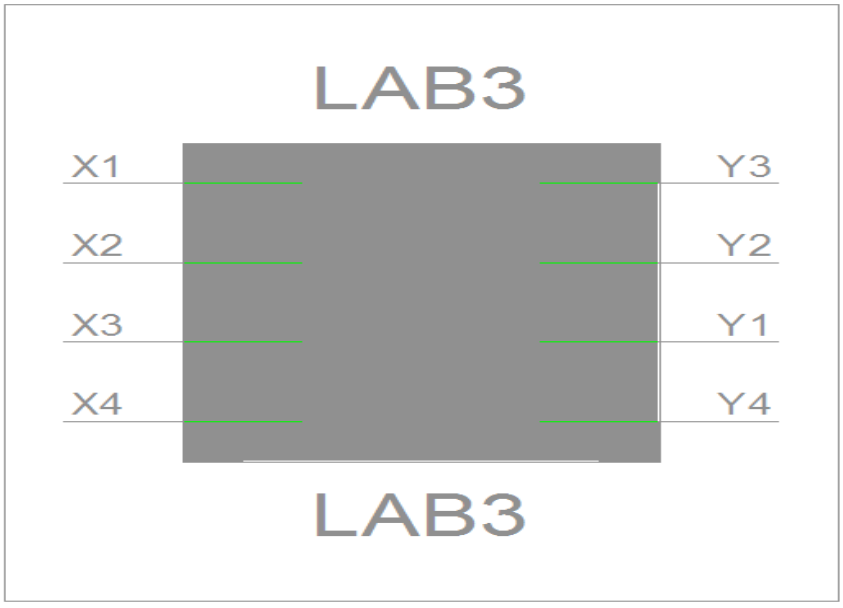

y3
y2
y1
y4
NOAO2
NO3A2
NAO2
NAOA2
NA3
EX2
N
NOA3
N
N
NO3
N
N
A2
N
x1
x3
x2
x4

Сгенерированной VHDL файл. (VHDL Functional Model)



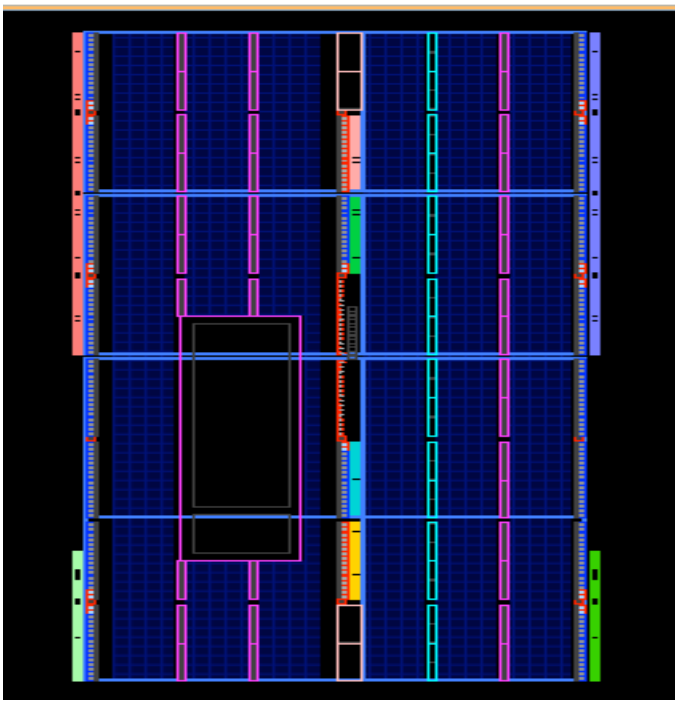

```
21
22  library ieee;
23  use ieee.std_logic_1164.ALL;
24  use ieee.numeric_std.ALL;
25  library UNISIM;
26  use UNISIM.Vcomponents.ALL;
27
28  entity NAOA2_MUSER_LAB3_RST is
29     port ( A : in    std_logic;
30            B : in    std_logic;
31            C : in    std_logic;
32            D : in    std_logic;
33            Y : out   std_logic);
34  end NAOA2_MUSER_LAB3_RST;
35
36  architecture BEHAVIORAL of NAOA2_MUSER_LAB3_RST is
37     attribute BOX_TYPE   : string ;
38     signal XLXN_1 : std_logic;
39     signal XLXN_3 : std_logic;
40     signal XLXN_7 : std_logic;
41     component AND2
42        port ( IO : in    std_logic;
43               I1 : in    std_logic;
44               O  : out   std_logic);
45     end component;
46     attribute BOX_TYPE of AND2 : component is "BLACK_BOX";
47
48     component OR2
49        port ( IO : in    std_logic;
50               I1 : in    std_logic;
51               O  : out   std_logic);
52     end component;
53     attribute BOX_TYPE of OR2 : component is "BLACK_BOX";
54
55     component INV
56        port ( I : in    std_logic;
```

Lab3:



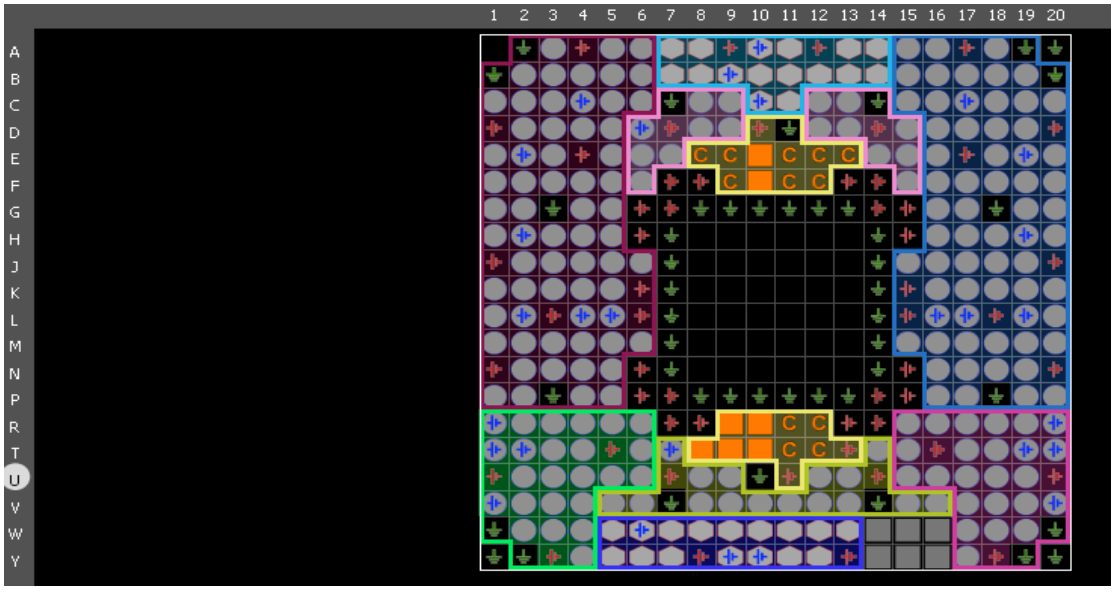
Без RST

I/O Pin planning Pre-Synthesis Device

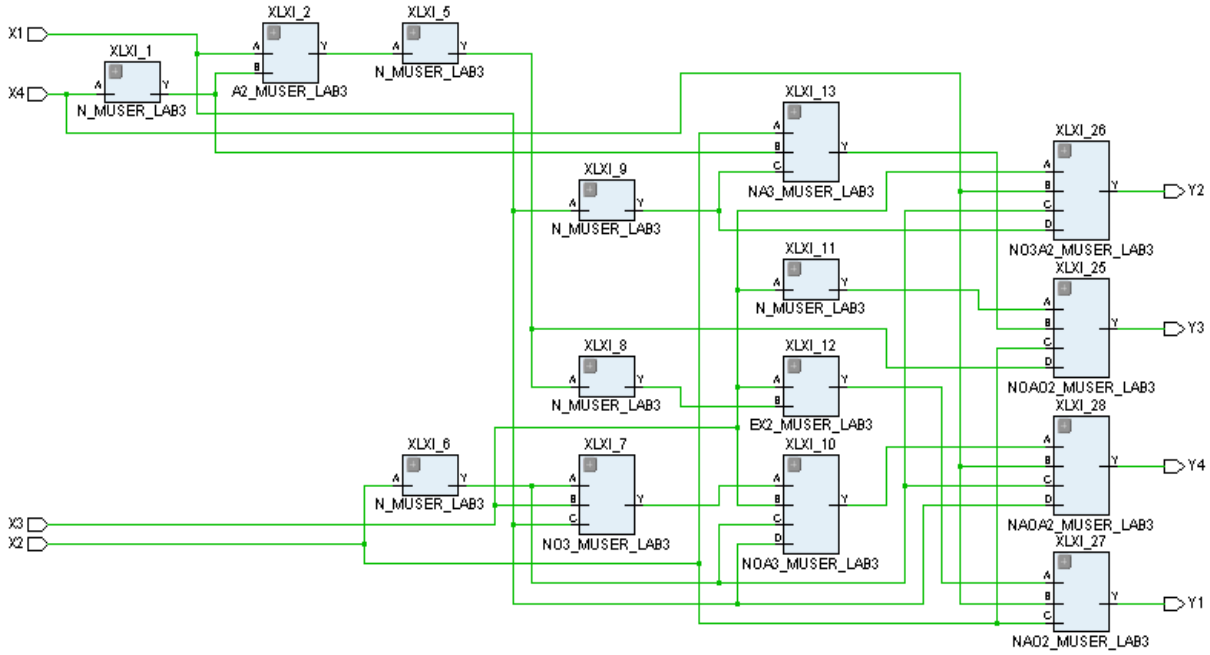


I/O pin planning Pre-Synthesis

Package:



RTL Schematic:



Schematic Post synthesis:

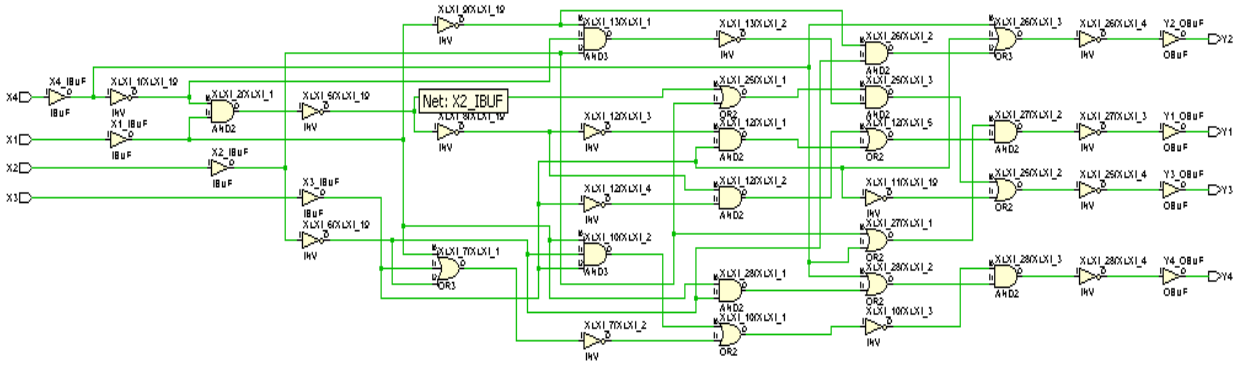
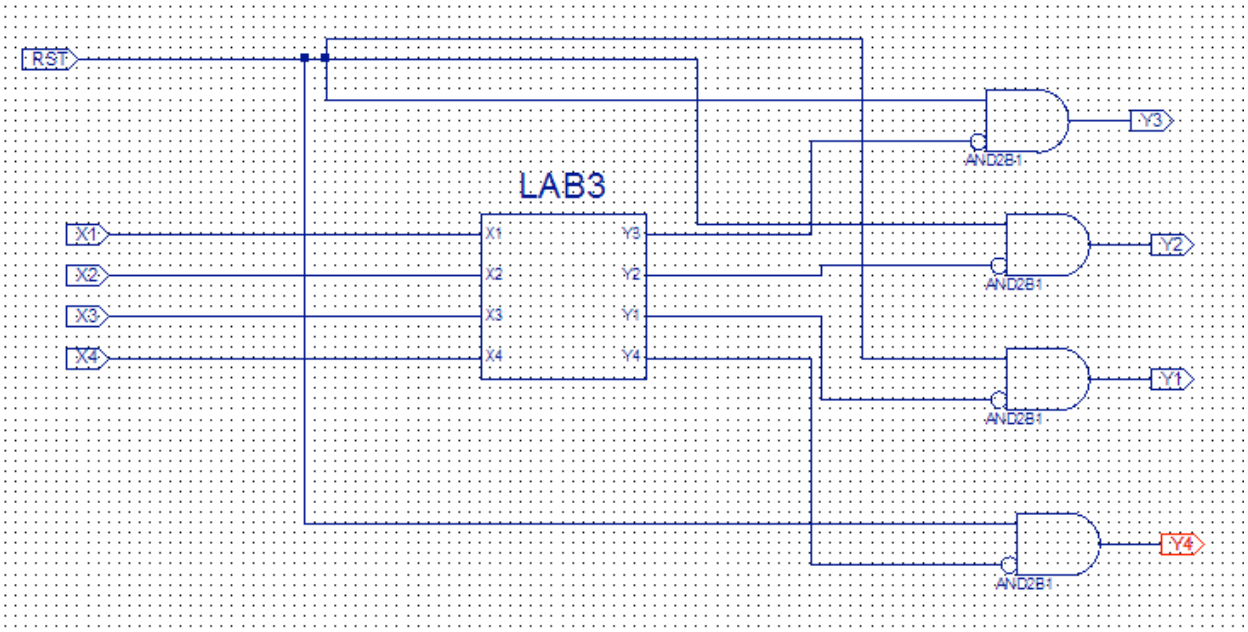
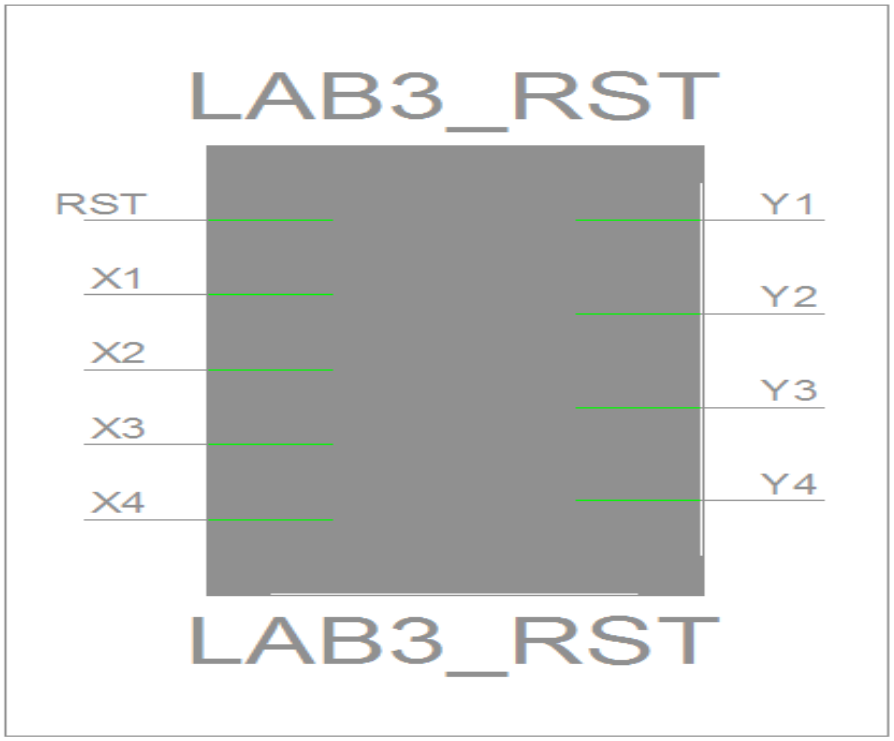


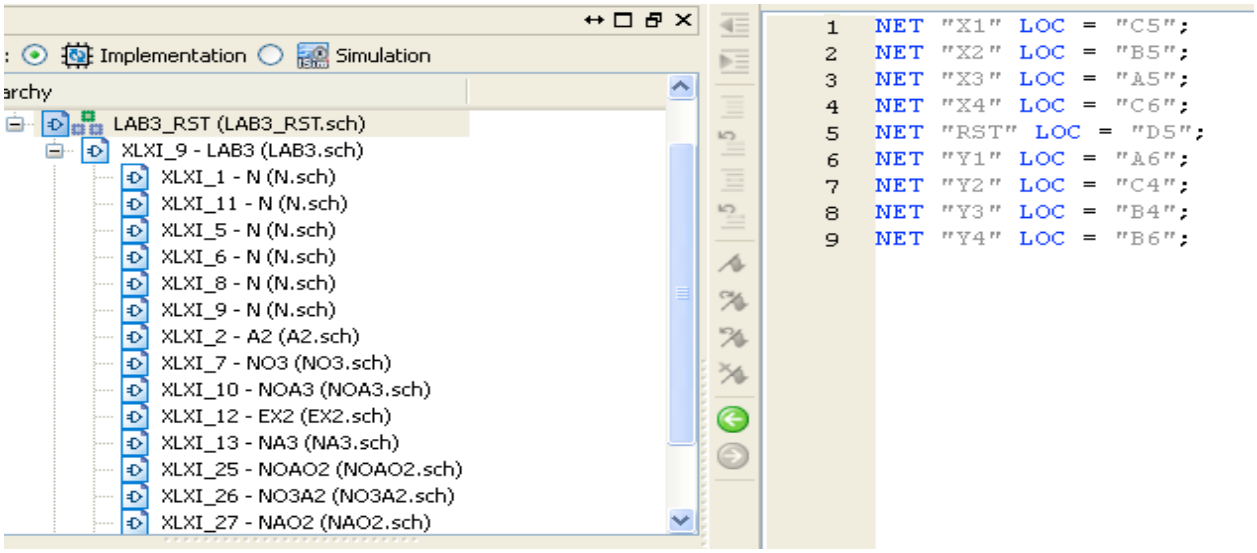
Схема с RST

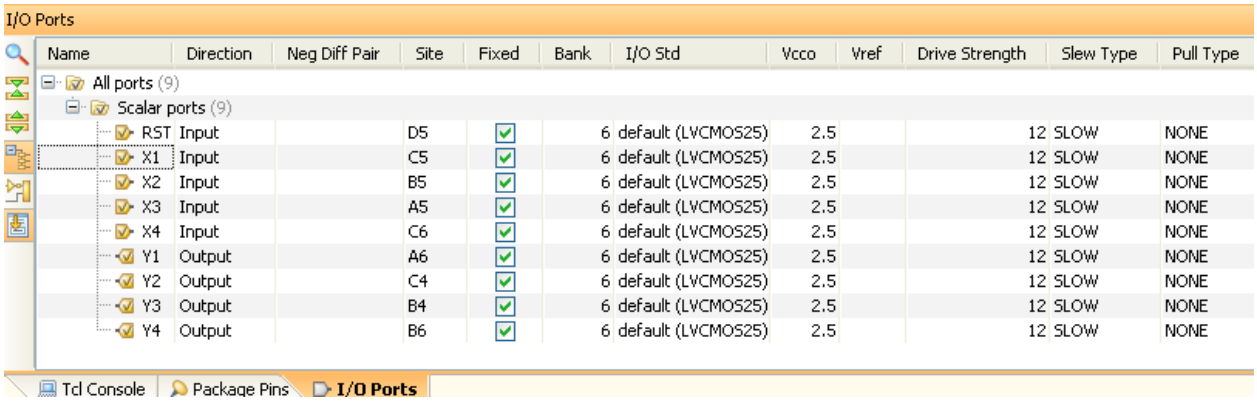


Lab3: с RST

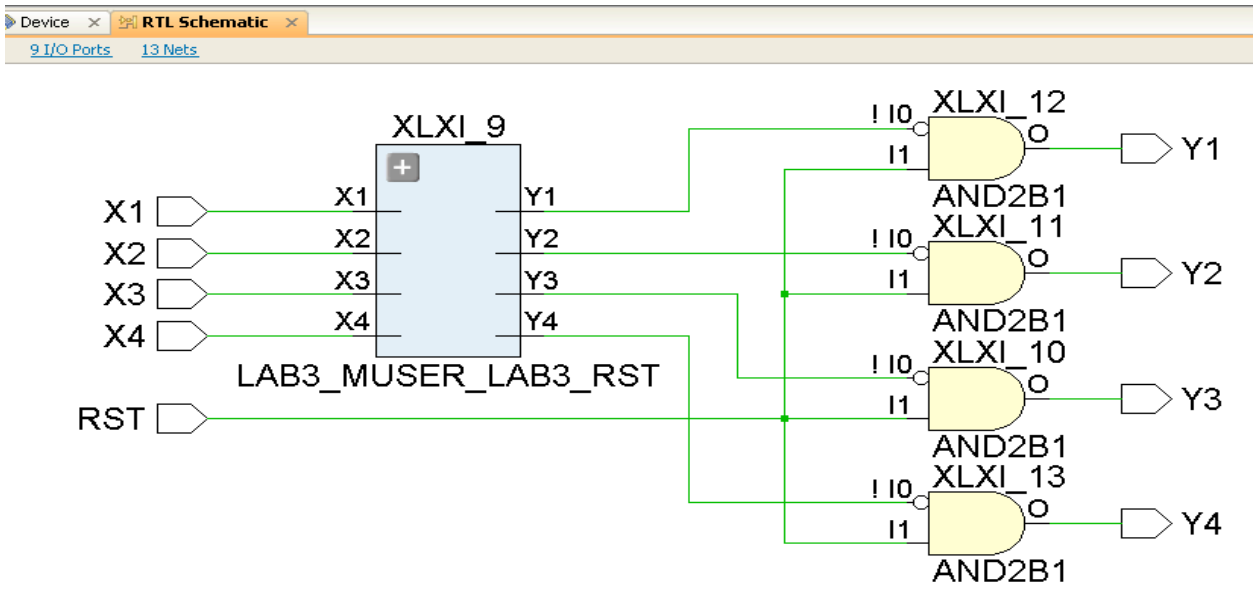


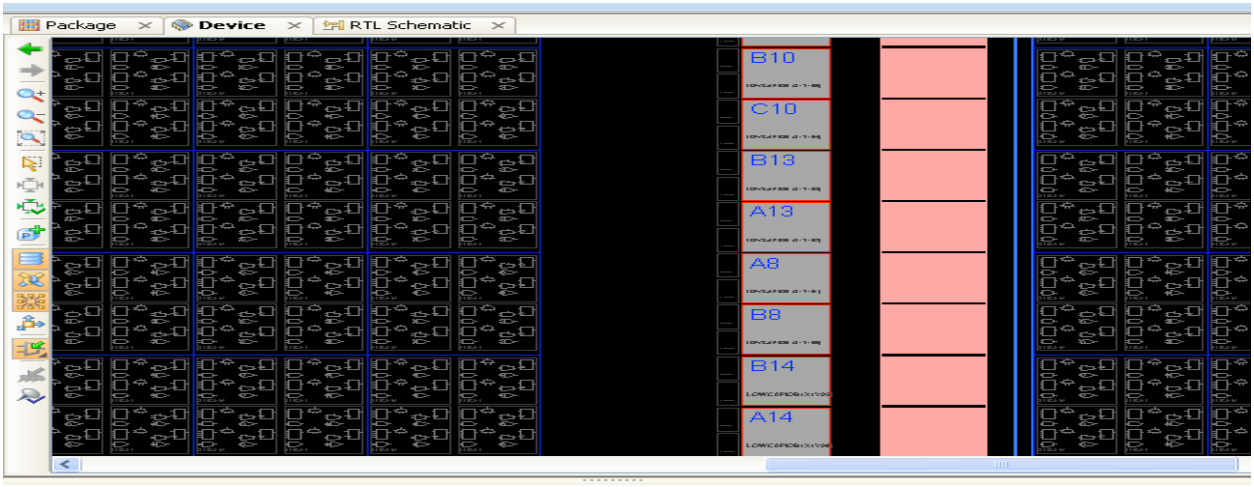
файл портов схема к реальные портов



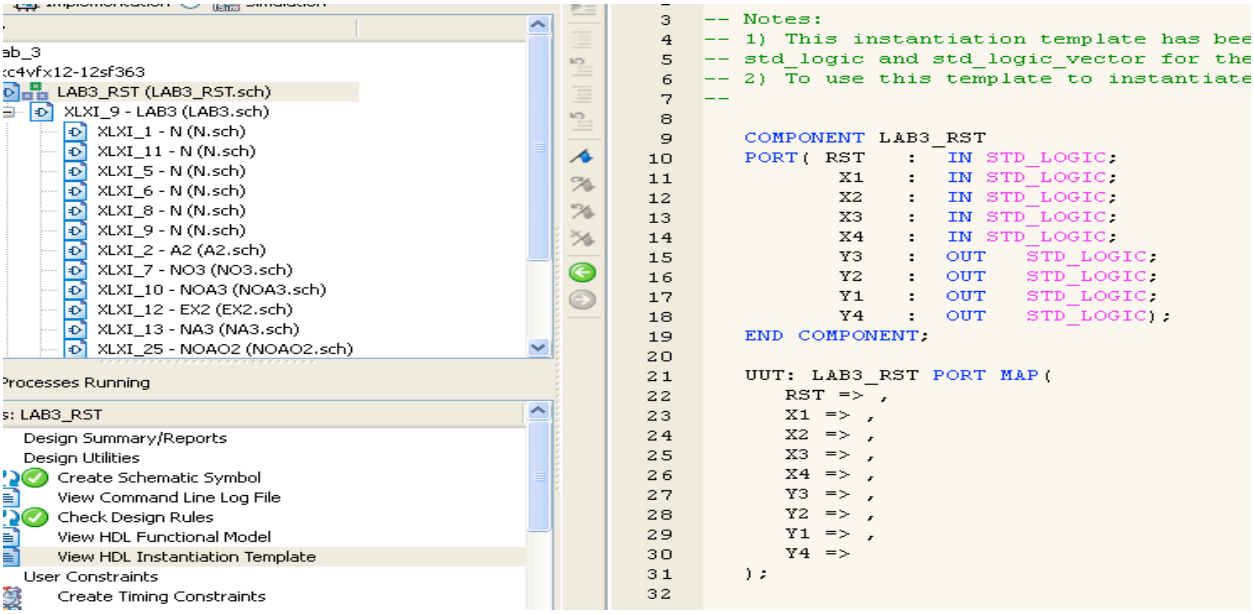


Реальный устройства с портами




Package
Device
RTL Schematic
B10
C10
B13
A13
A8
B8
B14
A14

VHDL Шаблон


LAB3_RST (LAB3_RST.sch)
XLXI_9 - LAB3 (LAB3.sch)
XLXI_1 - N (N.sch)
XLXI_11 - N (N.sch)
XLXI_5 - N (N.sch)
XLXI_6 - N (N.sch)
XLXI_8 - N (N.sch)
XLXI_9 - N (N.sch)
XLXI_2 - A2 (A2.sch)
XLXI_7 - NO3 (NO3.sch)
XLXI_10 - NOA3 (NOA3.sch)
XLXI_12 - EX2 (EX2.sch)
XLXI_13 - NA3 (NA3.sch)
XLXI_25 - NOAO2 (NOAO2.sch)
Processes Running
Design Summary/Reports
Design Utilities
Create Schematic Symbol
View Command Line Log File
Check Design Rules
View HDL Functional Model
View HDL Instantiation Template
User Constraints
Create Timing Constraints
-- Notes:
-- 1) This instantiation template has bee
-- std_logic and std_logic_vector for the
-- 2) To use this template to instantiate
COMPONENT LAB3_RST
PORT(RST : IN STD_LOGIC;
X1 : IN STD_LOGIC;
X2 : IN STD_LOGIC;
X3 : IN STD_LOGIC;
X4 : IN STD_LOGIC;
Y3 : OUT STD_LOGIC;
Y2 : OUT STD_LOGIC;
Y1 : OUT STD_LOGIC;
Y4 : OUT STD_LOGIC);
END COMPONENT;
UUT: LAB3_RST PORT MAP(
RST => ,
X1 => ,
X2 => ,
X3 => ,
X4 => ,
Y3 => ,
Y2 => ,
Y1 => ,
Y4 =>
);

Simulation:

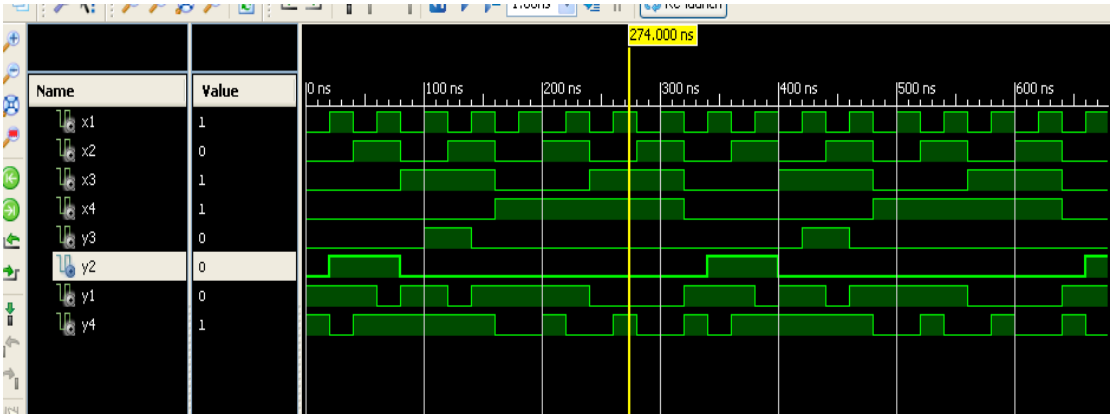


Таблица Истинности:

X1	X2	X3	X4	Y1	Y2	Y3	Y4
0	0	0	0	1	0	0	1
0	0	0	1	1	0	0	0
0	0	1	0	1	0	0	1
0	0	1	1	0	0	0	0
0	1	0	0	1	1	0	1
0	1	0	1	1	0	0	1
0	1	1	0	0	0	1	1
0	1	1	1	0	0	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	0	0	0
1	0	1	0	1	0	1	1
1	0	1	1	0	0	0	1
1	1	0	0	0	1	0	1
1	1	0	1	1	0	0	0
1	1	1	0	1	0	0	1
1	1	1	1	0	0	0	0

TestBench Code:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;
LIBRARY UNISIM;
USE UNISIM.Vcomponents.ALL;
ENTITY LAB3_LAB3_sch_tb IS
END LAB3_LAB3_sch_tb;
ARCHITECTURE behavioral OF LAB3_LAB3_sch_tb IS

   COMPONENT LAB3
   PORT( X1      :     IN    STD_LOGIC;
         X2      :     IN    STD_LOGIC;
         X3      :     IN    STD_LOGIC;
         X4      :     IN    STD_LOGIC;
         Y3      :     OUT   STD_LOGIC;
         Y2      :     OUT   STD_LOGIC;
         Y1      :     OUT   STD_LOGIC;
         Y4      :     OUT   STD_LOGIC);
   END COMPONENT;

   SIGNAL X1     :     STD_LOGIC;
   SIGNAL X2     :     STD_LOGIC;
   SIGNAL X3     :     STD_LOGIC;
   SIGNAL X4     :     STD_LOGIC;
   SIGNAL Y3     :     STD_LOGIC;
```

```
   SIGNAL Y2     :     STD_LOGIC;
   SIGNAL Y1     :     STD_LOGIC;
   SIGNAL Y4     :     STD_LOGIC;

BEGIN

   UUT: LAB3 PORT MAP(
           X1 => X1,
           X2 => X2,
           X3 => X3,
           X4 => X4,
           Y3 => Y3,
           Y2 => Y2,
           Y1 => Y1,
           Y4 => Y4
   );
   proces_x1 : PROCESS
     constant period :time := 20 ns;
   BEGIN
     X1 <= '0';
          wait for period;
          X1  <='1';
          wait for period;
   END PROCESS;

proces_x2 : PROCESS
     constant period :time := 40 ns;
```

```
   begin
      X2 <= '0';
       WAIT for period; -- will wait forever
            X2 <='1';
            wait for period;
   END PROCESS;
      proces_x3 : PROCESS
      constant period :time := 80 ns;
   begin
      X3 <= '0';
       WAIT for period; -- will wait forever
            X3 <='1';
            wait for period;
   END PROCESS;
      proces_x4 : PROCESS
      constant period :time := 160 ns;
   BEGIN
      X4 <= '0';
       WAIT for period; -- will wait forever
            X4 <='1';
            wait for period;
   END PROCESS;
-- *** End Test Bench - User Defined Section ***


END;
```

Вывод:

В заданном лаборатории был изучен как реализовать FPGA module в среде Xilinx.