**Задание:**Схема мультиплексирования(3 в 1) снастраиваемой̆ разрядностью (от 2 до 64 бит).

**VHDL-описание:**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity xilinx is

generic (width: integer := 64); --local variable

Port (

CLK: in std\_logic; -- clock sync

RST: in std\_logic; -- reset

DVI: in std\_logic; -- input validation data

DI\_A : in STD\_LOGIC\_VECTOR(width-1 downto 0);

DI\_B : in STD\_LOGIC\_VECTOR(width-1 downto 0);

DI\_C : in STD\_LOGIC\_VECTOR(width-1 downto 0);

d : in STD\_LOGIC\_VECTOR(width-1 downto 0);

MUX : in STD\_LOGIC\_VECTOR (1 downto 0); --control port

DVO: out std\_logic; -- output validation data

DO : out STD\_LOGIC\_VECTOR(width-1 downto 0) --output data

);

end xilinx;

architecturearchi of xilinx is

--local variable

signaloutputY: std\_logic\_vector(width downto 0);

begin

--process (DI\_A, DI\_B, DI\_C, d, MUX)

process(RST, CLK) ---

begin

if(RST ='1') then

outputY<= (others => '0');

DVO <= '0';

elsif(rising\_edge(CLK) and DVI = '1') then

DVO <= '1';

case MUX is

when "00" =>outputY<= ext(DI\_A, width+1);

when "01" =>outputY<= ext(DI\_B, width+1);

when "10" =>outputY<= ext(DI\_C, width+1);

when others =>outputY<= ext(d, width+1);

end case;

end if;

end process;

DO <= outputY(width-1 downto 0);

endarchi;

**Тестирование в ModelSim (дляразрядности 4 бит):**

force -freeze sim:/xilinx/clk 0 1, 1 {5 ns} -r 10

force -freeze sim:/xilinx/rst 0 0ns, 1 60ns

force -freeze sim:/xilinx/DVI 0 0ns, 1 10ns

force -freeze sim:/xilinx/DI\_A 0000 0ns, 1111 8ns, 1111 20ns, 1100 30ns, 0011 45ns, 0000 55ns, 1000 65ns

force -freeze sim:/xilinx/DI\_B 0000 0ns, 1111 8ns, 1100 20ns, 0011 30ns, 0010 45ns, 0001 55ns, 1001 65ns

force -freeze sim:/xilinx/DI\_C 0000 0ns, 1111 8ns, 1100 20ns, 0011 30ns, 0010 45ns, 0001 55ns, 1001 65ns

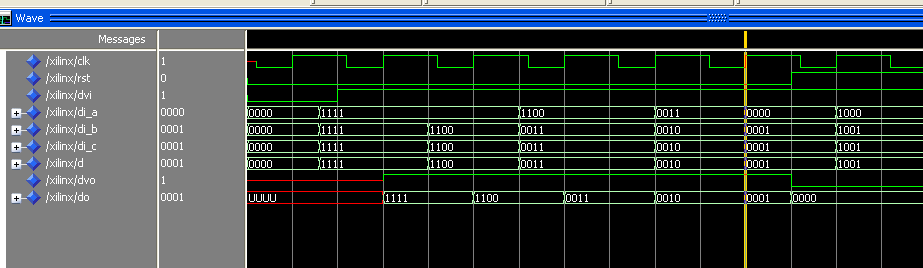
force -freeze sim:/xilinx/D 0000 0ns, 1111 8ns, 1100 20ns, 0011 30ns, 0010 45ns, 0001 55ns, 1001 65ns

run 85ns

run 85ns

write format wave -window .main\_pane.wave.interior.cs.body.pw.wf C:/modeltech\_6.5/examples/wave\_xilinx.do

write format wave -window .main\_pane.wave.interior.cs.body.pw.wf {C:/Documents and Settings/Administrator/My Documents/masters/Gladio/xilinx\_labs/wave\_xilinx.do}



**Тестирование в Xilinx (для разрядности 4 бит):**

**Отчет синтеза:**

Release 14.1 - xst P.15xf (nt)

Copyright (c) 1995-2012 Xilinx, Inc. All rights reserved.

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 1.00 secs

Total CPU time to Xst completion: 0.14 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 1.00 secs

Total CPU time to Xst completion: 0.14 secs

--> Reading design: lab1xilinx.prj

TABLE OF CONTENTS

1) Synthesis Options Summary

2) HDL Compilation

3) Design Hierarchy Analysis

4) HDL Analysis

5) HDL Synthesis

5.1) HDL Synthesis Report

6) Advanced HDL Synthesis

6.1) Advanced HDL Synthesis Report

7) Low Level Synthesis

8) Partition Report

9) Final Report

9.1) Device utilization summary

9.2) Partition Resource Summary

9.3) TIMING REPORT

=========================================================================

\* Synthesis Options Summary \*

=========================================================================

---- Source Parameters

Input File Name : "lab1xilinx.prj"

Input Format : mixed

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "lab1xilinx"

Output Format : NGC

Target Device : xc4vfx12-12-sf363

---- Source Options

Top Module Name : lab1xilinx

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Mux Style : Auto

Decoder Extraction : YES

Priority Encoder Extraction : Yes

Shift Register Extraction : YES

Logical Shifter Extraction : YES

XOR Collapsing : YES

ROM Style : Auto

Mux Extraction : Yes

Resource Sharing : YES

Asynchronous To Synchronous : NO

Use DSP Block : Auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 500

Add Generic Clock Buffer(BUFG) : 32

Number of Regional Clock Buffers : 16

Register Duplication : YES

Slice Packing : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As\_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Verilog 2001 : YES

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=========================================================================

=========================================================================

\* HDL Compilation \*

=========================================================================

Compiling vhdl file "C:/Documents and Settings/Administrator/My Documents/masters/Gladio/xilinx\_labs/xilinx.vhdl" in Library work.

Entity <lab1xilinx> compiled.

Entity <lab1xilinx> (Architecture <archi>) compiled.

=========================================================================

\* Design Hierarchy Analysis \*

=========================================================================

Analyzing hierarchy for entity <lab1xilinx> in library <work> (architecture <archi>) with generics.

width = 4

=========================================================================

\* HDL Analysis \*

=========================================================================

Analyzing generic Entity <lab1xilinx> in library <work> (Architecture <archi>).

width = 4

Entity <lab1xilinx> analyzed. Unit <lab1xilinx> generated.

=========================================================================

\* HDL Synthesis \*

=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit <lab1xilinx>.

Related source file is "C:/Documents and Settings/Administrator/My Documents/masters/Gladio/xilinx\_labs/xilinx.vhdl".

WARNING:Xst:647 - Input <d> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

Found 1-bit register for signal <DVO>.

Found 1-bit register for signal <outputY>.

Found 1-bit 3-to-1 multiplexer for signal <outputY$mux0000> created at line 37.

Summary:

inferred 2 D-type flip-flop(s).

inferred 1 Multiplexer(s).

Unit <lab1xilinx> synthesized.

=========================================================================

HDL Synthesis Report

Macro Statistics

# Registers : 2

1-bit register : 2

# Multiplexers : 1

1-bit 3-to-1 multiplexer : 1

=========================================================================

=========================================================================

\* Advanced HDL Synthesis \*

=========================================================================

=========================================================================

Advanced HDL Synthesis Report

Macro Statistics

# Registers : 2

Flip-Flops : 2

# Multiplexers : 1

1-bit 3-to-1 multiplexer : 1

=========================================================================

=========================================================================

\* Low Level Synthesis \*

=========================================================================

Optimizing unit <lab1xilinx> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block lab1xilinx, actual ratio is 0.

Final Macro Processing ...

=========================================================================

Final Register Report

Macro Statistics

# Registers : 2

Flip-Flops : 2

=========================================================================

=========================================================================

\* Partition Report \*

=========================================================================

Partition Implementation Status

-------------------------------

No Partitions were found in this design.

-------------------------------

=========================================================================

\* Final Report \*

=========================================================================

Final Results

RTL Top Level Output File Name : lab1xilinx.ngr

Top Level Output File Name : lab1xilinx

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

# IOs : 11

Cell Usage :

# BELS : 3

# LUT3 : 1

# MUXF5 : 1

# VCC : 1

# FlipFlops/Latches : 2

# FDCE : 2

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 9

# IBUF : 7

# OBUF : 2

=========================================================================

Device utilization summary:

---------------------------

Selected Device : 4vfx12sf363-12

Number of Slices: 1 out of 5472 0%

Number of 4 input LUTs: 1 out of 10944 0%

Number of IOs: 11

Number of bonded IOBs: 10 out of 240 4%

IOB Flip Flops: 2

Number of GCLKs: 1 out of 32 3%

---------------------------

Partition Resource Summary:

---------------------------

No Partitions were found in this design.

---------------------------

=========================================================================

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

------------------

-----------------------------------+------------------------+-------+

Clock Signal | Clock buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

CLK | BUFGP | 2 |

-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:

----------------------------------------

-----------------------------------+------------------------+-------+

Control Signal | Buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

RST | IBUF | 2 |

-----------------------------------+------------------------+-------+

Timing Summary:

---------------

Speed Grade: -12

Minimum period: No path found

Minimum input arrival time before clock: 1.723ns

Maximum output required time after clock: 3.793ns

Maximum combinational path delay: No path found

Timing Detail:

--------------

All values displayed in nanoseconds (ns)

=========================================================================

Timing constraint: Default OFFSET IN BEFORE for Clock 'CLK'

Total number of paths / destination ports: 7 / 3

-------------------------------------------------------------------------

Offset: 1.723ns (Levels of Logic = 3)

Source: MUX<0> (PAD)

Destination: outputY (FF)

Destination Clock: CLK rising

Data Path: MUX<0> to outputY

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 1 0.754 0.514 MUX\_0\_IBUF (MUX\_0\_IBUF)

LUT3:I0->O 1 0.147 0.000 Mmux\_outputY\_mux000021 (Mmux\_outputY\_mux00002)

MUXF5:I0->O 1 0.291 0.000 Mmux\_outputY\_mux00002\_f5 (outputY\_mux0000)

FDCE:D 0.017 outputY

----------------------------------------

Total 1.723ns (1.209ns logic, 0.514ns route)

(70.2% logic, 29.8% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'CLK'

Total number of paths / destination ports: 2 / 2

-------------------------------------------------------------------------

Offset: 3.793ns (Levels of Logic = 1)

Source: outputY (FF)

Destination: DO (PAD)

Source Clock: CLK rising

Data Path: outputY to DO

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDCE:C->Q 1 0.272 0.266 outputY (outputY)

OBUF:I->O 3.255 DO\_OBUF (DO)

----------------------------------------

Total 3.793ns (3.527ns logic, 0.266ns route)

(93.0% logic, 7.0% route)

=========================================================================

Total REAL time to Xst completion: 7.00 secs

Total CPU time to Xst completion: 6.39 secs

-->

Total memory usage is 155280 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 1 ( 0 filtered)

Number of infos : 0 ( 0 filtered)

**RTL-схема (черный ящик):**

**Белый ящик:**