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| 32-bit FLOATING POINT MULTIPLIER IMPLEMENTATION |

*Version 1.0 (Wednesday, April 17, 2019)*

Preface:

We[[1]](#footnote-0) have created this multiplier to handle the multiplication process of two 32-bit IEEE 754 based numbers as a part of FPU project[[2]](#footnote-1).

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APPENDEX a. OUR TOOLKIT

APPENDEX B. REFERENCES

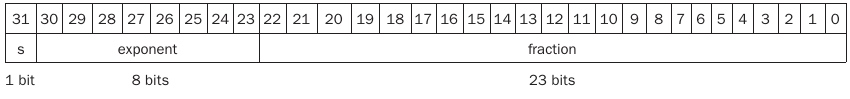
chapter 1:

“IEEE 754” representation

“This kind of refreshing part for the sake of comprehension.”

Floating-Point Representation:

Floating-point numbers are usually a multiple of the size of a word. The representation of a MIPS floating-point number is shown below, where s is the sign of the floating-point number (1 meaning negative), exponent is the value of the 8-bit exponent field (including the sign of the exponent), and fraction is the 23-bit number.



In general, floating-point numbers are of the form

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These formats go beyond MIPS. They are part of the IEEE 754 floating-point standard, found in virtually every computer invented since 1980. This standard has greatly improved both the ease of porting floating-point programs and the quality of computer arithmetic.

Before we go on board we have to take these notes with us:

1. Number must be normalized in an understandable language ( 1.01000 \* 2^E not 101.000\* 2^E-3 )
2. Exponents are biased by 127 which means 0 = 127 to get the the real exponent form IEEE754 one subtract 127 from it.

chapter 2:

Our implementation journey

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2. **FPU project:** the floating point unit to be used in our implementation of MIPS based processor [↑](#footnote-ref-1)