



- This is a closed book exam.
- Read each question carefully before answering it, and list any important assumptions you make.
- Exam questions in two pages, answer all of them.
- Good Luck!

1. Choose the correct answers

[10 marks]

- i. Combinational circuits are described by
 - a) Boolean functions
 - b) algebraic functions
 - c) geometric functions
 - d) linear equations
- ii. Most basic arithmetic function is
 - a) addition
 - b) subtraction
 - c) multiplication
 - d) division
- iii. The ⁸octal representation of the binary number 1011.0011 is
 - a) 3.14
 - b) 13.14
 - c) 11.1875
 - d) B.3
- iv. The BCD number for decimal 16 is $16+6=22$
 - a) 00010110
 - b) 00010011
 - c) 00010010
 - d) 11100000
- v. Decoder is a
 - a) combinational circuit
 - b) sequential circuit
 - c) complex circuit
 - d) gate
- vi. One that is a universal gate
 - a) AND gate
 - b) OR gate
 - c) NOR gate
 - d) XOR gates
- vii. In BCD, number 1010 has
 - a) meaning
 - b) no meaning
 - c) value
 - d) Vcc
- viii. In designing combinational circuits, truth table defines relationship of
 - a) input
 - b) output
 - c) logical circuit
 - d) input and output
- ix. The output of a NAND gate is LOW if
 - a) all inputs are LOW
 - b) all inputs are HIGH
 - c) any input is LOW
 - d) any input is HIGH
- x. Which of the following expressions is in the product-of-sums form?
 - a) $(AB)(CD)$
 - b) $AB(CD)$
 - c) $(A + B)(C + D)$
 - d) $AB + CD$
- ② Design a circuit that counts the number of 1's present in 3 inputs A, B and C. Its output is a two-bit number X_1X_0 , representing that count in binary. [10 marks]
- ③ Consider the two circuits shown below in Figure 1. Use algebraic transformations to prove or disprove that the two circuits implement the same function. ?? [10 marks]

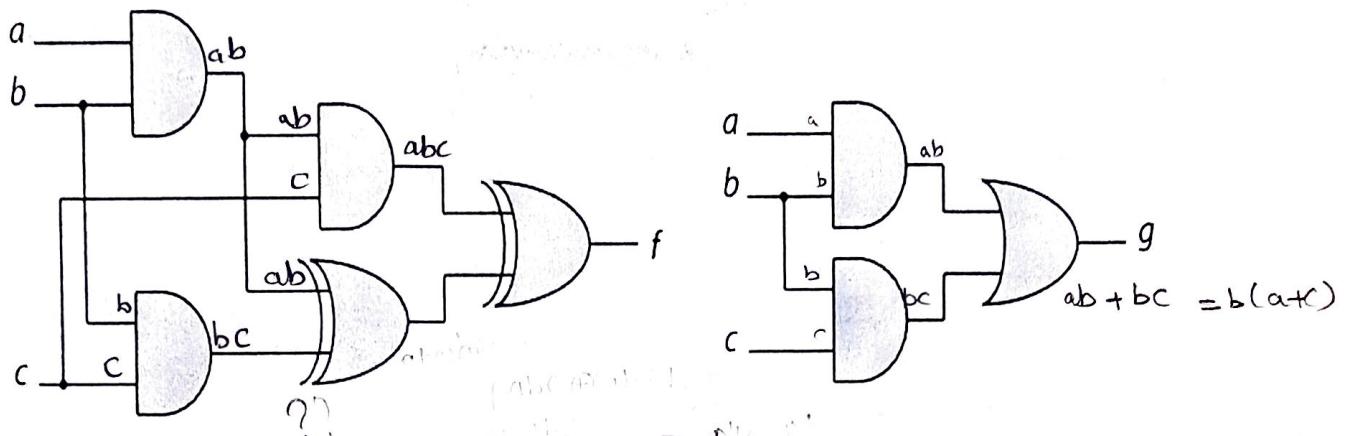


Figure 1

4. Minimize the following Boolean function and implement with

i. 8x1 multiplexer,

ii. 4x1 multiplexer and logic gates,

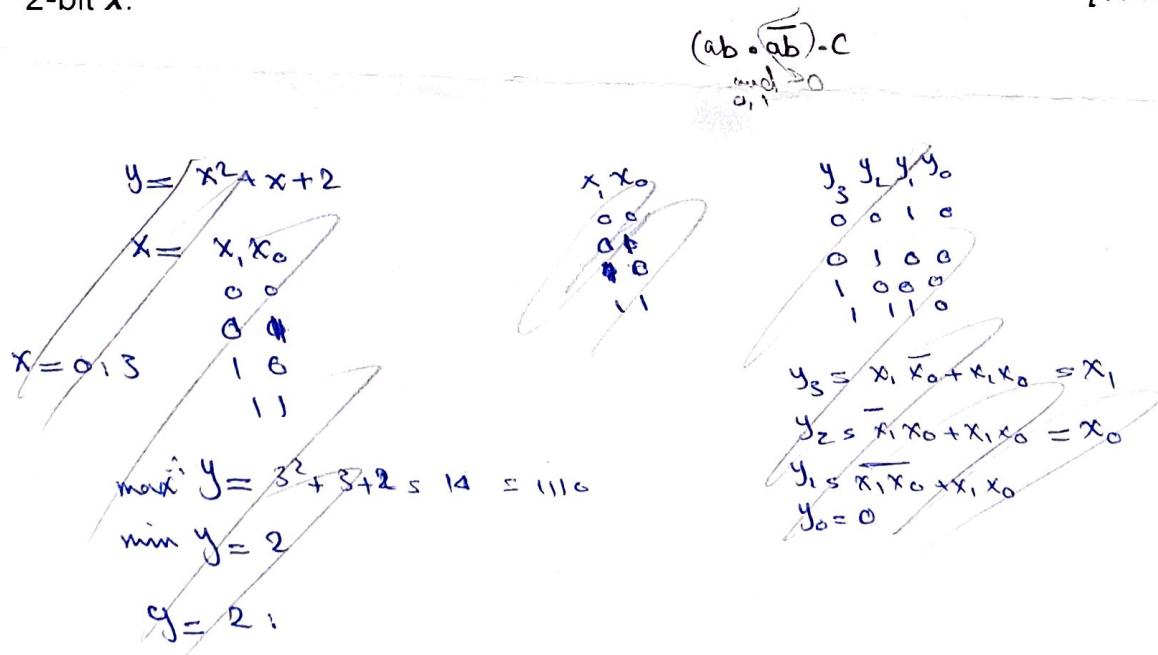
iii. a decoder.

$$F(A, B, C, D) = \sum(0, 1, 3, 4, 7, 9, 15).$$

[10 marks]

5. Design a combinational circuit that computes the function $f(x) = x^2 + x + 2$ for a 2-bit x .

[10 marks]





34.5
50

- This is a closed book exam.
- Read each question carefully before answering it, and list any important assumptions you make.
- Exam questions in 4 pages, answer all of them.
- Good Luck!

1. Complete the following sentences

5.5 [10 marks]

i. The equivalent decimal of the octal number $(270.4)_8$ is ... 184.5 1.....

ii. The 2's complement of the decimal number -48 is ... 110000 0.5.....

iii. Half Adder and Full Adder are types of the binary adders.

iv. The BCD number for decimal 14 is 1110

v. Multiplexer is a Combinational Circut that allows me to select one of the inputs to be output.

vi. If a decoder has 16 outputs, it requires 4 1 inputs to choose all possible outputs.

vii. $A \oplus 1$ is equal to \bar{A}

viii. The Quine-McCluskey algorithm is a method used for Reducing Logic gates numbers 1

ix. The output of a NOR gate is HIGH if Two inputs are zero 1

x. The minimum number of 2-input NAND gates required to implement a 2-input XOR gate is 9 NAND

2. Consider the circuit shown below in Figure 1. Determine the outputs functions A and B as sums of minterms.

3 [10 marks]

$$A = \bar{x}y\bar{z} + \bar{x}y{z}$$

x	y	z	N
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

$$B = x\bar{y}z + x\bar{y}\bar{z}$$

$$= xz(y + \bar{y})$$

$$B = xz$$

S ₁	S ₀	A	B
0	0	0	0
0	1	1	0

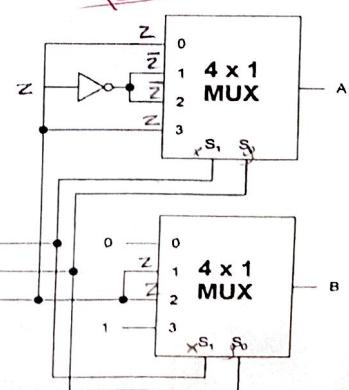


Figure 1

3. Design a combinational circuit with three inputs, x, y, and z, and three outputs, A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input. [10 marks]

	x	y	z	A	B	C
0	0	0	0	0	0	1
1	0	0	1	0	1	0
2	0	1	0	0	1	1
3	0	1	1	1	0	0
4	1	0	0	0	0	0
5	1	0	1	0	0	0
6	1	1	0	1	0	0
7	1	1	1	1	1	0

x	y	z	00	01	11	10	
0	0	0	0	0	0	1	0
1	1	0	1	1	1	1	0

$$A = \bar{y}z + xz + xy \quad \textcircled{1}$$

x	y	z	00	01	11	10	
0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0

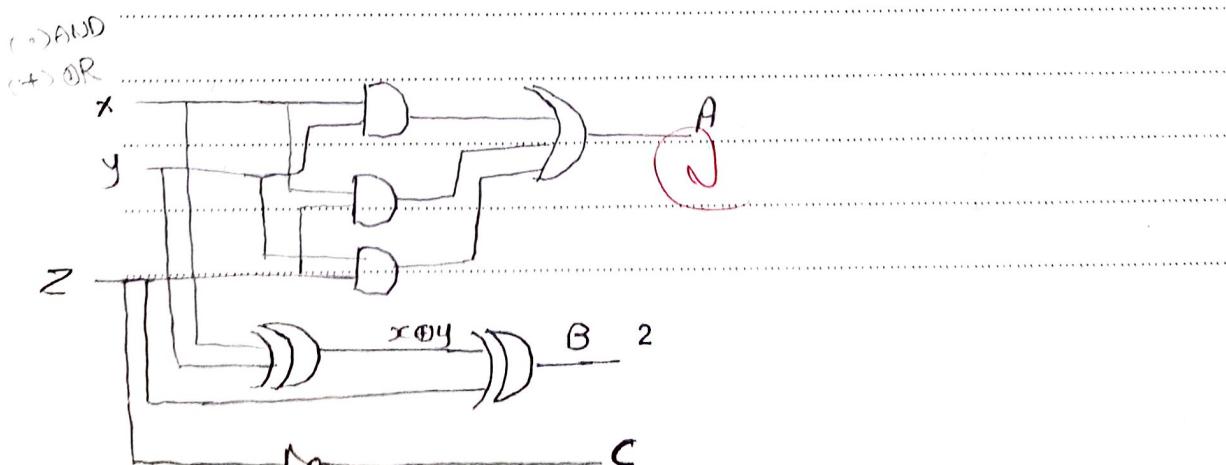
$$B = \bar{x}yz + \bar{x}y\bar{z} + x\bar{y}z + xy\bar{z}$$

$$= z(\bar{x}y + xy) + \bar{z}(x\bar{y} + \bar{x}y) \quad \textcircled{2}$$

$$= z(\bar{x} \oplus y) + \bar{z}(x \oplus y) = (z \oplus x \oplus y)$$

x	y	z	00	01	11	10	
0	1	0	0	0	0	1	0
1	1	0	0	0	1	1	0

$$C = \bar{z} \quad \textcircled{3}$$



4. Simplify the following Boolean function F , together with the don't care conditions d , and implement it with two-level NAND gate circuits. [10 marks]

$$F(A,B,C,D) = \sum(3,6,7,8,10,14,15)$$

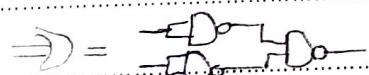
$$d(A,B,C,D) = \sum(1,4,5,13)$$

AB	CD	00	01	11	10
00	0	X	1	0	
01	X	X	1	1	
11	0	X	1	1	
10	1	1	0	1	1

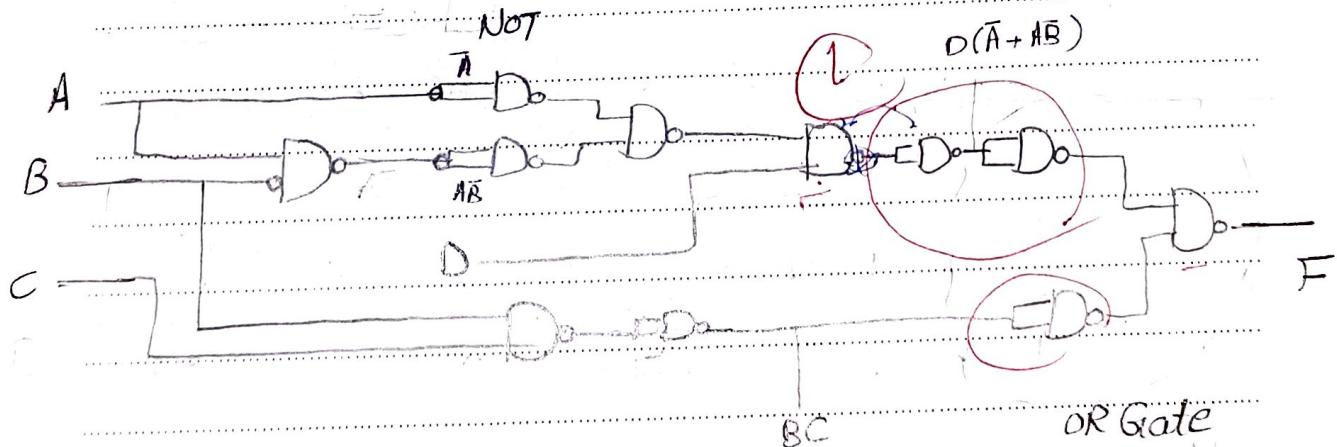
$$F = \bar{A}D + BC + A\bar{B}D$$

$$= D(\bar{A} + A\bar{B}) + BC$$

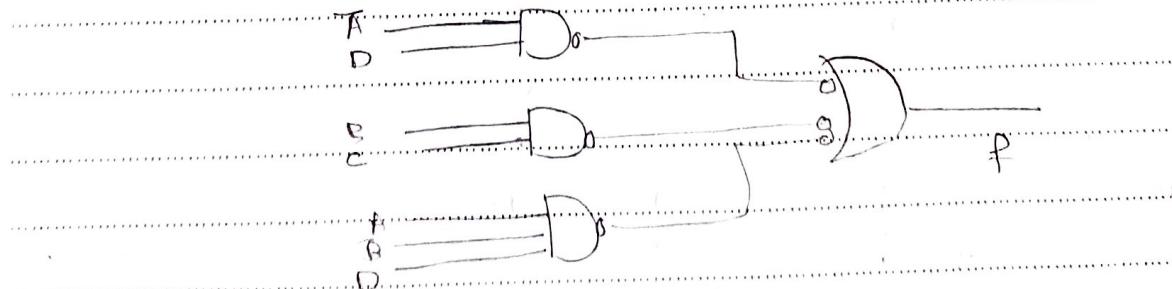
(B)



NOT



OR Gate



Allowed Time: 3 h.

Question 1:

- a) Complete the timing diagram for the circuit shown in figure (1), assuming all Q outputs begin in the low state

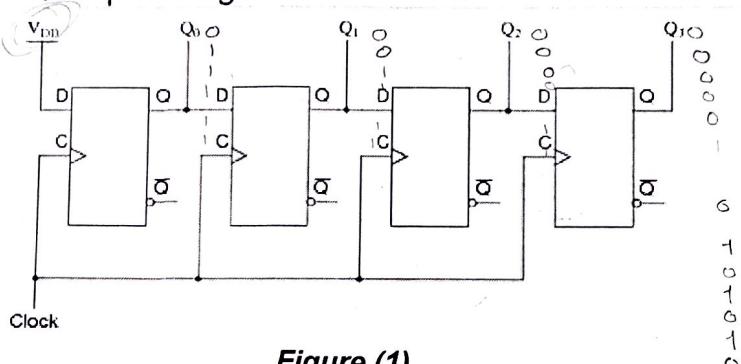


Figure (1)

- b) A XY Flip flop has four operations, complement, no change, set to 1, and clear to 0, when inputs X and Y are 00, 10, 01, and 11, respectively. Show how to build this flip flop using JK Flip Flop and any additional logic required.

Question 2:

- a) For function $F(x,y,z) = xy'z + xyz' + x'y'z'$:

1 Create the truth table.

2 Implement F by a 3-to-8 decoder and any additional logic required.

- b) Consider the combinational circuit shown in figure (2), derive the Boolean expression for the output F and G

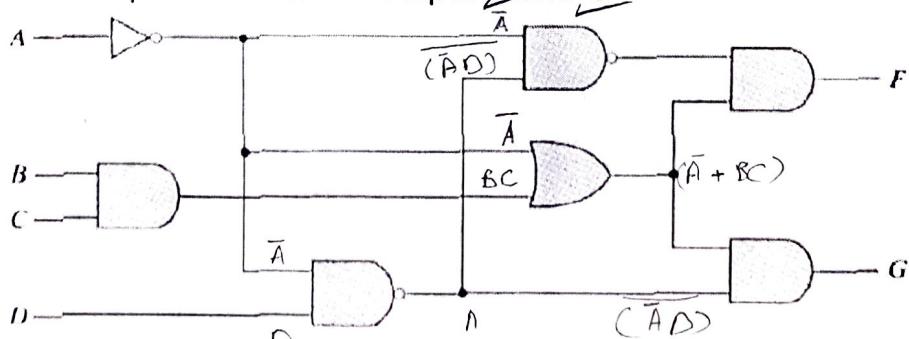


Figure (2)

Question 3:

- a) For 4×1 multiplexer (shown in figure (3)), determine the output for the following input states: $D_0=0$, $D_1=1$, $D_2=1$, $D_3=0$, $S_0=1$, $S_1=1$.

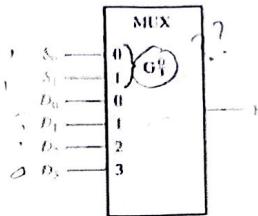


Figure (3)

- b) There are three major courses X, Y and Z, and three minor courses A and B and C in a department. A student can graduate if he or she passes:

1- All the major courses from X to Z, OR 2- X and Y and two of the minor courses

Write a Boolean equation to represent the graduation condition.

Hint: Use the name of the courses as the variables of your equation. i.e., X, Y, Z, A, B, C. Variable X is 1 if a student passes course X, otherwise 0.

Question 4:

- a) If you are given the Boolean expression $f = AB(CD+EF)$, implement the corresponding combinational circuit using logic gates.
- b) An 8-bit shift register holds the data word 11001100. What will the register contents are after four left and right shifts? (Assume that serial input = 1).

c) Design (draw circuit and timing diagram) 4 bit up binary counter.

Question 5:

- a) Design (truth table, Boolean function, and implement circuit using logic gates) 2-bit comparator to check equality.
- b) Write a VHDL program to implement 2-bit comparator to check equality.

Good Luck



- Read each question carefully before answering it and list any important assumptions you make.
- The Exam contains 8 questions in 3 pages, try to answer all of them.
- Good Luck!

1. Choose the correct answers

[20 marks]

i. $(A + B)(A' \cdot B') = ?$

- a. 0 b. 1 c. AB d. AB'

ii. 10100 is the two's complement representation of:

- a. +11 b. -11 c. +12 d. -12

$$\begin{array}{r} 10100 \\ 11111 + \\ \hline 110011 \\ 00\ 1100 \end{array}$$

iii. LUT is acronym for

- a. Look Up Table b. Local User Terminal c. Least Upper Time Period d. None of these

iv. What logic circuit would you use for addressing memory?

- a. Full adder b. Multiplexer c. ALU d. Decoder

v. Which parts of the computer perform arithmetic calculations?

- a. ALU b. Registers c. Logic bus d. none of them

vi. Dynamic memory cells use..... as the storage device.

- a. The reactance of a transistor b. The impedance of a transistor
c. The capacitance of a transistor d. None of the Mentioned

vii. The combinational circuit is depending on

- a. Future input b. Present input c. Past and present d. None of these

viii. One application of a digital multiplexer is to facilitate:

- a. code conversion b. parity checking c. parallel to serial data conversion d. data generation

ix. Odd parity of a bit stream can be tested using gate.

- a. NOR b. OR c. XNOR d. XOR

x. The group of bits 10110111 is serially shifted (right-most bit first) into an 8-bit parallel output shift register with an initial state 11110000. After two clock pulses, the register contains

- a. 10111000 b. 10110111 c. 11110000 d. 11111100

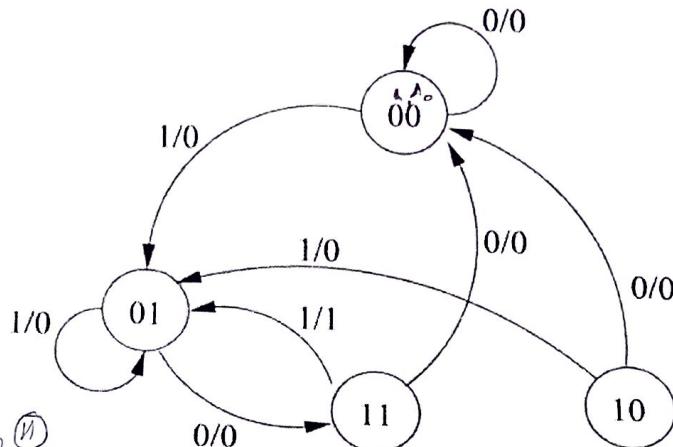
2. Describe how you can convert by adding external gates:

[20 marks]

- a) a D flip-flop to a J-K flip-flop.
- b) a T flip-flop to a D flip-flop.
- c) a JK flip-flop to a T flip-flop.

3. Consider the following state diagram for a synchronous circuit with one input X and one output Z. Analyze this state diagram and draw its circuit implementation using JK flip-flop (state Q0) and T flip-flop (state Q1) and MUX-4x1 for Z.

[30 marks]



4. Given a 32x8 ROM chip with an enable input, show the block level required connections to construct a 128x8 ROM with above ROM chips and a decoder. How many data and address lines these ROMs have? [20 marks]

5. Using the following table (Gray Code), do the following:
Design 3-bit Up/Down Synchronous Gray Code Counter (using JK flip-flops) and one external input Y, When Y=1, the counter works up, and Y=0, the counter works down.

[30 marks]

Decimal number	Gray Code Inputs		
	G2	G1	G0
0	0	0	0
1	0	0	1
2	0	1	1
3	0	1	0
4	1	1	0
5	1	1	1
6	1	0	1
7	1	0	0

6. Write a VHDL code to implement a basic 4x1 Multiplexer.

[15 marks]

7. Given the following Boolean function:

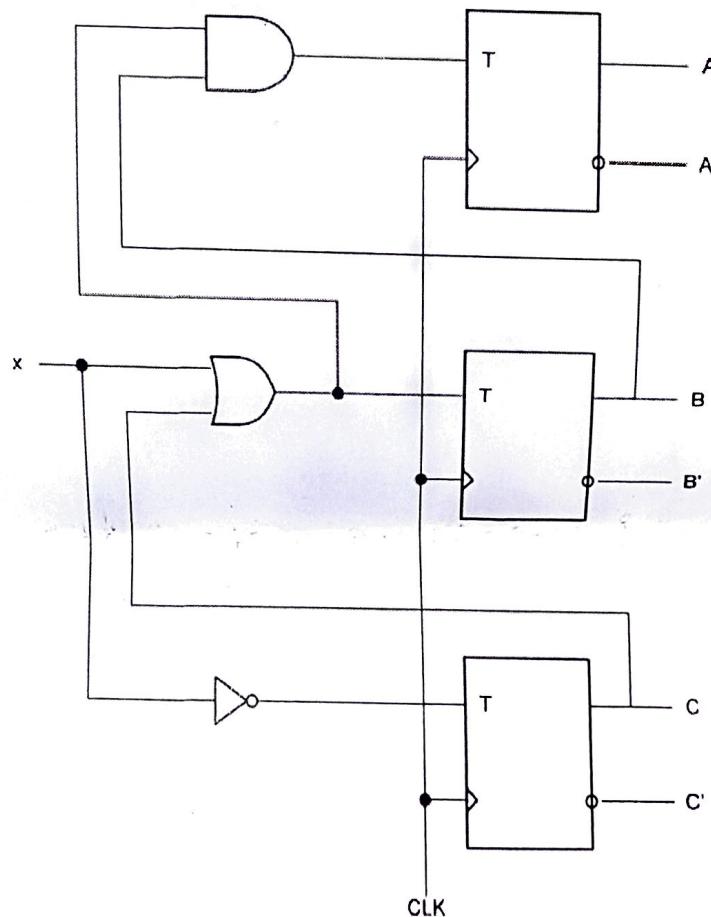
[20 marks]

$$F(w,x,y,z) = xy'z + x'y'z + w'xy + wx'y + wxy$$

- a) Draw a corresponding Karnaugh map of the function.
- b) Give minterm and maxterm expressions.
- c) Simplify the function and implement it by NAND gates only.

8. Derive the state table and the state diagram of the sequential circuit shown below. Explain the function that the circuit performs.

[25 marks]



With my best wishes

H.S. Mogahed