INTERFACING

WATCHDOG TIMER

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Watchdog Timer:

Definition:

- A watchdog timer is a piece of hardware that can be used to automatically detect software anomalies and reset the processor if any occur. Generally speaking, a watchdog timer is based on a counter that counts down from some initial value to zero. The embedded software selects the counter's initial value and periodically restarts it. If the counter ever reaches zero before the software restarts it, the software is presumed to be malfunctioning and the processor's reset signal is asserted. The processor (and the embedded software it's running) will be restarted as if a human operator had cycled the power.

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Watchdog Timer:

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- A watchdog timer is commonly used to calculate the approximately execution time of any function, by enabling the watchdog timer before calling and turning off after calling, if the system is reset, that means that the execution time of function exceeds the time that watchdog timer has been configured and if the system is not reset, that means that the time of function execution may be equaled or less than the time of watchdog timer.

- It is also used to avoid the system from dead lock, like when more than one task that needs the same semaphores, dead lock will be explained clearly later.

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Watchdog Timer:

Register Description:

- Watchdog Timer Control Register – WDTCR:
  - Watchdog Turn-off Enable: "**WDTOE**"

    This bit must be set when the WDE bit is written to logic zero. Otherwise, the Watchdog will not be disabled. Once written to one, hardware will clear this bit after four clock cycles. Refer to the description of the WDE bit for a Watchdog disable procedure.

Watchdog Timer Control Register – WDTCR

Bit	7	6	5	4	3	2	1	0
	–	–	–	WDTOE	WDE	WDP2	WDP1	WDP0
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

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Watchdog Timer:

Register Description:

- Watchdog Timer Control Register – WDTCR:
  - When the WDE is written to logic one, the Watchdog Timer is enabled, and if the WDE is written to logic zero, the Watchdog Timer function is disabled. WDE can only be cleared if the WDTOE bit has logic level one. To disable an enabled Watchdog Timer, the following procedure must be followed:
    - In the same operation, write a logic one to WDTOE and WDE. A logic one must be written to WDE even though it is set to one before the disable operation starts.
    - Within the next four clock cycles, write a logic 0 to WDE. This disables the Watchdog.

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Watchdog Timer:
Register Description:

- Watchdog Timer Control Register – WDTCR:
  - The WDP2, WDP1, and WDP0 bits determine the Watchdog Timer prescaling when the Watchdog Timer is enabled. The different prescaling values and their corresponding Timeout Periods are shown in Table 17.

Table 17. Watchdog Timer Prescale Select

WDP2	WDP1	WDP0	Number of WDT Oscillator Cycles	Typical Time-out at V_{CC} = 3.0V	Typical Time-out at V_{CC} = 5.0V
0	0	0	16K (16,384)	17.1 ms	16.3 ms
0	0	1	32K (32,768)	34.3 ms	32.5 ms
0	1	0	64K (65,536)	68.5 ms	65 ms
0	1	1	128K (131,072)	0.14 s	0.13 s
1	0	0	256K (262,144)	0.27 s	0.26 s
1	0	1	512K (524,288)	0.55 s	0.52 s
1	1	0	1,024K (1,048,576)	1.1 s	1.0 s
1	1	1	2,048K (2,097,152)	2.2 s	2.1 s

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Watchdog Timer:

Sudo Code of Watchdog Timer:

- Turn on Watchdog Timer:

```
WDTCR = (1<<WDE) | (Prescaler);
```

- Turn on Watchdog Timer:

```
WDTCR = (1<<WDE) | (1<<WDTOE);
WDTCR = 0x00;
```

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Watchdog Driver:

Time To Code

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THANK YOU!