INTERFACING

SESSION TIMER 2

Pulse Width Modulation:

Definition:

- Pulse-width modulation (PWM) is a modulation process or technique used in most communication systems for encoding the amplitude of a signal right into a pulse width or duration of another signal, usually a carrier signal, for transmission.

- Although PWM is also used in communications, its main purpose is to control the power that is supplied to various types of electrical devices, most especially to inertial loads such as AC/DC motors.

- Pulse-width modulation (PWM), or pulse-duration modulation (PDM), is a method of reducing the average power delivered by an electrical signal, by effectively chopping it up into discrete parts.

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Pulse Width Modulation:

Definition:

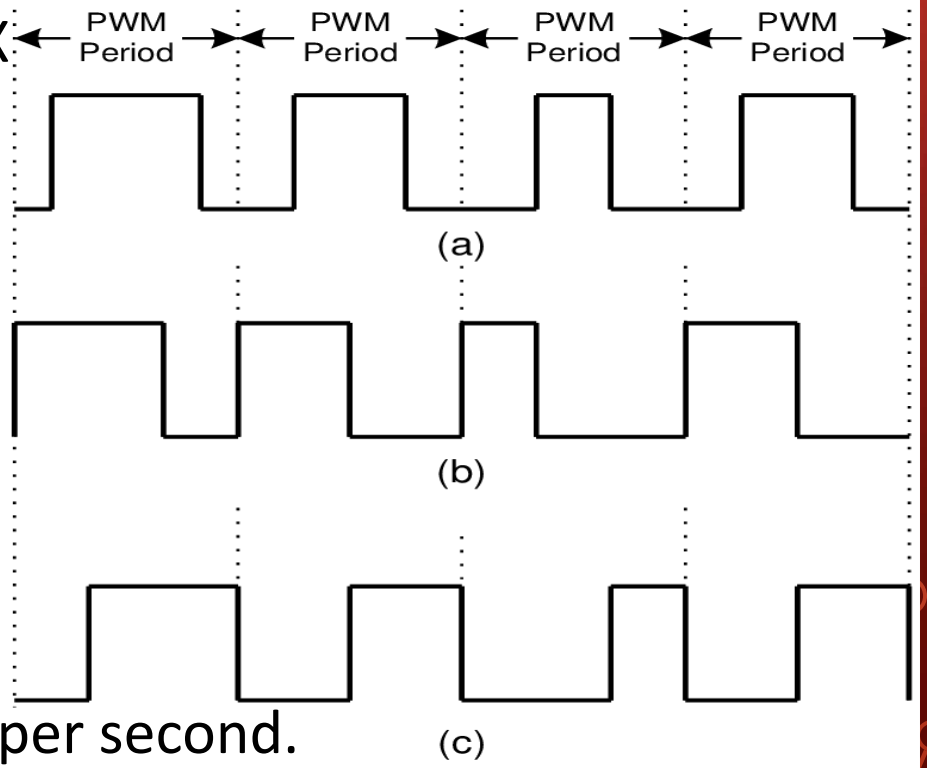
- As we mentioned before, PWM is a method to reduce the average of power.
- It can be generated by on-off sequence, I mean making a pin to be high then to be low in a speed sequence.
- PWM is like the potentiometer which also reduces the power according to its position which is human dependency controllable and most of power is consumed into it and it depends on voltage divider Law, but PWM is automatically control “by microcontroller” and the power is totally consumed inside the load, and it depends on root mean square Law.

AMIT

Pulse Width Modulation:

Main Parameters:

- Amplitude:
  - The voltage difference between the MAX voltage of cycle “on state” and the MIN voltage of cycle “off state”.



- Period:
  - It is the time of full cycle “High level time + Low level time”.

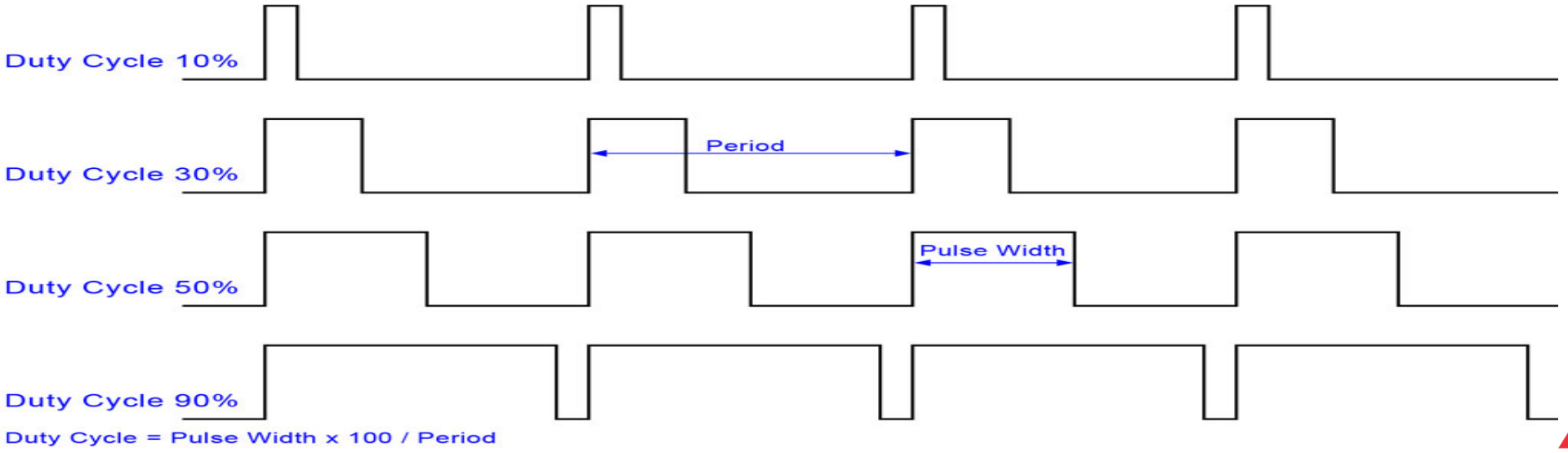
- Frequency:
  - It is the total number of cycles “period” per second.
  - $freq = \frac{1}{period\ of\ full\ cycle}$

AMIT

Pulse Width Modulation:

Main Parameters:

- Duty Cycle:
  - It is the ratio between the High-level time “on period” and the total time of the cycle “off period”.
  - $Duty\ Cycle = \frac{High\ level\ period}{time\ of\ full\ cycle} = \frac{Pulse\ Width}{Period}$



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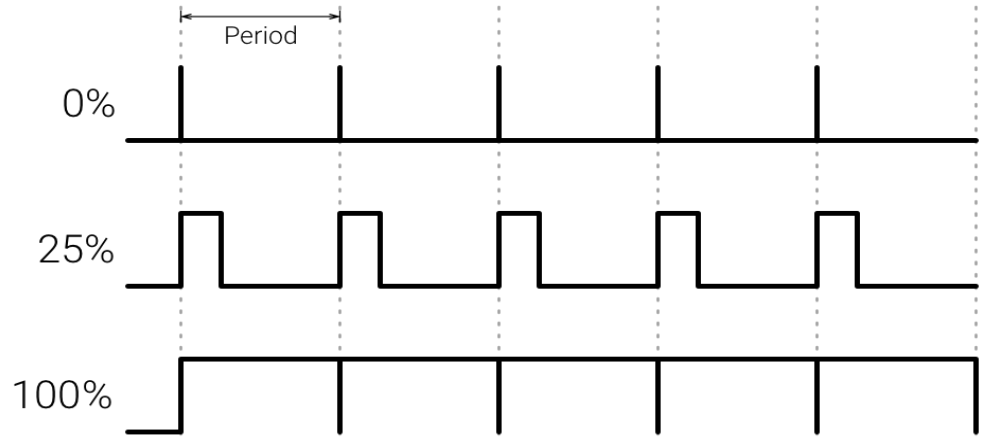
Pulse Width Modulation:

Main Parameters:

- Duty Cycle:
  - It is the ratio between the High-level time “on period” and the total time of the cycle “off period”.
  - $Duty\ Cycle\ = \frac{High\ level\ period}{time\ of\ full\ cycle}$



- Root Mean Square:
  - It is the effective volt that affects on the circuit, I mean that the equivalent voltage that has the same effective of PWM voltage.
  - $RMS = Amplitude\ \times \sqrt{Duty\ Cycle}$

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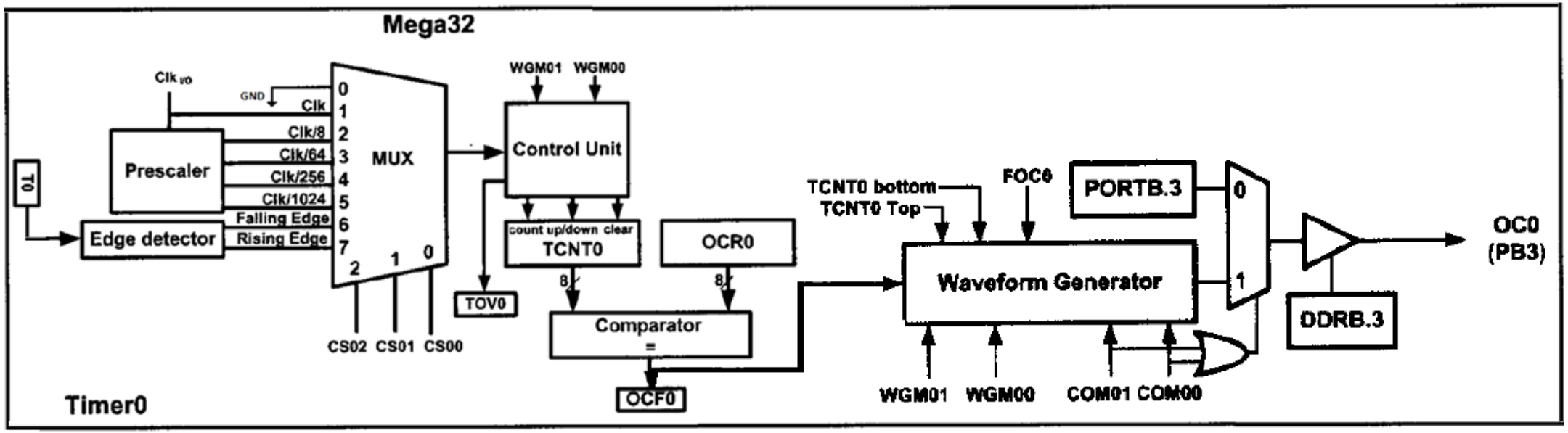
Pulse Width Modulation:

Hardware Implementation:

- The hardware of PWM is integrated with the hardware of the Timers, so, the Timers can be configured to generate a PWM.

- Let's discover how to generate a PWM using Timer Hardware.



Pulse Width Modulation:

Hardware Implementation:

- As we mentioned before that there is a I/O pin that the wave generator can control its level value according to the value of “COMxx” bits into overflow and compare match mode.
- Now, the mode of Timer will be changed to PWM generation, so the control unit behavior will act to generate a PWM away from the behavior of overflow or compare match.
- The main function of TCNTx is to overflow if it reaches its top.
- The main function of OCRx is to Compare with TCNTx, then a signal will be generated if the value into TCNTx equals the value of OCRx.

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Pulse Width Modulation:

Hardware Implementation:

- Because any PWM needs to be high for a specific time, then to be low for a specific time, we will exploit TCNTx and OCRx to change the value level on OCx pin using wave generator.

- TCNTx will be increased every clock cycle as usual, till it reaches its overflow point, and OCRx will be compared with TCNTx value every clock cycle, till they become having the same value, a signal will be generated, So on OCRx signal the OCx pin value will be changed and on the top of TCNTx the OCx pin value will be changed again.

- The previous explanation is exactly FAST PWM, it is called by fast because the TCNTx is overflowed after reaching its TOP.

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Pulse Width Modulation:

FAST PWM:

- Because any PWM needs to be high for a specific time, then to be low for a specific time, we will exploit TCNTx and OCRx to change the value level on OCx pin using wave generator.

- TCNTx will be increased every clock cycle as usual, till it reaches its overflow point, and OCRx will be compared with TCNTx value every clock cycle, till they become having the same value, a signal will be generated, So on OCRx signal the OCx pin value will be changed and on the top of TCNTx the OCx pin value will be changed again.

- The previous explanation is exactly FAST PWM, it is called by fast because the TCNTx is overflowed after reaching its TOP.

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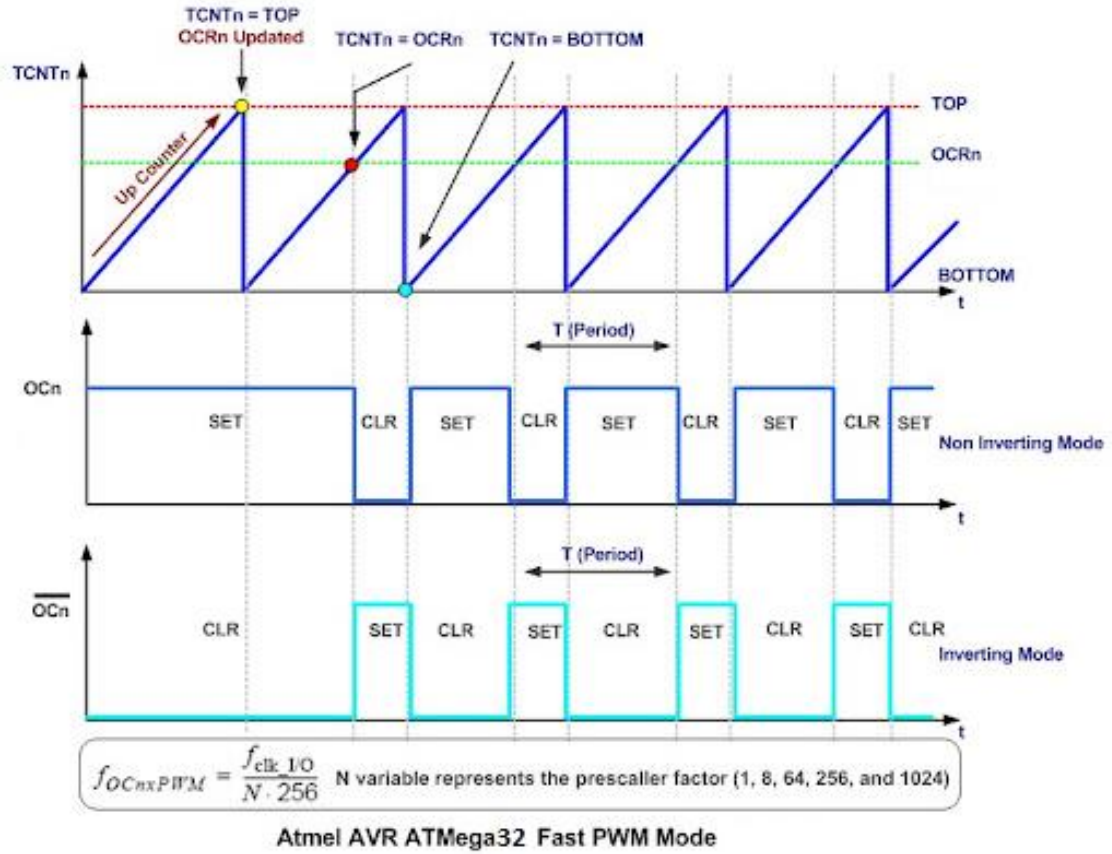
Pulse Width Modulation:

FAST PWM:

- As the shown figure, Fast PWM mode into the Timers, the wave generator will change the value of OCx pin every comparing and the Top of TCNTx.

- As we mentioned, OCx pin will be changed on OCRx value and will be changed again on Top on TCNTx, so we have two modes:
  - Inverted Mode.
  - Non-inverted Mode.

    Let us declare the difference.



Atmel AVR ATMega32 Fast PWM Mode

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Pulse Width Modulation:

FAST PWM:

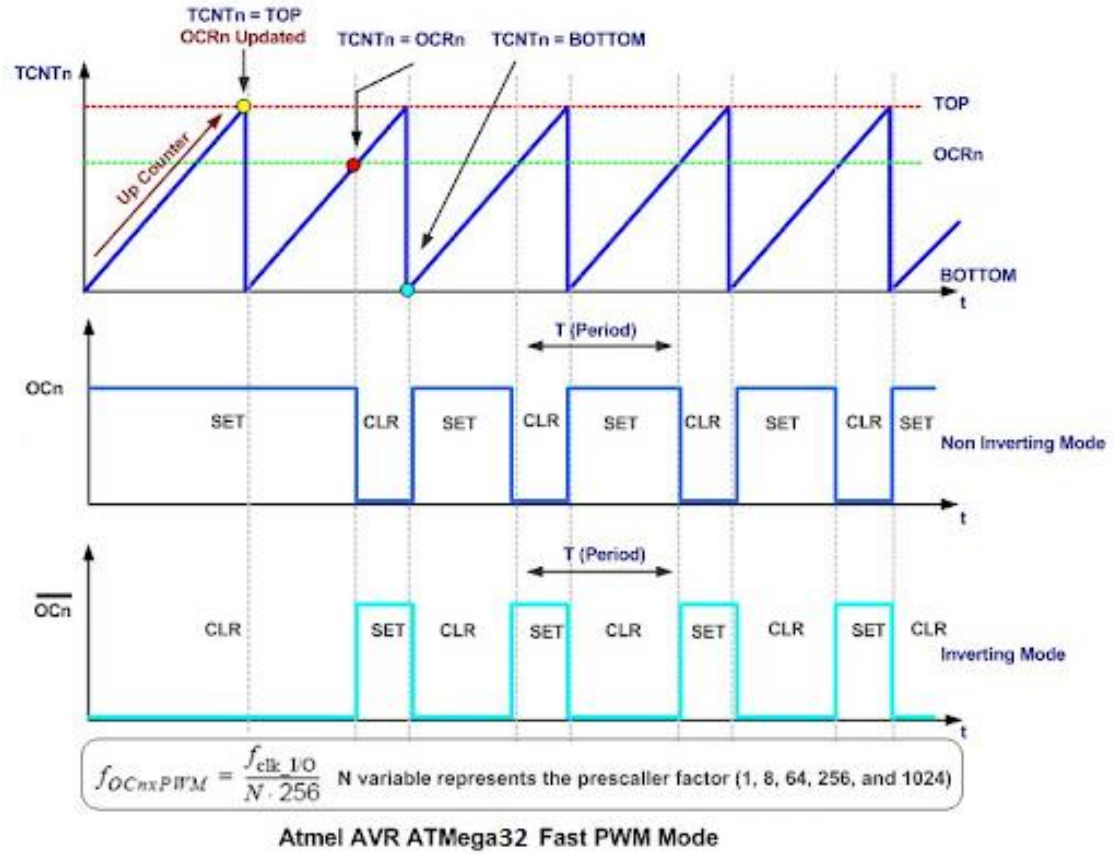
- Non-inverted Mode:

  - In this mode, the action on OCx pin will be clearing the pin on comparing and setting the pin on Top of TCNTx.

  - The Law of Duty Cycle will be:

$$Duty\ Cycle = \frac{OCRx\ value}{Top\ of\ TCNTx+1}$$

  - It is called non-inverted because the relation between OCRx value and the Duty Cycle is non-inverted.



Atmel AVR ATMega32 Fast PWM Mode

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Pulse Width Modulation:

FAST PWM:

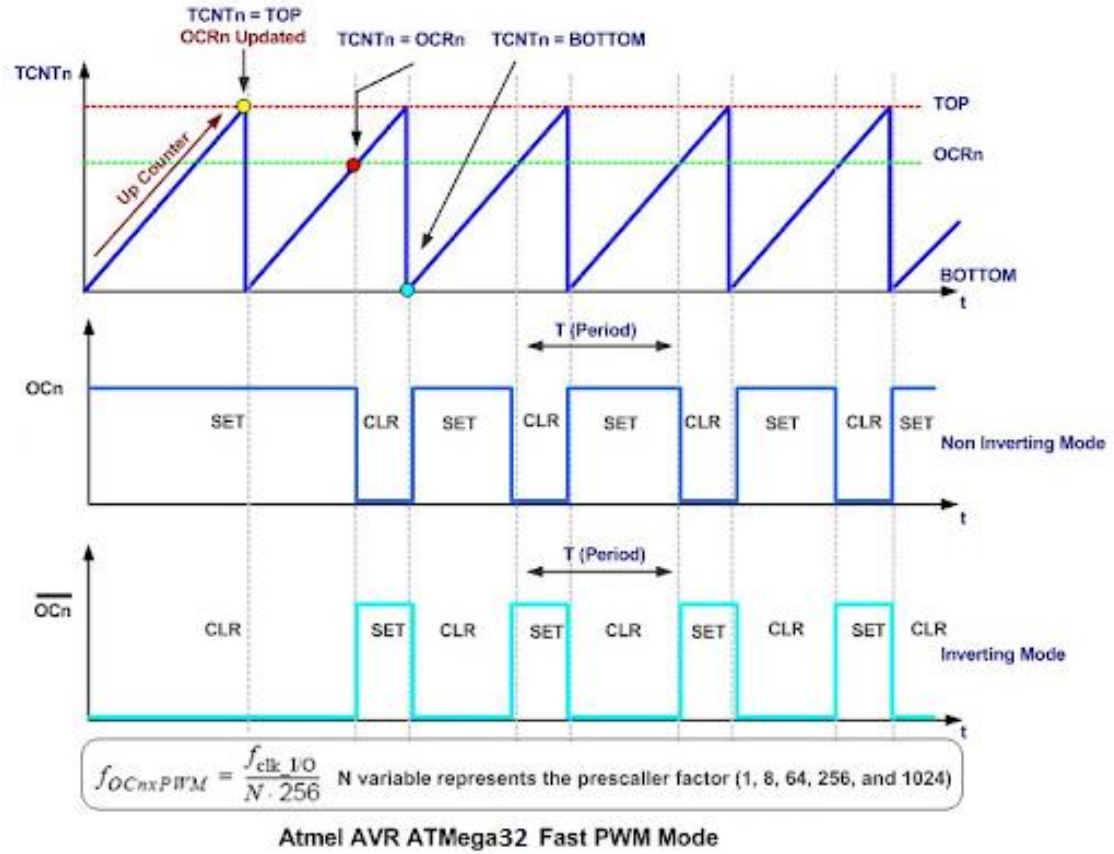
- Inverted Mode:

  - In this mode, the action on OCx pin will be setting the pin on comparing and clearing the pin on Top of TCNTx.

  - The Law of Duty Cycle will be:

$$Duty\ Cycle = \frac{Top\ of\ TCNTx - OCRx\ value}{Top\ of\ TCNTx+1}$$

  - It is called inverted because the relation between OCRx value and the Duty Cycle is inverted.



Atmel AVR ATMega32 Fast PWM Mode

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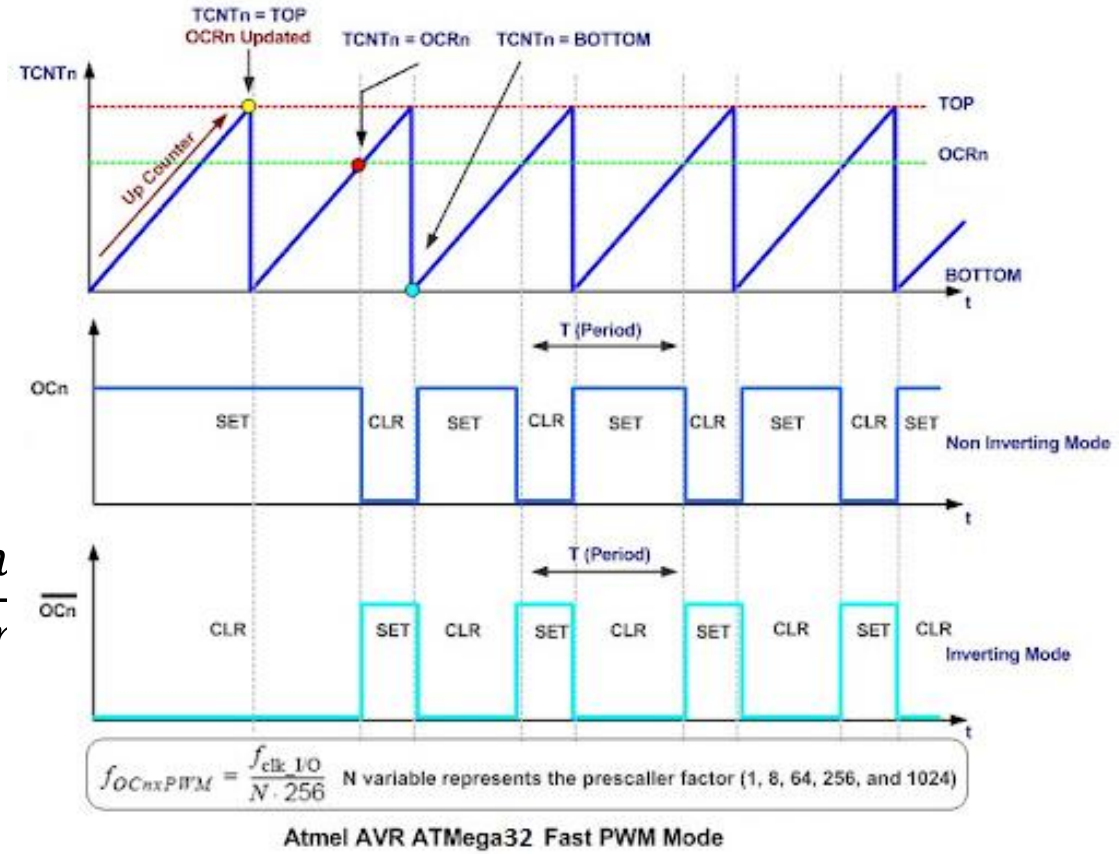
Pulse Width Modulation:

FAST PWM:

- The frequency of this PWM can be calculated by:

$$PWM\ frequency = \frac{frequency\ of\ system}{counts \times prescaler}$$

$$PWM\ frequency = \frac{frequency\ of\ system}{(TOP + 1) \times prescaler}$$



Atmel AVR ATMega32 Fast PWM Mode

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Pulse Width Modulation:

Phase-Correct PWM:

- As we mentioned before in Fast PWM, it is called by fast PWM because the TCNTx is overflowed after reaching it Top, but the phase-correct PWM TCNTx counts down after reaching its Top, so the total counts of this cycle will be double of Top value.

- Because TCNTx counts-up then counts down, it will be compared with OCRx twice “at counting-up and at counting-down”, the action on OCx pin will be taken on OCRx value only.

- OCx pin will be triggered at OCRx value while counting-up, and an inverse triggering on OCx will be taken while counting down.

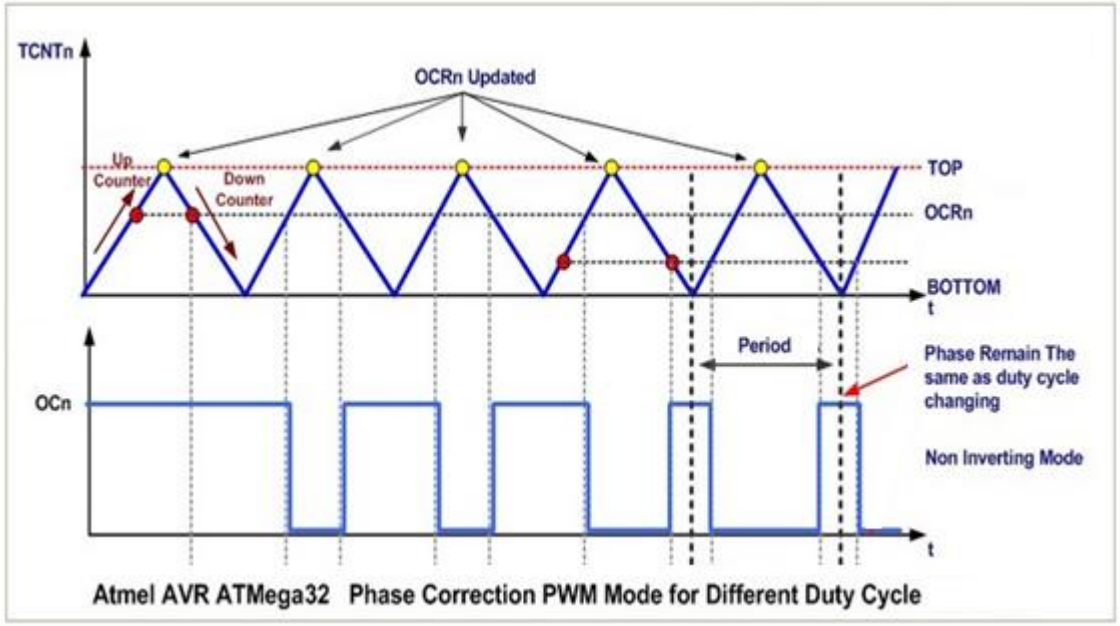
AMIT

Pulse Width Modulation:

Phase-Correct PWM:

- As the shown figure, phase-correct PWM mode into the Timers, the wave generator will change the value of OCx pin every comparing while counting-up and down.

- As we mentioned, OCx pin will be changed on OCRx value twice while counting-up and down, so we have two modes:
  - Inverted Mode.
  - Non-inverted Mode.



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Pulse Width Modulation:

Phase-Correct PWM:

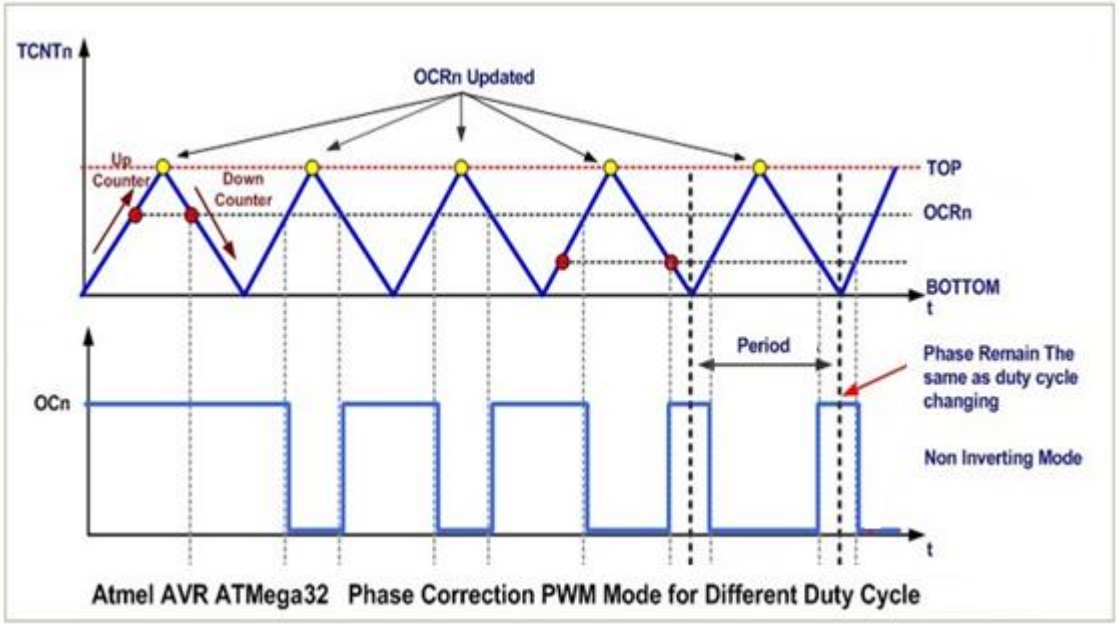
- Non-inverted Mode:

  - In this mode, the action on OCx pin will be clearing the pin while counting-up and setting while counting down.

  - The Law of Duty Cycle will be:

$$Duty\ Cycle = \frac{2 \times OCRx\ value}{2 \times Top\ of\ TCNTx}$$

  - It is called non-inverted because the relation between OCRx value and the Duty Cycle is non-inverted.



Atmel AVR ATMega32 Phase Correction PWM Mode for Different Duty Cycle

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Pulse Width Modulation:

Phase-Correct PWM:

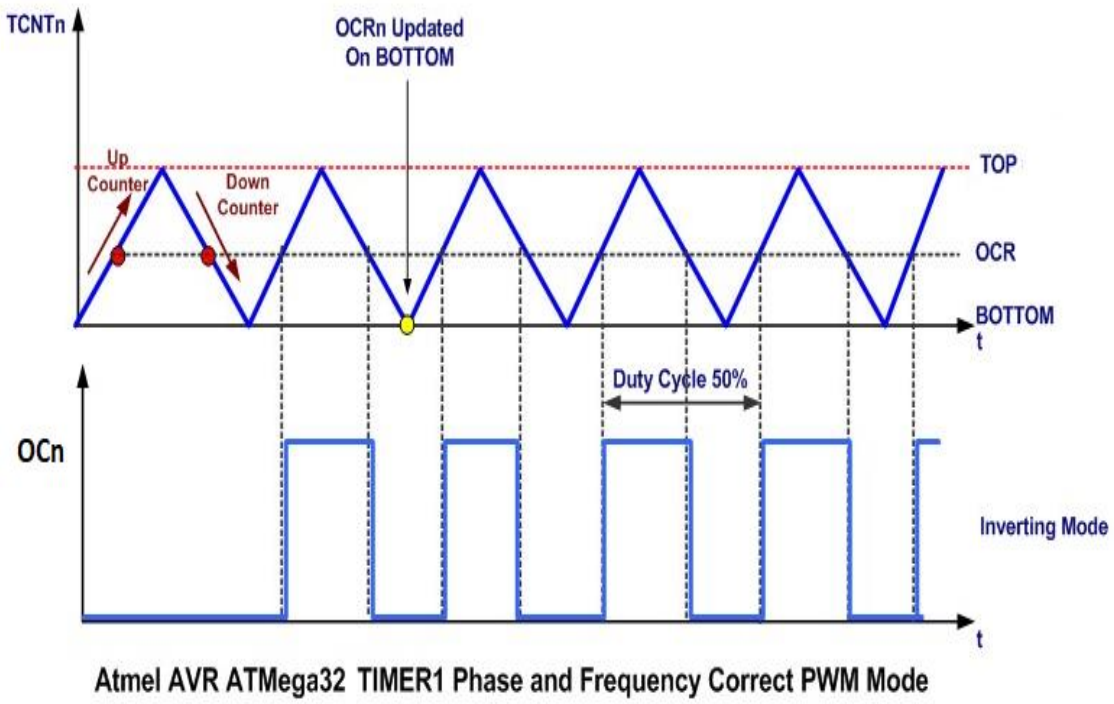
- Inverted Mode:

  - In this mode, the action on OCx pin will be setting the pin while counting-up and clearing while counting down.

  - The Law of Duty Cycle will be:

$$Duty\ Cycle\ = \frac{2 \times Top\ of\ TCNTx - 2 \times OCRx\ value}{2 \times Top\ of\ TCNTx}$$

  - It is called inverted because the relation between OCRx value and the Duty Cycle is inverted.



Atmel AVR ATMega32 TIMER1 Phase and Frequency Correct PWM Mode

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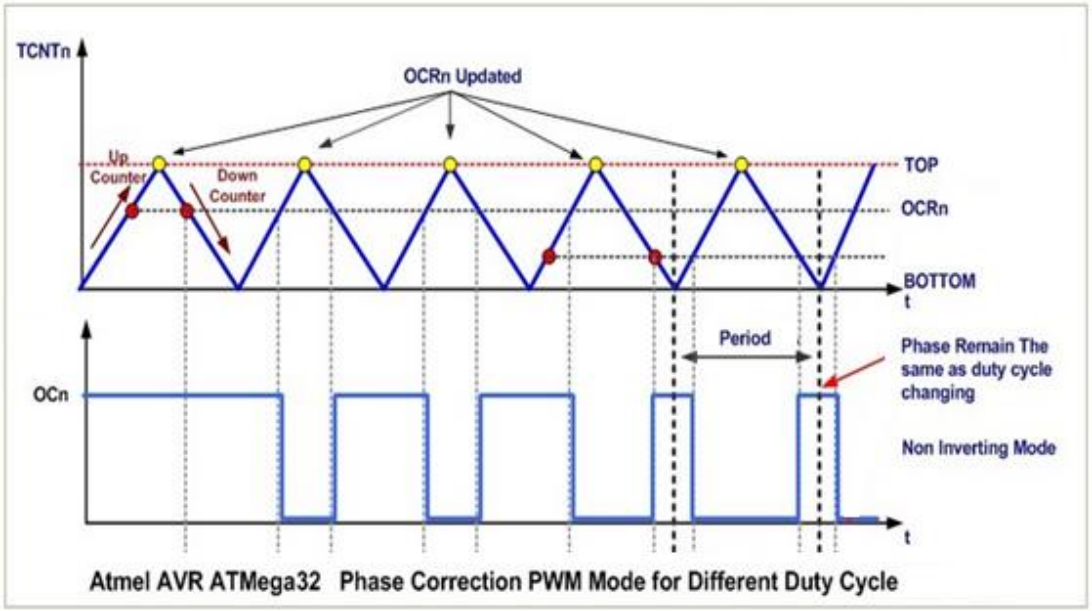
Pulse Width Modulation:

Phase-Correct PWM:

- The frequency of this PWM can be calculated by:

$$PWM\ frequency = \frac{frequency\ of\ system}{counts \times prescaler}$$

$$PWM\ frequency = \frac{frequency\ of\ system}{(2 \times TOP) \times prescaler}$$



Atmel AVR ATMega32 Phase Correction PWM Mode for Different Duty Cycle

Pulse Width Modulation:

How to Configure Timer to generate PWM:

- Configuration of Timer0:

  - from TCCR0, there are two bits "**WGM00, WGM01**", they can be set as:

    - Fast PWM "**11**".
    - Phase-Correct PWM "**01**".

  - Configuration of Mode "Inverted or Non-Inverted" by setting "**COM00, COM01**" bits.

Table 38. Waveform Generation Mode Bit Description[1]

Mode	WGM01 (CTC0)	WGM00 (PWM0)	Timer/Counter Mode of Operation	TOP	Update of OCR0	TOV0 Flag Set-on
1	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
3	1	1	Fast PWM	0xFF	TOP	MAX

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Pulse Width Modulation:

How to Configure Timer to generate PWM:

- Configuration of Timer0:

  - from TCCR0, there are two bits "**WGM00, WGM01**", they can be set as:

    - Fast PWM "**11**".
    - Phase-Correct PWM "**01**".

  - Configuration of Mode "Inverted or Non-Inverted" by setting "**COM00, COM01**" bits.

Table 38. Waveform Generation Mode Bit Description[1]

Mode	WGM01 (CTC0)	WGM00 (PWM0)	Timer/Counter Mode of Operation	TOP	Update of OCR0	TOV0 Flag Set-on
1	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
3	1	1	Fast PWM	0xFF	TOP	MAX

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Pulse Width Modulation:

How to Configure Timer to generate PWM:

- Configuration of Timer0:

  - from TCCR0, there are two bits "**WGM00, WGM01**", they can be set as:
    - Fast PWM "**11**".
    - Phase-Correct PWM "**01**".

Table 38. Waveform Generation Mode Bit Description(1)

Mode	WGM01 (CTC0)	WGM00 (PWM0)	Timer/Counter Mode of Operation	TOP	Update of OCR0	TOV0 Flag Set-on
1	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
3	1	1	Fast PWM	0xFF	TOP	MAX

- Configuration of Mode "Inverted or Non-Inverted" by setting "**COM00, COM01**" bits.

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Pulse Width Modulation:

How to Configure Timer to generate PWM:

- Configuration of Timer0:
  - from TCCR0, there are two bits "**COM00, COM01**" bits which configure the Mode "Inverted or Non-Inverted" PWM:

  - Phase-Correct PWM:
    - "**10**": Non-Inverted.
    - "**11**": Inverted.

Table 41. Compare Output Mode, Phase Correct PWM Mode(1)

COM01	COM00	Description
0	0	Normal port operation, OC0 disconnected.
0	1	Reserved
1	0	Clear OC0 on compare match when up-counting. Set OC0 on compare match when downcounting.
1	1	Set OC0 on compare match when up-counting. Clear OC0 on compare match when downcounting.

  - Fast PWM:
    - "**10**": Non-Inverted.
    - "**11**": Inverted.

Table 40. Compare Output Mode, Fast PWM Mode(1)

COM01	COM00	Description
0	0	Normal port operation, OC0 disconnected.
0	1	Reserved
1	0	Clear OC0 on compare match, set OC0 at TOP
1	1	Set OC0 on compare match, clear OC0 at TOP

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Pulse Width Modulation:

How to Configure Timer to generate PWM:

- Configuration of Timer0:

  - from TCCR0, there are three bits "**CS00, CS01, CS02**" bits which configure the prescaler of division factor:

    - they can be configured as they were configured before when the Timer0 was configured as overflow or comparing match modes.

Table 42. Clock Select Bit Description

CS02	CS01	CS00	Description
0	0	0	No clock source (Timer/Counter stopped).
0	0	1	$clk_{I/O}$/(No prescaling)
0	1	0	$clk_{I/O}$/8 (From prescaler)
0	1	1	$clk_{I/O}$/64 (From prescaler)
1	0	0	$clk_{I/O}$/256 (From prescaler)
1	0	1	$clk_{I/O}$/1024 (From prescaler)
1	1	0	External clock source on T0 pin. Clock on falling edge.
1	1	1	External clock source on T0 pin. Clock on rising edge.

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Pulse Width Modulation:

How to Configure Timer to generate PWM:

- Configuration of Timer0:

  - from OCR0, it is used to set your specific duty cycle if the PWM is inverted or non-inverted.

    - Non-inverted:

      $\text{OCR0} = Duty\ cycle \times Counts$

      $\text{OCR0} = Duty\ cycle \times (TOP + 1)$, if it is fast PWM.

      $\text{OCR0} = Duty\ cycle \times TOP$, if it is phase-correct PWM.

    - Inverted:

      $\text{OCR0} = Duty\ cycle \times Counts$,

      $\text{OCR0} = TOP - Duty\ cycle(TOP + 1)$, if it is fast PWM.

      $\text{OCR0} = TOP \times (1 - Duty\ cycle)$, if it is phase-correct PWM.

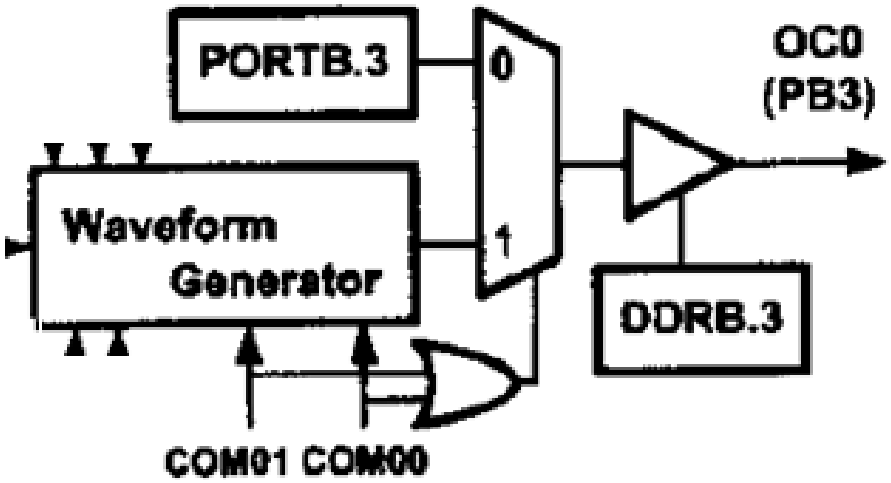
Pulse Width Modulation:

How to Configure Timer to generate PWM:

- Configuration of Timer0:

  - According to this schematic of hardware circuits, OC0 pin must be configured as an output pin to manage the wave generator to control the level of OC0 pin.

  - OC0 pin and PB3 are shared pin, so there is a multiplexer to select the controller of PB3 or OC0.



  - "**COM00, COM01**" are connected on OR gate, so, if these two bits values are zeros, the pin is connected to PORTB and disconnected from wave generator, but if any of them becomes one, the pin is disconnected from PORTB and connected to wave generator.

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Pulse Width Modulation:

Changing of PWM Frequency:

- On Timer0 or Timer2:

$$PWM\ frequency = \frac{frequency\ of\ system}{(255+1)\times prescaler}\ for\ fast\ PWM.$$

$$PWM\ frequency = \frac{frequency\ of\ system}{(2\times 255)\times prescaler}\ \text{for phase-correct PWM.}$$

- The frequency of PWM depends on:
  - System frequency: it depends hardware of microcontroller, so it will be fixed for the same system.
  - Prescaler: it depends hardware clock reduction circuit, it has five or seven options only, so it will be considered a fixed parameter.
  - Counts: here they are fixed, because TCNTx is increased until overflowing.

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Pulse Width Modulation:

Changing of PWM Frequency:

- On Timer0 or Timer2:

  According to the previous, the frequency of PWM in Timer0 or Timer2 will be constant as the following table:

Prescaler	Fast PWM at Timer0/2	Phase-Correct PWM at Timer0/2
1	62,500 Hz	31,372.55 Hz
8	7812.5 Hz	3,921.57 Hz
32	1,953.125 Hz (Timer2 only)	980.39 Hz (Timer2 only)
64	976.5625 Hz	490.20 Hz
128	488.28 Hz (Timer2 only)	245.10 Hz (Timer2 only)
256	244.14 Hz	122.55 Hz
1024	61.04 Hz	30.64 Hz

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Pulse Width Modulation:

Timer 1:

- Modes of Timer1:
  Timer1 is a 16-bit Timer, all registers into it are 16-bit size, it also has four bits for mode configuration.

  It has Two channels of PWM "**OC1A, OC1B**".

  It has an input-capture unit.

  It has about 16 mode as the following table at the next slide:

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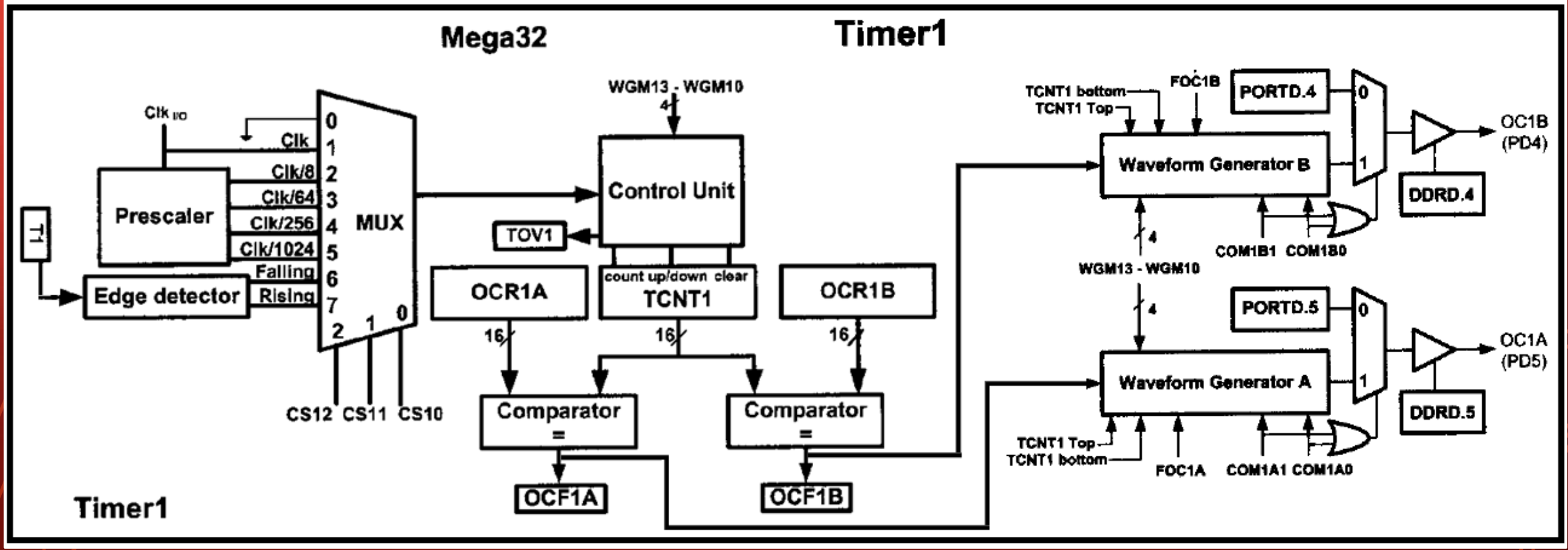
Pulse Width Modulation:

Timer 1:

- Hardware of Timer1:



Pulse Width Modulation:

Timer 1:

Table 47. Waveform Generation Mode Bit Description[1]

Mode	WGM13	WGM12 (CTC1)	WGM11 (PWM11)	WGM10 (PWM10)	Timer/Counter Mode of Operation	TOP	Update of OCR1x	TOV1 Flag Set on
0	0	0	0	0	Normal	0xFFFF	Immediate	MAX
1	0	0	0	1	PWM, Phase Correct, 8-bit	0x00FF	TOP	BOTTOM
2	0	0	1	0	PWM, Phase Correct, 9-bit	0x01FF	TOP	BOTTOM
3	0	0	1	1	PWM, Phase Correct, 10-bit	0x03FF	TOP	BOTTOM
4	0	1	0	0	CTC	OCR1A	Immediate	MAX
5	0	1	0	1	Fast PWM, 8-bit	0x00FF	TOP	TOP
6	0	1	1	0	Fast PWM, 9-bit	0x01FF	TOP	TOP
7	0	1	1	1	Fast PWM, 10-bit	0x03FF	TOP	TOP
8	1	0	0	0	PWM, Phase and Frequency Correct	ICR1	BOTTOM	BOTTOM
9	1	0	0	1	PWM, Phase and Frequency Correct	OCR1A	BOTTOM	BOTTOM
10	1	0	1	0	PWM, Phase Correct	ICR1	TOP	BOTTOM
11	1	0	1	1	PWM, Phase Correct	OCR1A	TOP	BOTTOM
12	1	1	0	0	CTC	ICR1	Immediate	MAX
13	1	1	0	1	Reserved	–	–	–
14	1	1	1	0	Fast PWM	ICR1	TOP	TOP
15	1	1	1	1	Fast PWM	OCR1A	TOP	TOP

Pulse Width Modulation:

Timer 1:

- Normal: “**0000**”
  it is the overflow mode like Timer0/2, but it is overflowed after its Top “**65,535**”.

- PWM, Phase-Correct “**8-bit**”: “**0001**”
  it is phase-correct mode exactly like Timer0/2, with any difference between of them.

- PWM, Phase-Correct “**9-bit**”: “**0010**”
  it is phase-correct mode exactly like Timer0/2, but the difference between of them is that the top of Timer1 is “**511**”.

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Pulse Width Modulation:

Timer 1:

- PWM, Phase-Correct “**10-bit**”: “**0011**”
  it is phase-correct mode exactly like Timer0/2, but the difference between of them is that the top of Timer1 is “**1023**”.

- CTC, Comparing Match “**OCR1A**”: “**0100**”
  it is compare time mode exactly like Timer0/2, but the comparing occurs only when TCNT1 equals OCR1A,
  “**Compares only with Channel A only**”.

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Pulse Width Modulation:

Timer 1:

- PWM, Fast PWM “**8-bit**”: “**0101**”
  it is Fast PWM mode exactly like Timer0/2, with any difference between of them.

- PWM, Fast PWM “**9-bit**”: “**0110**”
  it is Fast PWM mode exactly like Timer0/2, but the difference between of them is that the top of Timer1 is “**511**”.

- PWM, Fast PWM “**10-bit**”: “**0111**”
  it is Fast PWM mode exactly like Timer0/2, but the difference between of them is that the top of Timer1 is “**1023**”.

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Pulse Width Modulation:

Timer 1:

- PWM, Phase-Correct “**ICR1**”: “**1000**”
  it is phase-correct mode exactly like Timer0/2, but the difference between of them is that the top of Timer1 is the value of input-capture register “**ICR1**”, the triggering event will be occurred on “OCR1” and “OCR1B” which the two channels will run at the same frequency if their values are less than the value of “ICR1”.

- PWM, Phase-Correct “**OCR1A**”: “**1001**”
  it is phase-correct mode exactly like Timer0/2, but the difference between of them is that the top of Timer1 is the value of output-comparing register A “**OCR1A**”, the triggering event will be occurred on “OCR1B”,if “OCR1B” value is less than the value of “OCR1A”.

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Pulse Width Modulation:

Timer 1:

- PWM, Phase-Correct "**ICR1**": "**1010**"
- PWM, Phase-Correct "**OCR1A**": "**1011**"
  they are identically similar to the two-previous modes, but the only difference between of them that into these mode the updating of OCR1A/ICR1 "**we will discuss it later**" occurs on the Top of TCNT1, but the previous mode the updating of OCR1x occurs on the Bottom of TCNT1.
- CTC, Comparing Match "**ICR1**": "**1100**"
  it is compare time mode exactly like Timer0/2, but the difference between of them is that the top of Timer1 is the value of input-capture register "**ICR1**", the comparing match will be occurred on "OCR1" and "OCR1B", if their values are less than the value of "ICR1" on which TCNT1 will be zeroized.

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Pulse Width Modulation:

Timer 1:

- PWM, Fast PWM "**ICR1**": "**1110**"
  it is Fast PWM mode exactly like Timer0/2, but the difference between of them is that the top of Timer1 is the value of input-capture register "**ICR1**", the triggering event will be occurred on "OCR1" and "OCR1B" which the two channels will run at the same frequency if their values are less than the value of "ICR1".

- PWM, Fast PWM "**OCR1A**": "**1111**"
  it is Fast PWM mode exactly like Timer0/2, but the difference between of them is that the top of Timer1 is the value of output-comparing register A "**OCR1A**", the triggering event will be occurred on "OCR1B",if "OCR1B" value is less than the value of "OCR1A".

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Pulse Width Modulation:

Changing of PWM Frequency:

- On Timer1:

  there are about twelve modes to generate a PWM into Timer1:

  - PWM, fast or phase correct **"8 / 9 / 10 bit"**, these modes have a fixed frequencies like timer0/2 at every value of prescaler.

  - PWM, fast or phase correct "**ICR1 , OCR1A**", these modes allow the user to assign any value of counts into "**ICR1 or OCR1A**", so now we can generate any frequency by calculating the required value to generate this frequency.

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Pulse Width Modulation:

Changing of PWM Frequency:

- Frequency Law:

$$PWM\ frequency = \frac{frequency\ of\ system}{Counts \times prescaler}$$

- Frequency of Fast PWM Law:

$$PWM\ frequency = \frac{frequency\ of\ system}{Top \times prescaler}$$

- Frequency of phase-correct Law:

$$PWM\ frequency = \frac{frequency\ of\ system}{(2 \times Top) \times prescaler}$$

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Pulse Width Modulation:

Changing of PWM Frequency:

- The new top “counts” for Fast PWM mode:

$$\mathbf{OCR1A} \text{ or } \mathbf{ICR1} = \frac{frequency\ of\ system}{PWM\ frequency\ required \times prescaler}$$

- The new top “counts” for Phase-Correct PWM mode :

$$\mathbf{OCR1A} \text{ or } \mathbf{ICR1} = \frac{frequency\ of\ system}{2 \times PWM\ frequency\ required \times prescaler}$$

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Pulse Width Modulation:

Updating of OCRx / ICR1 Registers into PWM modes:

- The updating of OCRx/ICR1 register differs according to the Timer if it was overflow/compare-match or fast/phase-correct.

- The updating of OCRx/ICR1 at overflow/compare-match modes is immediately occurred.

- The updating of OCRx/ICR1 at fast/phase-correct PWM modes is commonly occurred at the Top value of TCNTx except the "**1000 , 1001**" modes at Timer1, the updating is occurs at the bottom of TCNT1.

but, how can the updating be delayed until the top/bottom of TCNTx?

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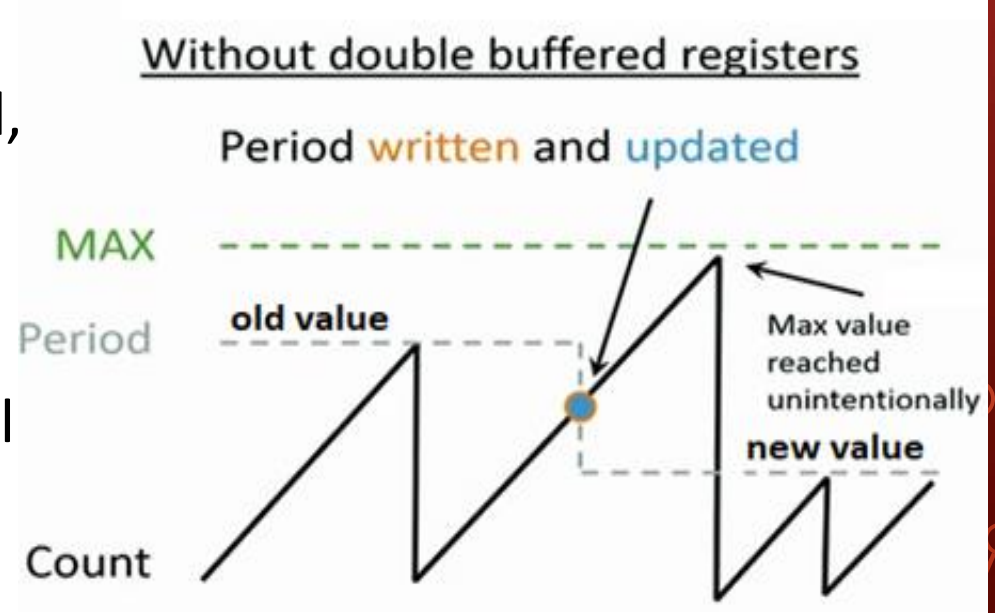
Pulse Width Modulation:

Updating of OCRx / ICR1 Registers into PWM modes:

- The OCRx/ICR1 registers in general are double-buffered registers, the double-buffered register save the updated value into it until the TCNTx reaches its Top, then it will copied to OCRx/ICR1 by hardware.

- If these registers are not a doubled-buffered, the following scenario will be occurred, Like the following figure, the updating occurs when TCNTx becomes higher than the new value that be updated, so the comparing will not be occurred and the TCNTx will be overflowed.



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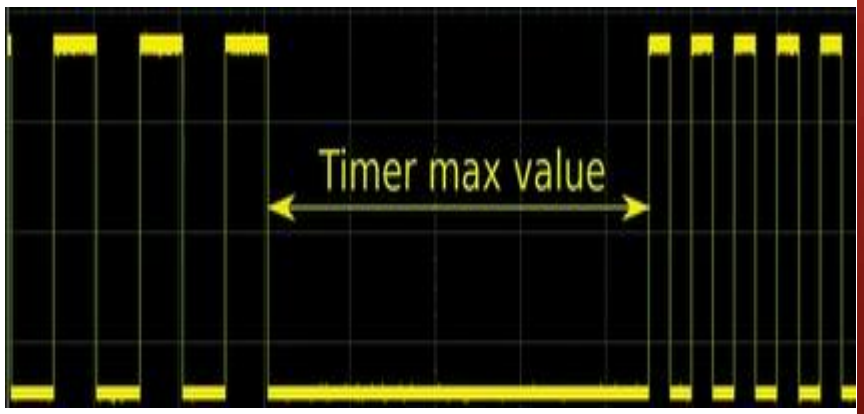
Pulse Width Modulation:

Updating of OCRx / ICR1 Registers into PWM modes:

- According to the previous, the PWM will contain a stretching cycle into it like the following figure.



- So, This mechanism of double-buffered allows to avoid generating a sudden stretching within the sequence of PWM cycles,
  like the following figure.

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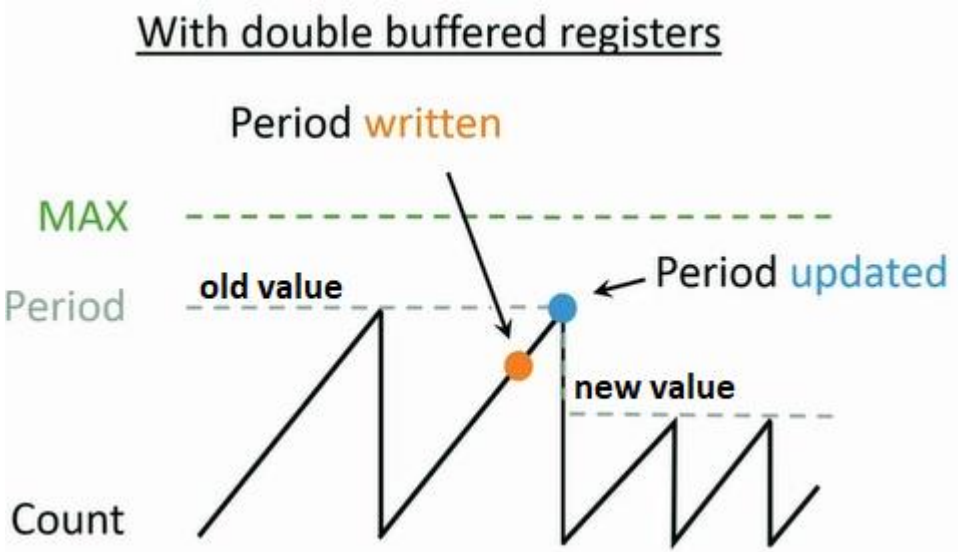
Pulse Width Modulation:

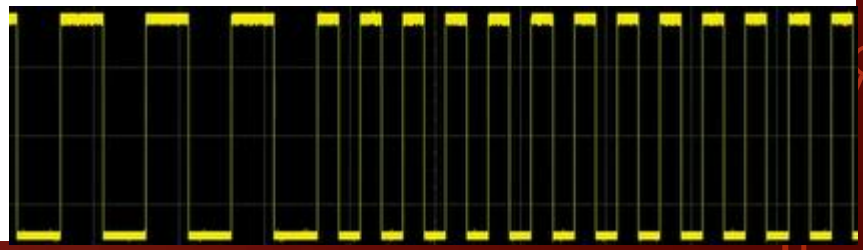
Updating of OCRx / ICR1 Registers into PWM modes:

- So, when the double-buffered mechanism is used, the TCNTx register will not be overflowed like the previous mechanism.



- It is the same if the updating occurs at the bottom of TCNTx, the main reason to use it is avoiding updating while running by a value when TCNTx may has a higher value than it because it will cause an overflow.

- The output PWM after using the double-buffered do not contain a stretched clock.



Pulse Width Modulation:

Accessing the 16-bit registers:

- The TCNT1, OCR1A/B, and ICR1 are 16-bit registers that can be accessed by the AVR CPU via the 8-bit data bus.
- The 16-bit register must be accessed byte-wise, using two read or write operations.
- Each 16-bit timer has a single 8-bit TEMP register for temporary storing of the high byte of the 16-bit access.
- The same temporary register is shared between all 16-bit registers within each 16-bit timer.

Pulse Width Modulation:

Accessing the 16-bit registers:

- Accessing the low byte triggers the 16-bit read or write operation:
  - When the low byte of a 16-bit register is written by the CPU, the high byte that is currently stored in TEMP
  - When the low byte being written, both are copied into the 16-bit register in the same clock cycle.
  - When the low byte of a 16-bit register is read by the CPU, the high byte of the 16-bit register is copied into the TEMP register in the same clock cycle as the low byte is read, and must be read subsequently.

PWM Driver:

Time To Code

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THANK YOU!