SAP_1 data sheet

First step

You put the (clk) signal in clock mode and set the (clr) signal to high to make sure the PC-program counter-clear and point to the first instruction and the SC-sequence counter-to the first step (T0) .

Second step

set the (clr) signal to low in order to make the program start.

what the program do

- It could sum or subtract two operands that you already store in the memory before the program starts.

- Data can be presented in an output register which can then be used to show it in seven segments.

- After the program ends its operations, it stops and gives you the output data whatever the clock-clk- positive edge or negative one.

As example of what this architecture do we chose program that

LAD &09	AC ← M[09]
Sum AC, &A -- D10	AC ← AC+M[10]
Out AC	S_out← AC
Sub AC, &B -- D11	AC←AC-M[11]
Out AC	S_out← AC
HLT	active_clk← 1 stop the clock

In Math >> 1st output=3+4=7 2nd output =7-4=5

Note

There is a data sheet for control unit that have all required truth tables that could help in understanding the control signals and bus.