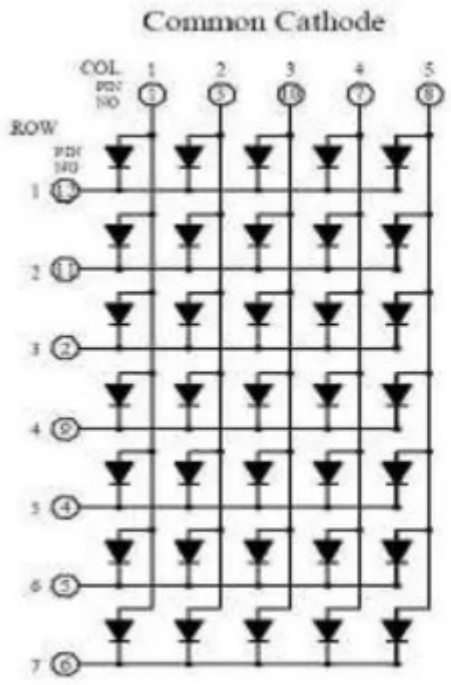
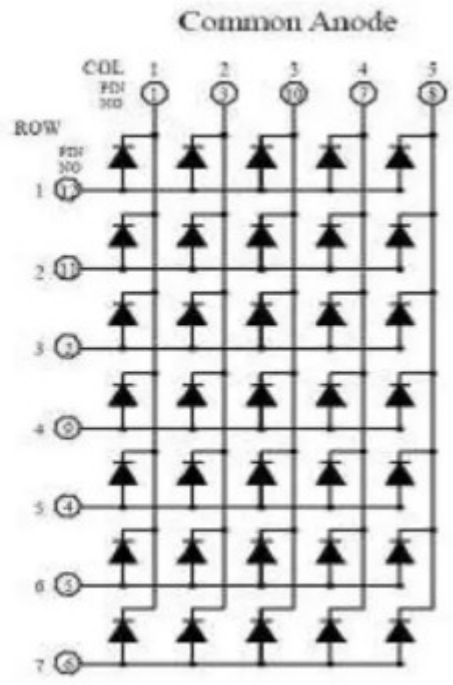
DOT MATRIX

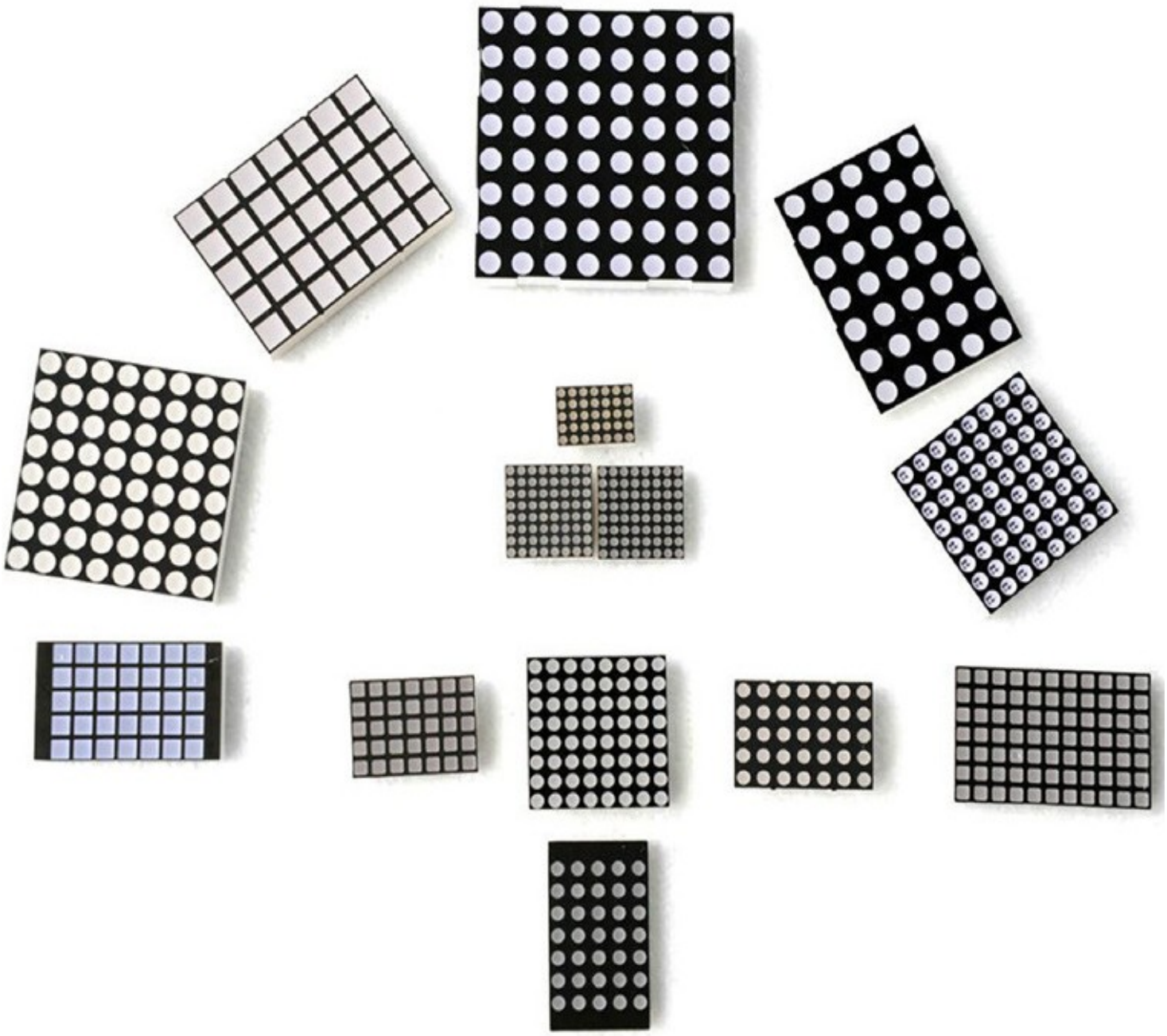
- Internally, the LEDs are organized in a matrix.
  - Here's a 5x7 display internal wiring.
- Dot Matrix has two types:
  - Common Cathode Type:
    - a common anode for LEDs in a row - all of the anodes in each row is common
  - Common Anode Type:
    - a common cathode for LEDs in a row – all the cathodes ir each row is common.



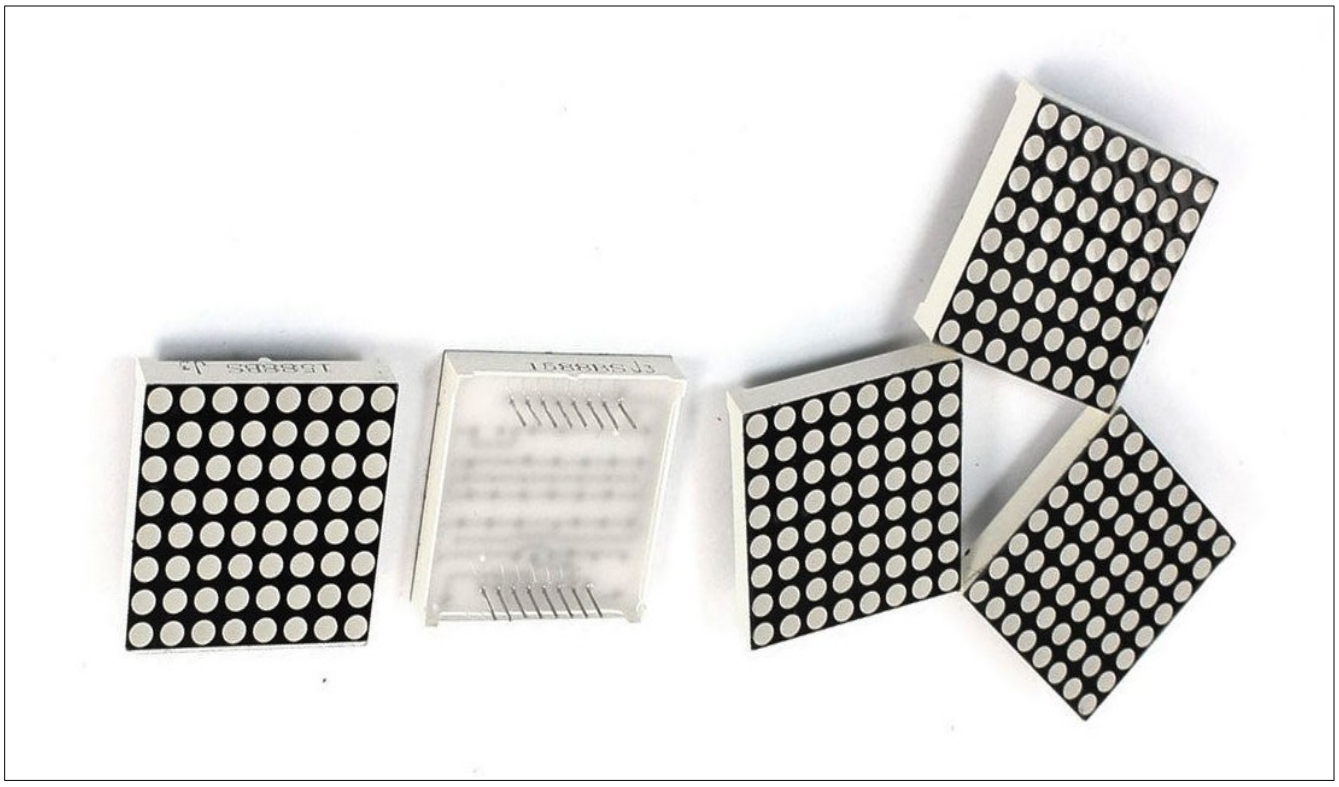


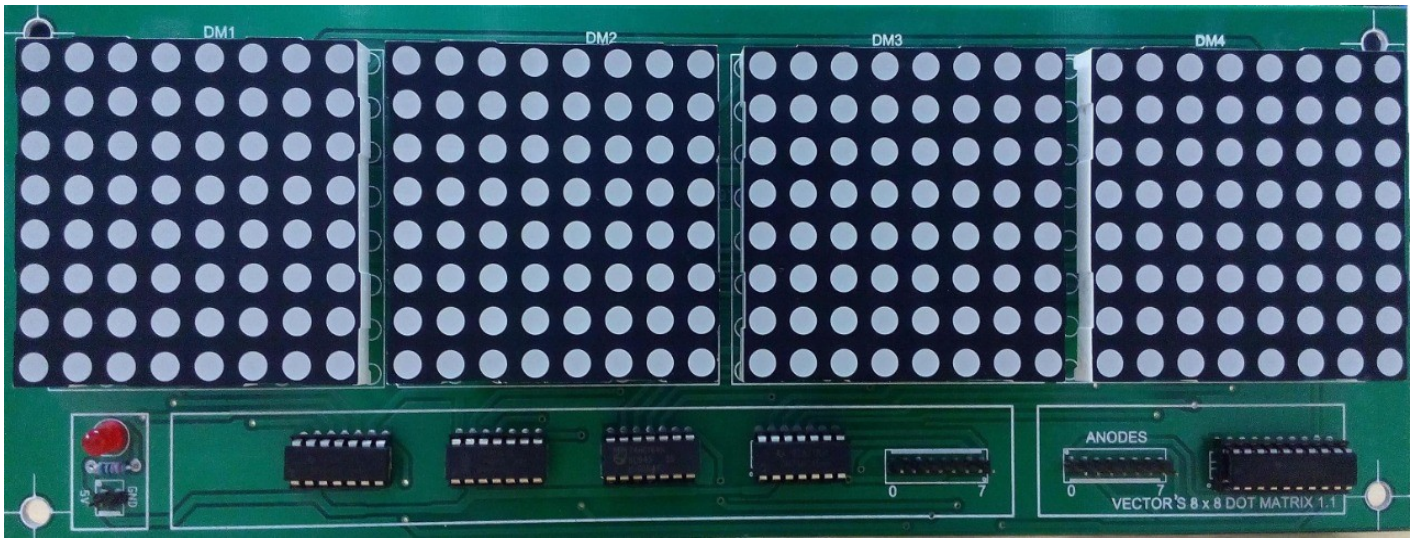

2:45:13


Thur
13:16:36
2020.1.12

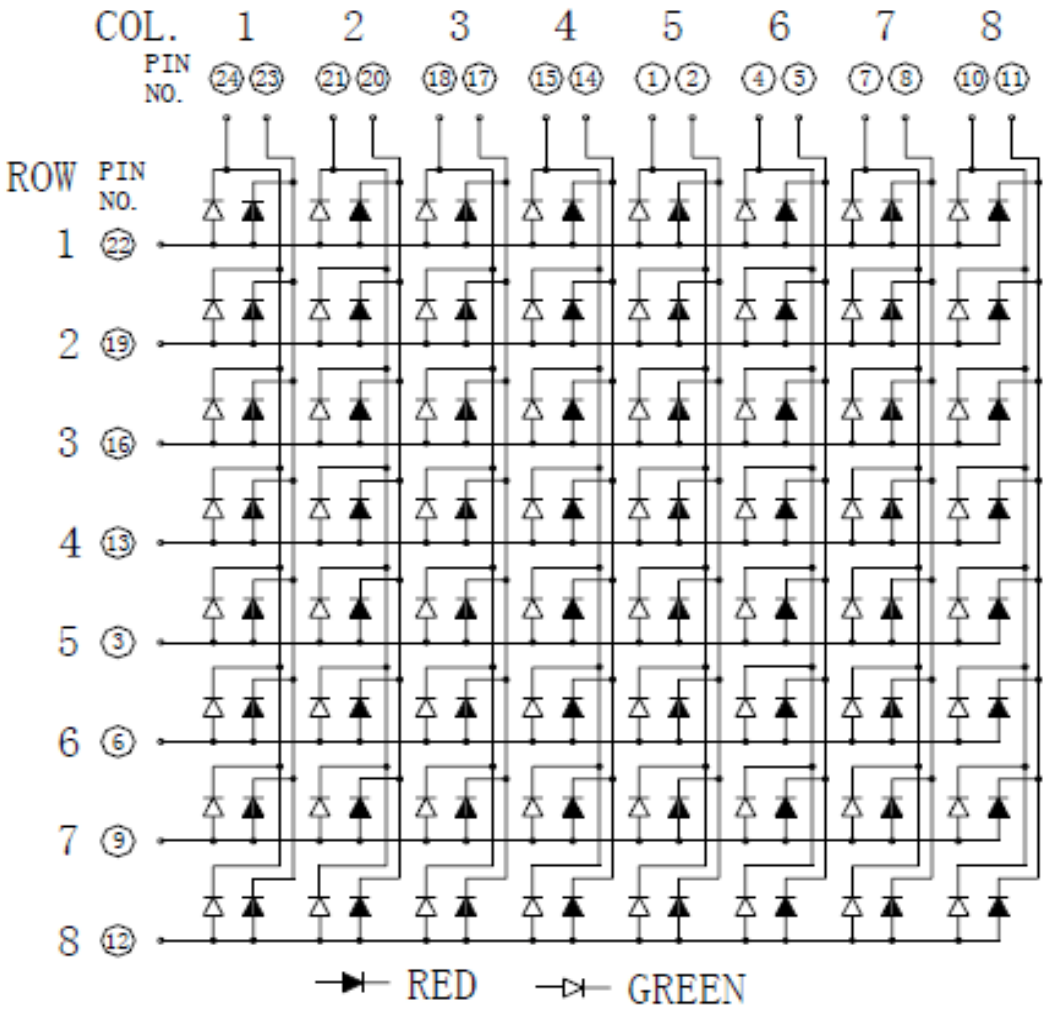


8*8 DOT MATRIX

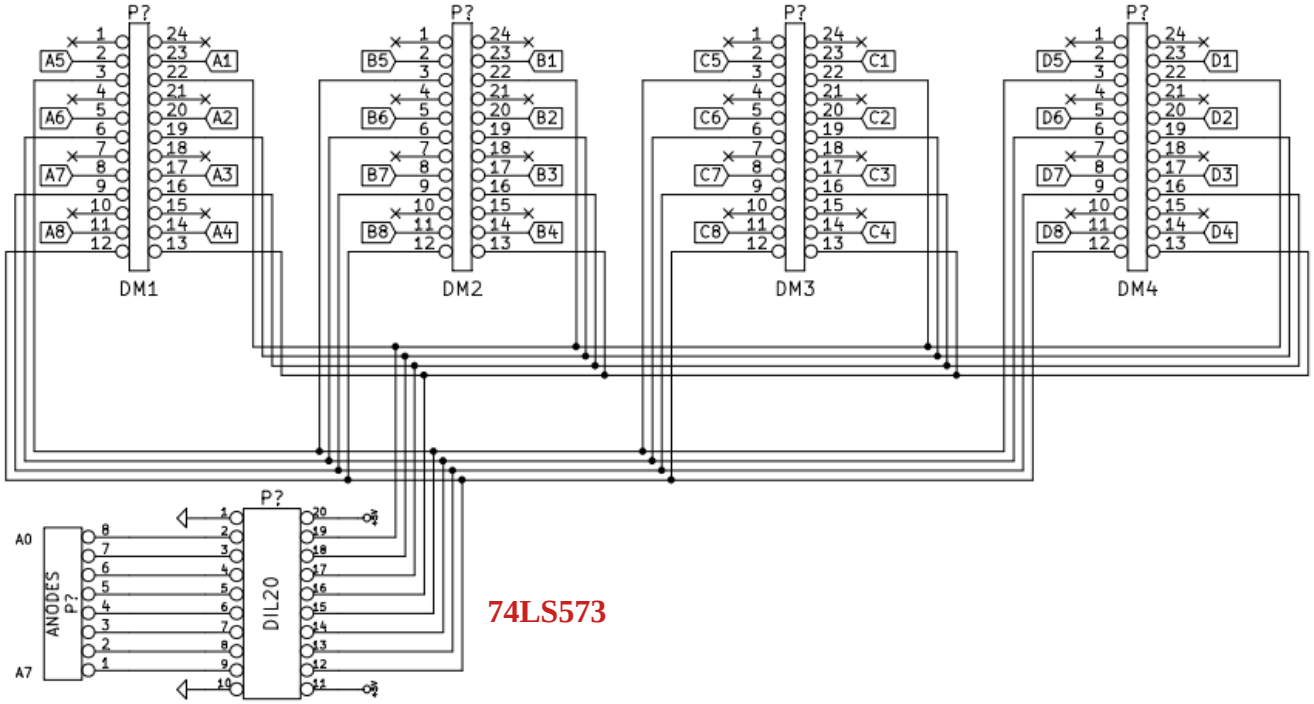




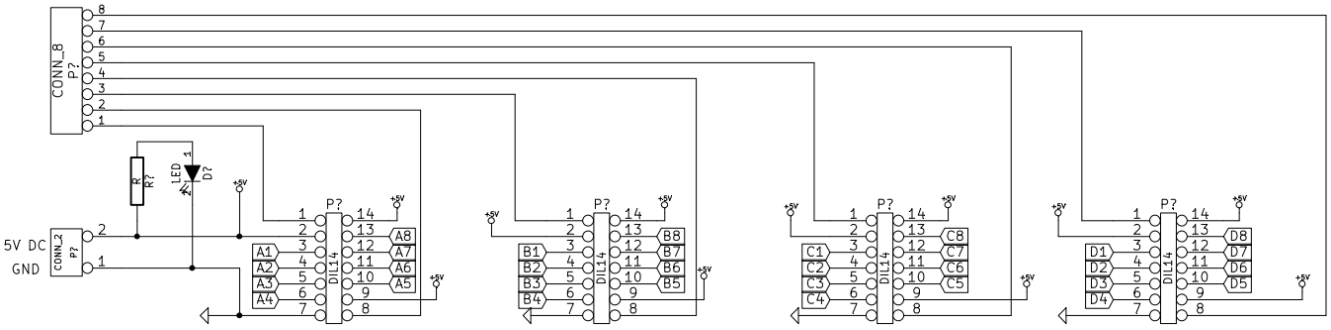
INTERNAL CIRCUIT :



SCHEMATIC



74LS573



74LS164

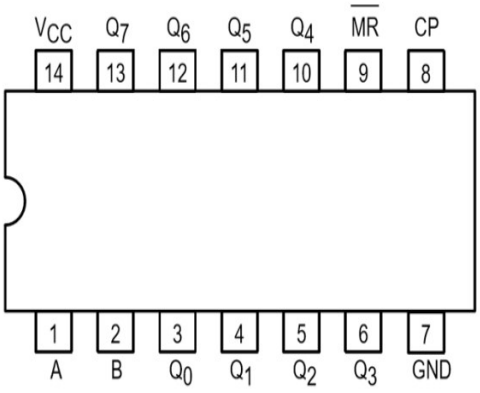
74LS164

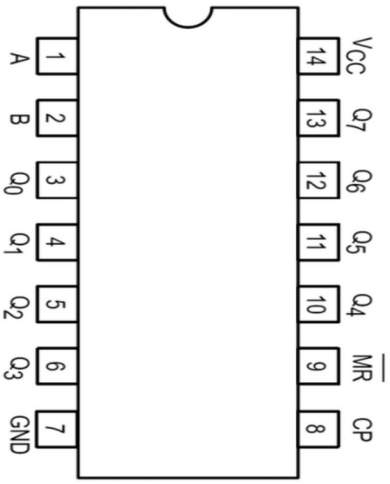
The 74LS164 is a high speed 8-Bit Serial-In Parallel-Out Shift Register. Serial data is entered through a 2-Input AND gate synchronous with the LOW to HIGH transition of the clock. Master Reset which clears the register setting all outputs LOW independent of the clock.

FUNCTIONAL DESCRIPTION:

The 74LS164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH, or both inputs connected together.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q0 the logical AND of the two data inputs (A•B) that existed before the rising clock edge. A LOW level on the Master Reset (MR) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW





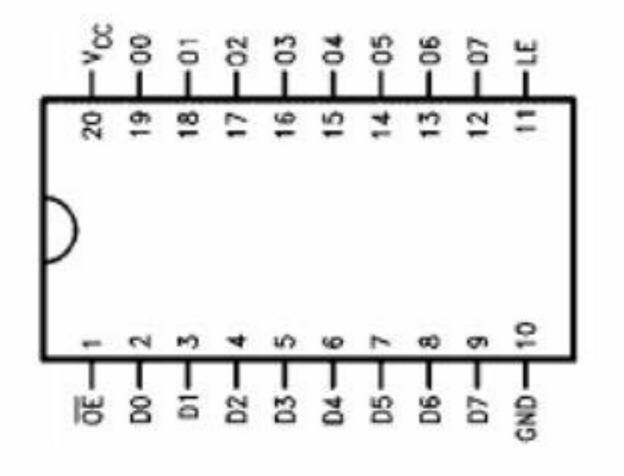
74LS573

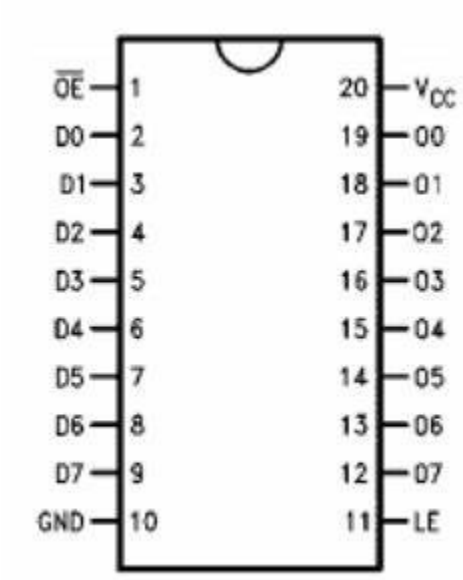
General Description :

The 74LS573 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (OE) inputs.

Features :

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Fully TTL and CMOS compatible





THANK YOU