Abdul Muneeb

Toronto | Canada

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Objective

Experienced ASIC Design Engineer with a strong background in RTL design, verification, synthesis, timing closure, and physical design. Passionate about developing high-performance digital designs and driving innovation in display technologies.

Research Experience and Employment

Senior ASIC Design Engineer **Mar/2025 – Present**
Nokia **Ottawa, Canada**

- Design and optimize low-power DSP components for next-gen optical network ASICs.
- Perform RTL development and synthesis for power-efficient optical transport solutions.

Digital Design Engineer **Sep/2022 – Mar/2024**
Neuro-IC Lab, York University **Toronto, Canada**

- Developed and optimized RTL designs for energy-efficient digital processing.
- Designed and implemented micro-architecture based on high-level design requirements.
- Performed functional verification and ensured design meets functionality, performance, power, and area constraints.
- Defined and resolved timing issues, including STA analysis and timing closure.
- Executed pre- and post-layout validation and resolved eco-related issues.

Digital Design Engineer **April/2021 – Sep/2022**
IC Design Lab, LUMS **Lahore, Pakistan**

- Designed and verified ASIC IPs for biomedical applications.
- Developed micro-architecture and RTL implementations using Verilog/SystemVerilog.
- Conducted synthesis, timing analysis, and formal verification to ensure design closure.
- Collaborated with architects and verification engineers to resolve functional and performance issues.
- Led test plan development and functional validation of critical IP blocks.

Associate Design Engineer **October/2019 – May/2021**
Lampro Mellon **Lahore, Pakistan**

- Designed RTL modules for multi-clock domain digital systems.
- Performed functional verification using SystemVerilog and UVM methodology.
- Conducted synthesis, STA, and formal verification to meet timing constraints.
- Developed scalable and testable display technology IPs for video processing.
- Resolved ECO-related issues and contributed to improving chip performance and reliability.

Technical Skills

- **Hardware Design:** RTL design, micro-architecture, Verilog, SystemVerilog, timing closure, synthesis.
- **Verification:** Functional verification, UVM, formal verification, testbench development.

- **Tools:** Cadence Innovus, Synopsys VCS/DC/PT, Xilinx Vivado, OpenSTA, Magic VLSI.
- **Interface Protocols:** AHB-Lite, TileLink, Wishbone, PCIe.
- **Programming:** Python, C, RISC-V Assembly, Tcl, Makefile.
- **Methodologies:** Agile development, test plan execution, code reviews, sprint planning.

Education

M.A.Sc. Electrical and Computer Engineering (CGPA 3.93/4.0) **Sep/2022 – Dec/2024**
York University **Toronto, Canada**
Thesis: Energy-efficiency-optimized convolutional spiking neural networks for patient-specific seizure detection

B.Sc. Electronic Engineering (CGPA 3.58/4.00) **Sep/2015 – June/2019**
The Islamia University of Bahawalpur **Bahawalpur, Pakistan**

Certifications & Achievements

- **Best Thesis Award Nominee** for research on low-power neuromorphic processors
- **Most Interesting Research Award** at Industrial Night, YorkU
- Provided "**Cadence EDA Tools Training**" at the University of Engineering and
- Technology(UET) Lahore
- **Certified** in Cadence Design Systems Innovus Block Level Implementation Training
- **Certified** in Innovus Clock Concurrent Optimization for Clock Tree Synthesis Training
- **Tapeout Experience:** Successfully contributed to ASIC designs at 45nm and 180nm nodes.
- Served as **President** of the **IEEE** student chapter at The Islamia University of Bahawalpur

Research Publications

A. Muneeb, and H. Kassiri, "Customized Development and Hardware Optimization of a Fully-Spiking SNN" IEEE Biomedical Circuits and Systems Conference **(BioCAS)**, 2024.

H. Kassiri, **A. Muneeb**, R. Salahi, and A. Dabbaghian, "Closed-Loop Implantable Neurostimulators for Individualized Treatment of Intractable Epilepsy: A Review of Recent Developments, Ongoing Challenges, and Future Opportunities," IEEE Transactions on Biomedical Circuits and Systems, (**TBioCAS**), 2024.

A. Muneeb, S. Mehrotra, and H. Kassiri, "A 9.5ms-Latency 6.2μJ/Inference Spiking CNN for Patient-Specific Seizure Detection" IEEE Biomedical Circuits and Systems(**BioCAS**), 2023.

A. Muneeb, and H. Kassiri, "Energy-Efficient Spiking-CNN-Based Cross-Patient Seizure Detection" IEEE International Symposium on Circuits and Systems(**ISCAS**), 2023.

A. Muneeb, M. Ali, and M. A. Altaf, "A 2.7μJ/Classification Machine-Learning Based Approximate Computing Seizure Detection SoC" IEEE International Symposium on Circuits and Systems(**ISCAS**), 2022.

A. Muneeb, M.Ali, and M. A. Altaf, "A 0.82μJ/Classification Difference of Dual Differential Channel-based Approximate Computing Machine Learning SoC for Seizure Onset Detection" **(IEEE TBioCAS) (Submitted)**

References

Dr. Hossein Kassiri
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