

KernelGen – A prototype of auto-parallelizing Fortran/C compiler for NVIDIA GPUs

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KernelGen compiler project

Goals:

- Conserve the original application source code, keep all GPU-specific things in the background
- Minimize manual work on specific code ⇒ develop a compiler toolchain usable with many existing computational applications

Rationale:

- Old good programming languages could still be usable, if accurate code analysis & parallelization methods exist
- OpenACC is too restrictive for complex apps and needs more flexibility
- GPU tends to become a central processing unit in near future, contradicting with OpenACC paradigm

Simple example: Fortran

```
program demo
     integer :: argc, nx, nv, ns
     character(len=32) :: arg
     real, allocatable, dimension(:.:.) :: x, y, xy
     real :: start, finish
    ! Read arguments
     call get_command_argument(1, arg)
    read(arg, '(I32)') nx
    call get command argument(2, arg)
    read(arg, '(I32)') ny
    call get command argument(3, arg)
     read(arg, '(I32)') ns
16
    ! Allocate data arrays.
     allocate(x(nx.nv.ns), v(nx.nv.ns), xv(nx.nv.ns))
18
     ! Initialize arrays.
    x = atan(1.0)
    v = x
```

```
! Computational loop
call cpu time(start)
                                                                   24
                                                                   25
do k = 1, ns
 do j = 1, nv
   do i = 1, nx
     xy(i,j,k) = asin(sin(x(i,j,k))) + acos(cos(y(i,j,k)))
   enddo
 enddo
                                                                   30
enddo
call cpu time(finish)
write(*.*) 'compute time = '. finish - start
                                                                   34
                                                                   35
write(*.*) 'maxval = '. maxval(xv). &
                                                                   36
 'minval = '. minval(xv)
                                                                   38
! Deallocate arrays.
                                                                   39
                                                                   40
deallocate(x, y, xy)
                                                                   41
end program demo
                                                                   47
```

Simple example: Fortran

Compile the Fortran example as usual, just use kernelgen-gfortran instead of gfortran:

```
$ kernelgen-gfortran -03 example_f.f90 -o example_f
```

KernelGen always generates binaries usable both on CPU and GPU. To execute the regular version, run it as usual:

```
$ ./example_f 512 256 256

compute time = 1.8481150

maxval = 1.5707963 minval = 1.5707963
```

In order to run GPU-accelerated version, simply set kernelgen_runmode environment variable to 1:

```
$ kernelgen_runmode=1 ./example_f 512 256 256
compute time = 0.28801799
maxval = 1.5707964 minval = 1.5707964
```

Simple example: C

```
#include <malloc.h>
     #include <math.h>
     #include <stdio.h>
     #include <stdlib.h>
     #include <sys/time.h>
 6
     int main(int argc, char* argv[]) {
 9
     int nx = atoi(argv[1]);
     int ny = atoi(argv[2]);
     int ns = atoi(argv[3]):
     size_t szarray = nx * ny * ns;
14
     size t szarravb = szarrav * sizeof(float);
16
     float* x = (float*)malloc(szarravb);
     float* v = (float*)malloc(szarravb);
     float* xv = (float*)malloc(szarravb):
     for (int i = 0: i < szarray: i++)</pre>
       x[i] = atan(1.0);
       v\Gamma i  = x\Gamma i  :
     struct timeval start, finish:
```

```
gettimeofday(&start, NULL);
for (int k = 0: k < ns: k++)
  for (int j = 0; j < nv; j++)
    for (int i = 0: i < nx: i++)
      int idx = i + nx * (i + nv * k):
      xv[idx] = asinf(sinf(x[idx])) + acosf(cosf(v[idx]));
gettimeofday(&finish, NULL):
printf("compute time = %f\n",
  get time diff(&start, &finish));
float minval = xy[0], maxval = xy[0];
for (int i = 0: i < szarray: i++)</pre>
  if (minval > xv[i]) minval = xv[i]:
  if (maxval < xv[i]) maxval = xv[i];</pre>
printf("maxval = %f, minval = %f\n", maxval, minval):
// Deallocate arrays.
free(x): free(v): free(xv):
return 0:
```

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Simple example: C

Compile the Fortran example as usual, just use kernelgen-gcc instead of gcc:

```
$ kernelgen-gcc -03 -std=c99 example_c.c -o example_c
```

KernelGen always generates binaries usable both on CPU and GPU. To execute the regular version, run it as usual:

```
$ ./example_c 512 256 256
compute time = 1.848575
maxval = 1.570796, minval = 1.570796
```

In order to run GPU-accelerated version, simply set kernelgen_runmode environment variable to 1:

```
$ kernelgen_runmode=1 ./example_c 512 256 256
compute time = 0.293359
maxval = 1.570796, minval = 1.570796
```



Current limitations of OpenACC compilers

OpenACC currently focuses on immediate acceleration benefits in small and average codes, and could hardly be shifted to broader scope without addressing the following limitations:

- External calls support of external calls in accelerated loops is a must for big projects, where functionality is distributed between multiple code units, for instance, Fortran modules.
- Pointers analysis in many circumstances compiler cannot reliably determine the relationship between pointers and memory access ranges, requiring user to provide additional information with directives.
- ⇒ Should one sacrifice code design and integrity for the benefit of acceleration?

OpenACC: no external calls

OpenACC compilers do not allow calls from different compilation units:

sincos.f90

```
!$acc parallel
do k = 1, nz
    do j = 1, ny
    do i = 1, nx
        xy(i, j, k) = sincos_ijk(x(i, j, k), y(i, j, k))
    enddo
enddo
enddo
!$acc end parallel
```

function.f90

```
function sincos_ijk(x, y)
implicit none
  real, intent(in) :: x, y
  real :: sincos_ijk
  sincos_ijk = sin(x) + cos(y)
end function sincos_ijk
```

```
pgfortran -fast -Mnomain -Minfo=accel -ta=nvidia,time -Mcuda=keepgpu,keepbin,keepptx,←
    ptxinfo -c ../sincos.f90 -o sincos.o

PGF90-W-0155-Accelerator region ignored; see -Minfo messages (../sincos.f90: 33)

sincos:
    33, Accelerator region ignored
    36, Accelerator restriction: function/procedure calls are not supported
    37, Accelerator restriction: unsupported call to sincos_ijk
```

KernelGen: can handle external calls

Dependency resolution during linking Kernels generation in runtime

⇒ Support for external calls defined in other objects or static libraries

sincos.f90

function.f90

```
function sincos_ijk(x, y)
implicit none
  real, intent(in) :: x, y
  real :: sincos_ijk
  sincos_ijk = sin(x) + cos(y)
end function sincos_ijk
```

```
Launching kernel __kernelgen_sincos__loop_3
blockDim = { 32, 4, 4 }
gridDim = { 16, 128, 16 }
Finishing kernel __kernelgen_sincos__loop_3
_kernelgen_sincos__loop_3 time = 4.986428e-03 sec
```

KernelGen: and external static libraries

Thanks to cutomized LTO wrapper, KernelGen can extract kernels dependencies from static libraries:

```
kernelgen-gcc -std=c99 -c ../main.c -o main.o
kernelgen-gfortran -c ../sincos.f90 -o sincos.o
kernelgen-gfortran -c ../function.f90 -o function.o
ar rcs libfunction.a function.o
kernelgen-gfortran main.o sincos.o -o function -L. -lfunction
```

```
$ kernelgen_runmode=1 ./function 512 512 64
   __kernelgen_sincos__loop_3: regcount = 22, size = 512
Loaded '__kernelgen_sincos__loop_3' at: 0xc178f0
Launching kernel __kernelgen_sincos__loop_3
   blockDim = { 32, 4, 4 }
   gridDim = { 16, 128, 16 }
Finishing kernel __kernelgen_sincos__loop_3
   __kernelgen_sincos__loop_3 time = 4.974710e-03 sec
```

OpenACC: no pointers tracking

Compiler cannot determine relationships between pointers and data ranges:

sincos.c

```
pgcc -fast -Minfo=accel -ta=nvidia,time -Mcuda=keepgpu,keepbin,keepptx,ptxinfo -c ../sincos.c -o sincos.o
PGC-W-0155-Compiler failed to translate accelerator region (see -Minfo messages): Could not find allocated-variable index ←→
for symbol (../sincos.c: 27)
sincos:

27, Accelerator kernel generated
28, Complex loop carried dependence of *(y) prevents parallelization
Complex loop carried dependence of *(x) prevents parallelization
Complex loop carried dependence of *(xy) prevents parallelization
...
30, Accelerator restriction: size of the GPU copy of xy is unknown
```

Pointer alias analysis is performed in runtime, assisted with addresses substitution:

```
for (c2=0;c2<=63;c2++) {
  for (c4=0;c4<=511;c4++) {
   for (c6=0;c6<=511;c6++) {
      Stmt__5_cloned_(c2,c4,c6);
    }
  }
}</pre>
```

Pointer alias analysis is performed in runtime, assisted with addresses substitution:

```
for (c2=0;c2<=63;c2++) {
  for (c4=0;c4<=511;c4++) {
   for (c6=0;c6<=511;c6++) {
      Stmt__5_cloned_(c2,c4,c6);
    }
  }
}</pre>
```

Static Control Part (SCoP) representation of the loop kernel

```
Statements {
    Stmt__5_cloned_
    Domain := { Stmt__5_cloned_[i0, i1, i2] : i0 >= 0 and i0 <= 63 and i1 >= 0 and i1 <= 511 and i2 >= 0 and ← i2 <= 511 };
    Scattering := { Stmt__5_cloned_[i0, i1, i2] -> scattering[0, i0, 0, i1, 0, i2, 0] };
    ReadAccess := { Stmt__5_cloned_[i0, i1, i2] -> NULL[o0] : o0 >= 47246749696 + 1048576i0 + 2048i1 + 4i2 and o0← ← 47246749699 + 1048576i0 + 2048i1 + 4i2 };
    ReadAccess := { Stmt__5_cloned_[i0, i1, i2] -> NULL[o0] : o0 >= 47313862656 + 1048576i0 + 2048i1 + 4i2 and o0← ← 47313862659 + 1048576i0 + 2048i1 + 4i2 };
    WriteAccess := { Stmt__5_cloned_[i0, i1, i2] -> NULL[o0] : o0 >= 47380975616 + 1048576i0 + 2048i1 + 4i2 and o0← ← 47380975619 + 1048576i0 + 2048i1 + 4i2 };
}
```

Pointer alias analysis is performed in runtime, assisted with addresses substitution:

```
for (c2=0;c2<=63;c2++) {
  for (c4=0;c4<=511;c4++) {
    for (c6=0;c6<=511;c6++) {
        Stmt__5_cloned_(c2,c4,c6);
     }
  }
}</pre>
```

Static Control Part (SCoP) representation of the loop kernel

```
Statements {
    Stmt__5_cloned_
    Domain := { Stmt__5_cloned_[i0, i1, i2] : i0 >= 0 and i0 <= 63 and i1 >= 0 and i1 <= 511 and i2 >= 0 and ← i2 <= 511 };
    Scattering := { Stmt__5_cloned_[i0, i1, i2] -> scattering[0, i0, 0, i1, 0, i2, 0] };
    ReadAccess := { Stmt__5_cloned_[i0, i1, i2] -> NULL[o0] : o0 >= 47246749696 + 1048576i0 + 2048i1 + 4i2 and o0← <= 47246749699 + 1048576i0 + 2048i1 + 4i2 };
    ReadAccess := { Stmt__5_cloned_[i0, i1, i2] -> NULL[o0] : o0 >= 47313862656 + 1048576i0 + 2048i1 + 4i2 and o0← <= 47313862659 + 1048576i0 + 2048i1 + 4i2 };
    WriteAccess := { Stmt__5_cloned_[i0, i1, i2] -> NULL[o0] : o0 >= 47380975616 + 1048576i0 + 2048i1 + 4i2 and o0← <= 47380975619 + 1048576i0 + 2048i1 + 4i2 };
}

Dotal read/write access analysis after
```

substituting pointers and constants

Pointer alias analysis is performed in runtime, assisted with addresses substitution:

sincos.c

result

```
Launching kernel __kernelgen_sincos_loop_10
blockDim = { 32, 4, 4 }
gridDim = { 16, 128, 16 }
Finishing kernel __kernelgen_sincos_loop_10
__kernelgen_sincos_loop_10 time = 2.300006e-02 sec
```



Comfortable acceleration framework should be designed, taking in account properties of the supported languages and common habits of developers, for instance:

- Handle different forms of loops, not only arithmetic for/do
- Parallelize implicit loops (Fortran array-wise statements, elemental functions, etc.)
- Pointer arithmetics (C/C++)
- ...

Parallelizing while-loops

Thanks to the nature of LLVM and Polly, KernelGen can parallelize while-loops *semantically equivalent* to for-loops (OpenACC can't):

```
Launching kernel __kernelgen_matmul__loop_9

blockDim = { 32, 32, 1 }

gridDim = { 2, 16, 1 }

Finishing kernel __kernelgen_matmul__loop_9

__kernelgen_matmul__loop_9 time = 0.00953514 sec
```

Parallelizing Fortran array-wise code

Fortran array-wise statements are expanded into plain loops inside compiler frontend. For this reason, KernelGen is able to parallelize them into GPU kernels, for instance:

```
program demo
    implicit none
    integer :: n
    complex*16, allocatable, dimension(:) :: c1, c2, ←
    character(len=128) :: arg
    integer :: i
   real*8 :: v1. v2
9
   real :: start. finish
    call get command argument(1, arg)
    read(arg. '(I64)') n
    ! Allocate data arrays.
    allocate(c1(n), c2(n), z(n))
    ! Initialize arrays.
    do i = 1. n
      call random number(v1)
      call random number(v2)
```

```
c1(i) = cmplx(v1, v2)
  call random_number(v1)
  call random number(v2)
 c2(i) = cmplx(v1, v2)
enddo
! Implicit computational loop
call cpu time(start)
z = coniq(c1) * c2
call cpu time(finish)
write(*.*) 'compute time = '. finish - start
print *. 'z min = ('. minval(realpart(z)), &
   '. '. minval(imagpart(z)), '), max = (', &
 maxval(realpart(z)), ', ', minval(imagpart(z)), ')'
! Deallocate arrays.
deallocate(c1, c2, z)
end program demo
```

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Parallelizing Fortran array-wise code

Compile the Fortran example as usual, just use kernelgen-gfortran instead of gfortran:

```
$ kernelgen-gfortran -03 -std=c99 conjg.f90 -o conjg
```

```
$ ./conjg $((256*256*256)) compute time = 0.10800600 z min = ( 7.18319034686704879E-006 , -0.99788337878880551 ), max = ( \leftrightarrow 1.9723582564715194 , -0.99788337878880551 )
```

```
$ kernelgen_runmode=1 ./conjg $((256*256*256))
compute time = 2.80020237E-02
z min = ( 7.18319034686704879E-006 , -0.99788337878880551 ), max = ( ←
1.9723582564715194 , -0.99788337878880551 )
```

OpenACC: no pointer arithmetics

Compiler cannot parallelize loops containing pointer arithmetics:

sincos.c

```
$ make
pgc -fast -Minfo=accel -ta=nvidia,time -Mcuda=keepgpu,keepbin,keepptx,ptxinfo -c ../sincos.c -o sincos.o
PGC-W-0155-Pointer assignments are not supported in accelerator regions: xyp (../sincos.c: 34)
PGC-W-0155-Accelerator region ignored (../sincos.c: 29)
PGC/x86-64 Linux 13.2-0: compilation completed with warnings
```

KernelGen: pointer arithmetics support

In LLVM/Polly used by KernelGen all arrays accesses are lowered to pointers, thus there is no difference between indexed arrays and pointer arithmetics, both are supported:

sincos.c

```
Launching kernel __kernelgen_sincos_loop_10

blockDim = { 32, 4, 4 }

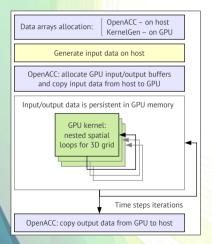
gridDim = { 16, 128, 16 }

Finishing kernel __kernelgen_sincos_loop_10

__kernelgen_sincos_loop_10 time = 2.298868e-02 sec
```



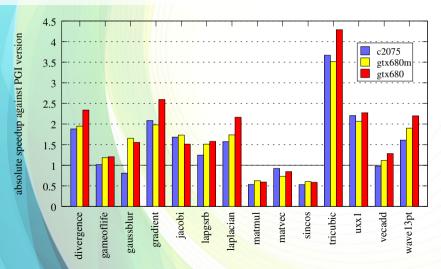
Performance test suite



The test suite is composed out of similarly organized small applications, simulating typical numerical model behavior:

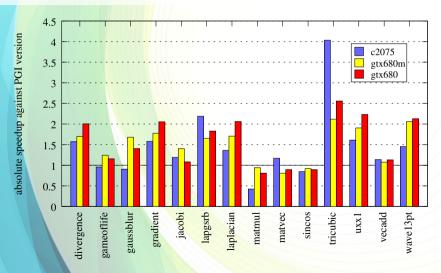
- Outer time iterations loop (sequential)
- Inner 2D or 3D spatial loops on regular grid (parallel)
- Input/output data is persistent in GPU memory during time iterations
- Results correctness in checked by computing means/norms of output data

Performance: KernelGen vs PGI OpenACC



- Tests precision mode: single
- Software: KernelGen r1740, PGI OpenACC 13.2
- Hardware: NVIDIA Tesla C2075 (GF110, sm_20), NVIDIA GTX 680M (GK104, sm_30), NVIDIA GTX 680 (GK104, sm_30)
- Values above 1 KernelGen kernel is faster than PGI, values below 1 – PGI kernel is faster than KernelGen (on the same GPU)
- Measurements are averaged from 10 invocations of all tests and 10 iterations inside every test

Performance: KernelGen vs PGI OpenACC



- Tests precision mode: double
- Software: KernelGen r1740, PGI OpenACC 13.2
- Hardware: NVIDIA Tesla C2075 (GF110, sm_20), NVIDIA GTX 680M (GK104, sm_30), NVIDIA GTX 680 (GK104, sm_30)
- Values above 1 KernelGen kernel is faster than PGI, values below 1 – PGI kernel is faster than KernelGen (on the same GPU)
- Measurements are averaged from 10 invocations of all tests and 10 iterations inside every test

Performance factors: cache config

Cache config Since current kernels generator does not utilize shared memory, in KernelGen cache mode is configured to larger L1 cache, giving some additional speedup

```
// Since KernelGen does not utilize shared memory at the moment,
// use larger L1 cache by default.
CU_SAFE_CALL(cuCtxSetCacheConfig(CU_FUNC_CACHE_PREFER_L1));
```

Performance factors: compute grid

KernelGen uses {128, 1, 1} blocks and 3D grid, while PGI uses {128, 1} blocks and 2D grid. Previously we used {32, 4, 4}, which was slower.

PGI and KernelGen profilers reports for divergence test, single precision, $512 \times 256 \times 256$ problem:

```
Accelerator Kernel Timing data
/home/marcusmae/forge/kernelgen/tests/perf/divergence/pgi/../divergence.c
divergence NVIDIA devicenum=0
time(us): 154,660
62: kernel launched 10 times
grid: [4x254] block: [128]
device time(us): total=154,660 max=15,560 min=15,373 avg=15,466
elapsed time(us): total=154,742 max=15,570 min=15,381 avg=15,474
```

```
Kernel function call __kernelgen_divergence_loop_10
__kernelgen_divergence_loop_10 @ 0xeb32b61a9530d97f53f77c5abbd67132
Launching kernel __kernelgen_divergence_loop_10
blockDim = { 128, 1, 1 }
gridDim = { 4, 254, 254 }
Finishing kernel __kernelgen_divergence_loop_10
__kernelgen_divergence_loop_10 time = 7.912811e-03 sec
```

Performance factors: code optimization

S KernelGen under-optimizes GPU math (sincos) and stores in reduction (matmul, matvec):

```
CUDA.LoopHeader.x.preheader:
                                                : preds = %"Loop Function Root"
 %p_newGEPInst.cloned = getelementptr float* inttoptr (i64 47380979712 to float*)
 store float 0.000000e+00, float * %p newGEPInst.cloned
 %p .moved.to.4.cloned = shl nsw i64 %3, 9
 br label %polly.loop body
CUDA Afterloop x:
                                                 : preds = %polly.loop body, %"Loop Function Root"
 ret void
polly.loop body:
                                                  : preds = %polly.loop body. %CUDA.LoopHeader.x.preheader
 % p scalar = phi float [ 0.000000e+00, %CUDA,LoopHeader,x,preheader ], [ %p 8, %polly,loop body ]
 %polly.loopiv10 = phi i64 [ 0, %CUDA.LoopHeader.x.preheader ], [ %polly.next loopiv, %polly.loop body ]
 %pollv.next loopiv = add i64 %pollv.loopiv10. 1
 %p_ = add i64 %polly.loopiv10, %p_.moved.to.4.cloned
 %p newGEPInst9.cloned = getelementptr float* inttoptr (i64 47246749696 to float*), i64 %p
 %p newGEPInst12.cloned = getelementptr float* inttoptr (i64 47380971520 to float*), i64 %polly.loopiy10
 % p scalar 5 = load float* %p newGEPInst9.cloned
 % p scalar 6 = load float* %p newGEPInst12.cloned
 %p 7 = fmul float % p scalar 5, % p scalar 6
 %p 8 = fadd float % p scalar , %p 7
 store float %p 8, float* %p newGEPInst.cloned
 %exitcond = icmp eq i64 %pollv.next loopiv. 512
 br i1 %exitcond, label %CUDA.AfterLoop.x. label %polly.loop body
```

Performance factors: code optimization

S KernelGen under-optimizes GPU math (sincos) and stores in reduction (matmul, matvec):

```
CUDA. LoopHeader.x.preheader:
                                                : preds = %"Loop Function Root"
 %p newGEPInst.cloned = getelementptr float* inttoptr (i64 47380979712 to float*)
 store float 0.000000e+00, float * %p newGEPInst.cloned
 %p .moved.to.4.cloned = shl nsw i64 %3. 9
 br label %polly.loop body
CUDA. AfterLoop.x:
                                                 ; preds = %polly.loop body, %"Loop Function Root"
 ret void
polly.loop body:
                                                 : preds = %polly.loop body. %CUDA.LoopHeader.x.preheader
 % p scalar = phi float Γ 0.000000e+00, %CUDA.LoopHeader.x.preheader ], Γ %p 8, %polly.loop body ]
 %polly.loopiv10 = phi i64 [ 0, %CUDA.LoopHeader.x.preheader 1. [ %polly.next loopiy. %polly.loop.body 1
 %pollv.next loopiv = add i64 %pollv.loopiv10. 1
                                                               Marked out lines are header, tail and
 %p = add i64 %polly.loopiv10, %p .moved.to.4.cloned
 %p newGEPInst9.cloned = getelementptr float* inttoptr (i
                                                              body of loop, as it looks like in LLVM IR
 %p newGEPInst12.cloned = getelementptr float* inttoptr
 % p_scalar_5 = load float* %p_newGEPInst9.cloned
 % p scalar 6 = load float* %p newGEPInst12.cloned
 %p 7 = fmul float % p scalar 5. % p scalar 6
 %p 8 = fadd float % p scalar , %p 7
 store float %p 8, float* %p newGEPInst.cloned
 %exitcond = icmp eq i64 %polly.next loopiy, 512
 br i1 %exitcond, label %CUDA.AfterLoop.x, label %polly.loop body
```

Performance factors: code optimization

S KernelGen under-optimizes GPU math (sincos) and stores in reduction (matmul, matvec):

```
CUDA.LoopHeader.x.preheader:
                                                                                                                           : preds = %"Loop Function Root"
    %p newGEPInst.cloned = getelementptr float* inttoptr (i64 47380979712 to float*)
    store float 0.000000e+00, float * %p newGEPInst.cloned
    %p .moved.to.4.cloned = shl nsw i64 %3. 9
    br label %polly.loop body
CUDA.AfterLoop.x:
                                                                                                                             ; preds = %polly.loop body, %"Loop Function Root"
    ret void
                                                                                                                              : preds = %polly.loop body. %CUDA.LoopHeader.x.preheader
polly.loop body:
    % p scalar = phi float Γ 0.000000e+00, %CUDA.LoopHeader
                                                                                                                                                              Properly optimized reduction should ac-
    %polly.loopiv10 = phi i64 [ 0, %CUDA.LoopHeader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preheader.x.preh
    %pollv.next loopiv = add i64 %pollv.loopiv10. 1
                                                                                                                                                                 cumulate sum on register and store it
    %p = add i64 %polly.loopiv10, %p .moved.to.4.cloned
    %p newGEPInst9.cloned = getelementptr float* inttoptr (:
                                                                                                                                                           (memory operation) at the end only once.
    %p newGEPInst12.cloned = getelementptr float* inttoptr
                                                                                                                                                         Here store is performed on every iteration!
    % p_scalar_5 = load float* %p_newGEPInst9.cloned
    % p scalar 6 = load float* %p newGEPInst12.cloned
    %p 7 = fmul float % p scalar 5. % p scalar 6
    %p 8 = fadd float % p scalar , %p 7
    store float %p 8, float* %p newGEPInst.cloned
    %exitcond = icmp eq i64 %polly.next loopiy, 512
    br i1 %exitcond, label %CUDA.AfterLoop.x. label %polly.loop body
```

Performance factors: code generation

4 PGI is a source-to-source compiler, while KernelGen is a full compiler, thanks to LLVM NVPTX backend

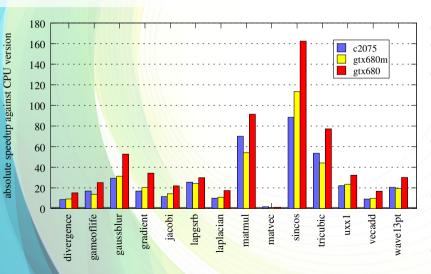
PGI:



KernelGen:

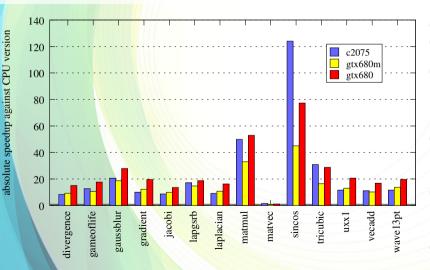


Performance: KernelGen vs CPU



- Tests precision mode: single
- Software: KernelGen r1740, GCC 4.6.4
- Hardware: NVIDIA Tesla C2075 (GF110, sm_20), NVIDIA GTX 680M (GK104, sm_30), NVIDIA GTX 680 (GK104, sm_30), Intel Core i7-3610QM CPU 2.30GHz
- Measurements are averaged from 10 invocations of all tests and 10 iterations inside every test
- Values above 1 KernelGen GPU kernel is faster than GCC CPU kernel, values below 1 – GCC is faster than KernelGen
- CPU version is single-core

Performance: KernelGen vs CPU



- Tests precision mode: double
- Software: KernelGen r1740, GCC 4.6.4
- Hardware: NVIDIA Tesla C2075 (GF110, sm_20), NVIDIA GTX 680M (GK104, sm_30), NVIDIA GTX 680 (GK104, sm_30), Intel Core i7-3610QM CPU 2.30GHz
- Measurements are averaged from 10 invocations of all tests and 10 iterations inside every test
- Values above 1 KernelGen GPU kernel is faster than GCC CPU kernel, values below 1 – GCC is faster than KernelGen
- CPU version is single-core



Parallelism detection

KernelGen analyses loops dependencies and maps parallel loops on GPU compute grid. Sequential loops are kept unchanged, either inner or outer.

```
subroutine match filter(HH, szhh, XX, szxx, YY, szvy)
 implicit none
 integer(kind=IKIND), intent(in) :: szhh, szxx, szvv
 real(kind=RKIND), intent(in) :: HH(szhh), XX(szxx)
 real(kind=RKIND), intent(out) :: YY(szyy)
 integer(kind=IKIND) :: i. i
 integer, parameter :: rkind = RKIND
  ! This loop will be parallelized
 do i = 1. szvv
  YY(i) = 0.0 \text{ rkind}
   ! This loop will not be parallelized
   do i = 1, szhh
     YY(i) = YY(i) + XX(i + i - 1) * HH(i)
    enddo
  enddo
end subroutine match filter
```

Parallelism detection

KernelGen analyses loops dependencies and maps parallel loops on GPU compute grid. Sequential loops are kept unchanged, either inner or outer.

```
subroutine match filter(HH, szhh, XX, szxx, YY, szvv)
 implicit none
 integer(kind=IKIND), intent(in) :: szhh, szxx, szvv
 real(kind=RKIND). intent(in) :: HH(szhh). XX(szxx)
 real(kind=RKIND), intent(out) :: YY(szyy)
 integer(kind=IKIND) :: i, j
 integer, parameter :: rkind = RKIND
  ! This loop will be parallelized
 do i = 1. szvv
   YY(i) = 0.0 \text{ rkind}
    ! This loop will not be parallelized
   do i = 1, szhh
     YY(i) = YY(i) + XX(i + i - 1) * HH(i)
    enddo
  enddo
end subroutine match filter
```

Parallelization of reduction loops not yet supported, this loop will be serial

Parallelism detection

KernelGen analyses loops dependencies and maps parallel loops on GPU compute grid. Sequential loops are kept unchanged, either inner or outer.

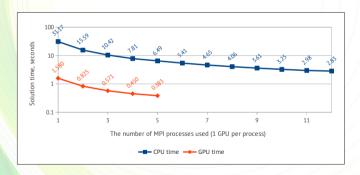
```
subroutine match filter(HH, szhh, XX, szxx, YY, szvy)
 implicit none
 integer(kind=IKIND). intent(in) :: szhh. szxx. szvv
 real(kind=RKIND). intent(in) :: HH(szhh). XX(szxx)
 real(kind=RKIND), intent(out) :: YY(szyy)
 integer(kind=IKIND) :: i, j
 integer, parameter :: rkind = RKIND
  ! This loop will be parallelized
 do i = 1, szvv
   YY(i) = 0.0 \text{ rkind}
   ! This loop will not be parallelized
   do i = 1, szhh
     YY(i) = YY(i) + XX(i + i - 1) * HH(i)
    enddo
  enddo
end subroutine match filter
```

However, the outer loop will be detected parallel and taken on GPU, with inner serial loop processed by each thread



Cooperation with MPI

KernelGen naturally co-exists with MPI parallelism, assigning each MPI process a single GPU:



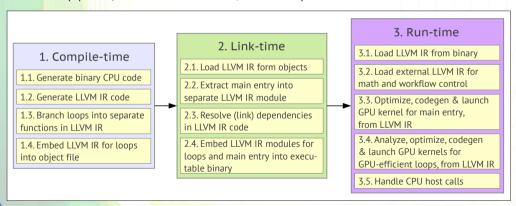
Comparing performance of time domain matched filter application, compiled with KernelGen r1740 for 1-12 cores of Intel Xeon X5670 CPUs and 1-5 NVIDIA Tesla C2070 GPUs (Fermi sm_20)

KernelGen dependencies

- GCC for frontends and regular compiling pipeline (GPL)
- DragonEgg GCC plugin for converting GCC's IR (gimple) into LLVM IR (GPL)
- <u>LLVM</u> for internal compiler infrastructure (BSD)
- Polly for loops parallelism analysis (BSD+GPL)
- NVPTX backend for emitting LLVM IR into PTX/GPU intermediate assembly (BSD)
- PTXAS for emitting PTX/GPU into target GPU ISA (proprietary, no source code)
- AsFermi for necessary CUBIN-level tricks in Fermi GPU ISA (MIT/BSD)
- NVIDIA GPU driver for deploying the resulting code on GPUs (proprietary, no source code)

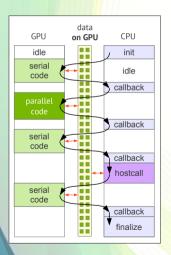
KernelGen compiler pipeline

KernelGen conserves original host compiler pipeline (based on GCC), extending it with parallel LLVM-based pipeline, which is activated and/or used if specific environment variables are set.





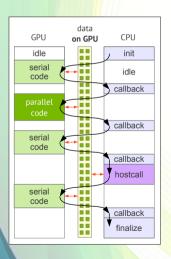
GPU-directed execution



KernelGen uses GPU-directed execution model:

- All activities are initiated by GPU (CPU is "passive")
- All data (global, dynamic, immediate) resides GPU memory
- GPU data and control flow are managed by main kernel, which is persistent on GPU during whole application lifetime

GPU-directed execution

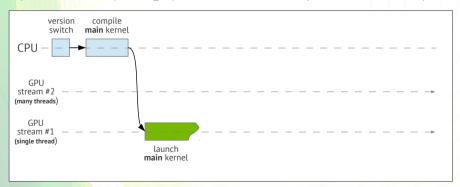


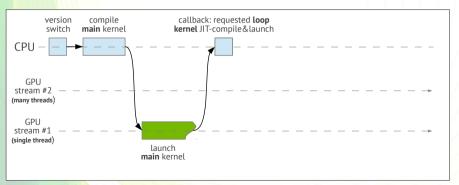
GPU-directed execution model benefits:

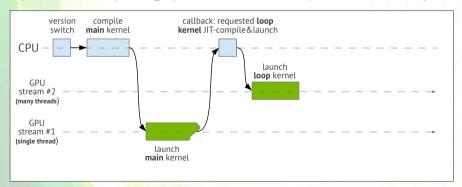
- No need to manage host
 ⇔device memory transfers explicitly and track hidden data dependencies (side-effects)
- Possibility to utilize long uninterrupted kernels with dynamic parallelism, where available
- Transparent transition of CPU MPI nodes into GPU MPI nodes, with CUDA-aware MPI
- GPU device functions initially loaded with main kernel are shared with all other dynamically loaded kernels, minimizing compilation time and code size (in contrast, OpenACC and CUDA kernels must be self-containing)

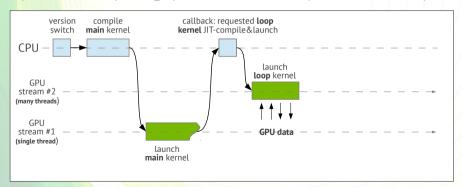
version switch	
GPU	
GFU GFU (many threads)	
GPU stream #1	

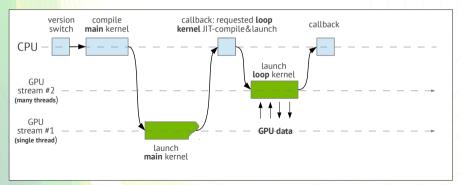
version compile switch main kernel
GPU stream #2 — — — — — — — — → nany threads)
GPU tream #1 — — — — — — — — — — — — — — — — — —

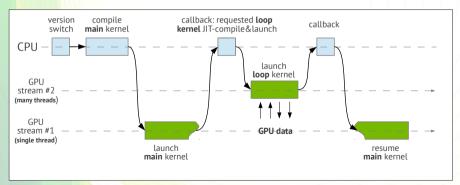


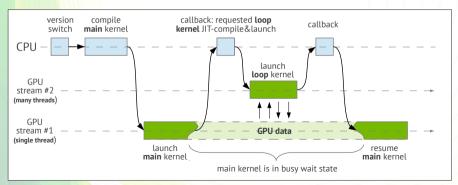


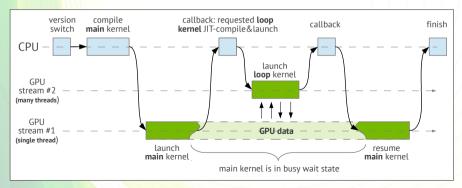






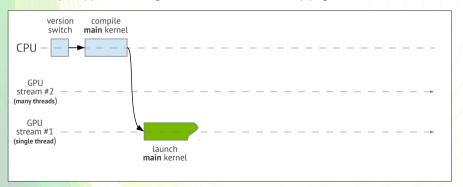


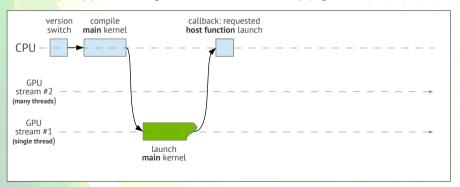


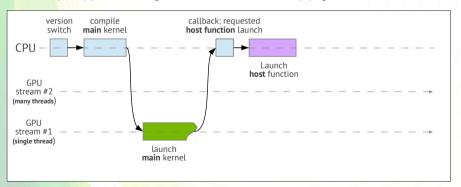


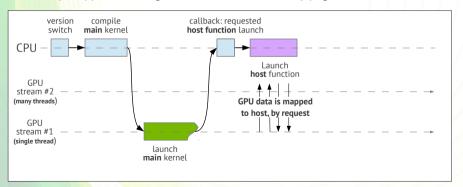
version switch	
CPU	
GPU stream #2 — — — — — — — — — — — — — — — — — —	
GPU stream #1 — — — — — — — — — — — — — — — — — (single thread)	-

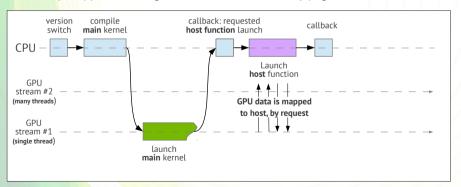


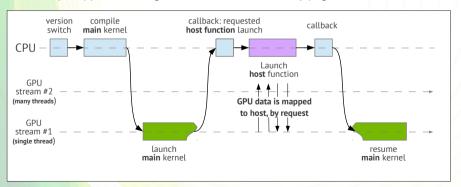


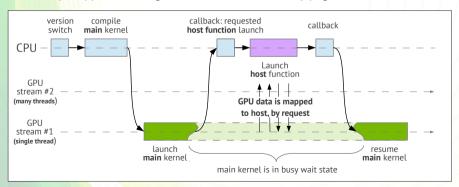


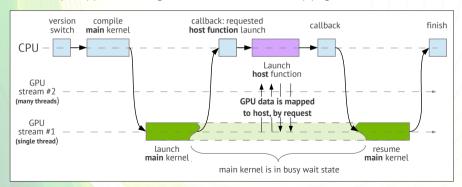






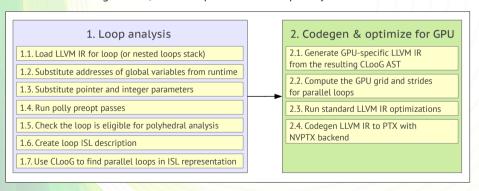






KernelGen loops analysis pipeline

KerenlGen takes part of loop analysis into runtime, in order to process only really used loops, and do it better with help of additional information available from the execution context. Introduced runtime overhead is neglectible, if the loop is invoked frequently.





Let's briefly walk through KernelGen code generation steps for the following function:

sincos.c

First, GCC frontend produces GIMPLE IR from any high-level language:

```
sincos (integer(kind=4) & restrict nx. integer(kind=4) & restrict nv. integer(kind=4) & restrict nz. real(kind=4) Γ0:D←
      .1629] * restrict x, real(kind=4)[0:D.1626] * restrict y, real(kind=4)[0:D.1632] * restrict xy)
 D.1646 = ~stride.16:
 offset.19 = D.1646 - stride.18:
       if (i <= D.1568) goto <D.1650>; else goto <D.1651>;
       <D.1650>:
        <D.1652>:
          logical(kind=4) D.1576:
              logical(kind=4) D.1575:
              D.1676 = sincos iik (D.1675, D.1669):
              *xvΓD.16637 = D.1676;
```

3/75

Next, DragonEgg converts GIMPLE IR to LLVM IR:

```
: ModuleID = '../sincos.f90'
target datalayout = "e-p:64:64:64-5128-i1:8:8-i8:8:8-i16:16:16-i32:32:32-i64:64:64-f16:16:16-f32:32:32-f64:64:64-f128↔
      :128:128-v64:64:64-v128:128:128-a0:0:64-s0:64:64-f80:128:128-n8:16:32:64"
target triple = "x86 64-unknown-linux-gnu"
declare float asincos ijk (...)
define void asincos (i32* noalias %nx. i32* noalias %ny. i32* noalias %nz. [0 x float]* noalias %x. [0 x float]* noalias ↔
      %v, [0 x float]* noalias %xv) nounwind uwtable {
 \%92 = add i64 \%89. \%91
 %93 = add i64 %87, %92
 \%94 = add i64 \%93. \%41
 %95 = bitcast Γ0 x float]* %4 to float*
 %96 = getelementptr float* %95, i64 %94
 %97 = call float bitcast (float (...)* @sincos iik to float (float*, float*)*)(float* %96, float* %86) nounwind
 %98 = bitcast [0 x float]* %5 to float*
 %99 = getelementptr float* %98, i64 %76
 store float %97, float* %99, align 4
 %100 = icmp eq i32 %68. %66
 %101 = add i32 %68. 1
 %102 = icmp ne i1 %100. false
 br i1 %102. label %"7". label %"6"
```

KernelGen compile-time extracts loops potentially suitable for GPU kernels into new functions. Groups of multiple loops are extracted recursively, in case only subset of them is parallel. KernelGen runtime substitutes constants and pointers from runtime context for easier analysis:

```
; ModuleID = '__kernelgen_sincos__loop_3_module'
target datalayout = "e-p:64:64:64-i1:8:8-i8:8:8-i16:16:16:16-i32:32:32-i64:64:64-f32:32:32-f64:64:64-v16:16:16-v32:32:32-v64↔
       :64:64-v128:128:128-n16:32:64"
target triple = "nyptx64-unknown-unknown"
define void a kernelgen sincos loop 3(i32*) nounwind {
"Loop Function Root":
  br label %"4.preheader.cloned"
  *8 = getelementptr Γ0 x float]* inttoptr (i64 47313862656 to Γ0 x float]*). i64 0. i64 %7
  \%9 = \text{getelementptr } [0 \times \text{float}]^* \text{ inttoptr } (\text{i64} \frac{47246749696}{47246749696} \text{ to } [0 \times \text{float}]^*), \text{ i64 } [0, \text{i64} \%]
  %10 = load float* %9, align 4
  %11 = call float @sinf(float %10) nounwind readnone alignstack(1)
  %12 = load float* %8, align 4
  %13 = call float acosf(float %12) nounwind readnone alignstack(1)
  %14 = fadd float %11, %13
  %15 = getelementptr [0 x float]* inttoptr (i64 47380975616 to [0 x float]*), i64 0, i64 %7
  store float %14, float* %15, align 4
declare float asinf(float) nounwind readnone alignstack(1)
declare float acosf(float) nounwind readnone alignstack(1)
```

KernelGen runtime analyses kernel loop for parallelism. In case it is parallel, LLVM IR is specialized for NVPTX (note @llvm.nvvm.* intrinsics, ptx_kernel and ptx_device):

```
: ModuleID = ' kernelgen sincos loop 3 module'
target datalayout = "e-p:64:64:64-i1:8:8-i8:8:8-i16:16:16-i32:32:32-i64:64:64-f32:32:32-f64:64:64-v16:16:16-v32:32:32-v64↔
      .64.64-v128.128.128-n16.32.64"
target triple = "nyptx64-unknown-unknown"
a kernelgen version = constant Γ15 x i81 c"0.2/1654:1675M\00"
define ptx kernel void a kernelgen sincos loop 3(i32* nocapture) nounwind alwaysinline {
"Loop Function Root":
 %tid.z = tail call ptx device i32 allvm.nvvm.read.ptx.sreq.tid.z()
 %ctaid.z = tail call ptx device i32 @llvm.nvvm.read.ptx.sreq.ctaid.z()
 %PositionOfBlockInGrid.z = shl i32 %ctaid.z. 2
 %BlockLB.Add.ThreadPosInBlock.z = add i32 %PositionOfBlockInGrid.z. %tid.z
 %p_28 = tail call ptx_device float @sinf(float %_p_scalar_) nounwind readnone alignstack(1)
 % p scalar 29 = load float* %p scevgep6
 %p 30 = tail call ptx device float acosf(float % p scalar 29) nounwind readnone alignstack(1)
 %p 31 = fadd float %p 28, %p 30
 store float %p 31, float* %p scevgep
 br label %CUDA.AfterLoop.z
```

PTX assembler is generated from LLVM IR, using LLVM NVPTX backend:

```
.visible .entry _kernelgen_sincos_loop_3(.param .u64 _kernelgen_sincos_loop_3_param_0)
// RR#0 ·
                                       // %Loop Function Root
   mov.u32 %r0. %tid.z:
  mov.u32 %r1, %ctaid.z:
   shl.b32 %r1. %r1. 2:
   add.s32 %r2. %r1. %r0:
   a%p0 bra BB0 4;
   // Callseg Start 42
    .reg .b32 temp param reg:
   // <end>}
    .param .b32 param0:
   st.param.f32 [param0+0]. %f0:
    .param .b32 retval0:
   call.uni (retval0).
    sinf.
    param0
```

Finally, a Fermi ISA is generated for function, in no-cloning mode. Unresolved function calls (*JCAL 0x0*) are replaced with actual addresses of functions already loaded by main kernel.

```
Function: kernelgen sincos loop 3
/*0008*/
             /*0×10005de428004001*/
                                     MOV R1, c [0x0] [0x44];
/*0010*/
            /*0×9c00dc042c000000*/
                                     S2R R3. SR CTAid Z:
/*0018*/
             /*0x8c001c042c000000*/
                                     S2R RØ. SR Tid Z:
/*0120*/
             /*0x08451c036000c000*/
                                    SHL R20. R4. 0x2:
/*0128*/
             /*0×14055c4340000000*/
                                    ISCADD R21, R0, R5, 0x2;
/*0130*/
             /*0×01411c020c0080c0*/
                                    TADD32T R4.CC. R20. 0x203000:
/*0138*/
                                    IADD.X R5. R21. 0xb:
             /*0x2d515c434800c000*/
/*0148*/
             /*0×00411c8584000000*/
                                     LD.E R4, [R4]:
/*0150*/
             /*0x00010007100017b2*/ JCAL 0x5ec80:
/*0158*/
             /*0x01419c020c108100*/
                                     IADD32I R6.CC, R20, 0x4204000:
/*0160*/
             /*0x10009de428000000*/
                                     MOV R2. R4:
/*0168*/
             /*0x2d51dc434800c000*/
                                     IADD.X R7, R21, 0xb:
/*0170*/
             /*0×00611c8584000000*/
                                     LD.E R4. [R6]:
/*0178*/
             /*0x00010007100018eb*/ JCAL 0x63ac0:
/*0188*/
             /*0x01419c020c208140*/
                                     IADD32I R6.CC. R20. 0x8205000:
/*0190*/
             /*0×10201c0050000000*/
                                     FADD RØ, R2, R4:
/*0198*/
             /*0x2d51dc434800c000*/
                                     IADD.X R7. R21. 0xb:
/*01a0*/
             /*0x00601c8594000000*/
                                     ST. F [R6]. R0:
/*01a8*/
             /*0x00001de780000000*/
                                     FXTT:
```

KernelGen current limitations

KernelGen still has several important features not covered:

- Loop index must be incremented with positive unit value
- No support for arbitrary indirect indexing, e.g. a(b(i)) (same issue in OpenACC)
- No support for reduction idiom (supported by OpenACC)
- Polly may face insufficient code optimization for proper parallelizing some specific test cases

Conclusions

- KernelGen project implemented a full compiler prototype to produce parallel GPU kernels from unmodified CPU source code
- 2 C and Fortran languages support is widely tested, focusing mostly on Fortran
- Performance of GPU kernels generated by KernelGen is 0.5x-4x in comparison to newest commercial PGI OpenACC compiler
- KernelGen eases porting of applications on GPU by means of supporting many features missing in OpenACC
- GPU-directed execution model allows seamless transition between CPU-MPI and GPU-MPI versions of application
- 6 KernelGen is based on freeware and mostly open-source technologies

Now to test?

- Note you will need SM_20 or newer NVIDIA GPU and CUDA 5.0 driver installed
- Compile KernelGen for your target system, as described in guide
- Use KernelGen to compile a program with computational loops:

```
$ source ~/rpmbuild/CHROOT/opt/kernelgen/usr/bin/kernelgen-vars.sh
$ kernelgen-gfortran test.f90 -o test
```

- Deploy the code on GPU and check out the verbose reports about launched GPU kernels:
 - \$ kernelgen runmode=1 ./test <args>
- Compare performance and result to the original CPU version:
 - \$./test <args>
- Encountered an issue? Please file it into our public bug tracker

Testing COSMO and WRF

KernelGen is able to compile original source code for COSMO and WRF into valid executables. Both models are now being actively tested.

WRF:

```
$ NETCDF=/opt/kernelgen ./configure
Please select from among the following supported platforms.
...
27. Linux x86_64, kernelgen-gfortran compiler for CUDA (serial)
28. Linux x86_64, kernelgen-gfortran compiler for CUDA (smpar)
29. Linux x86_64, kernelgen-gfortran compiler for CUDA (dmpar)
30. Linux x86_64, kernelgen-gfortran compiler for CUDA (dm+sm)
Enter selection [1-38] : 27
...
$ ./compile em_real
...
$ cd test/em_real/
$ kernelgen_runmode=1 ./real.exe
```

Testing COSMO and WRF

KernelGen is able to compile original source code for COSMO and WRF into valid executables. Both models are now being actively tested.

COSMO:

```
$ source -/rpmbuild/CHR00T_release/opt/kernelgen/usr/bin/kernelgen-vars.sh
$ ./setup
Select build configuration:
1. gnu
2. kernelgen
3. path64
Enter the value: 2
Configured build for kernelgen
...
5 OMPI_FC=kernelgen-gfortran OMPI_CC=kernelgen-gcc NETCDF=-/rpmbuild/CHR00T_release/opt/kernelgen/usr/ make -j12
...
$ cd .../tests/
$ tar -xjf 2006102312.tar.bz2
$ cd 2006102312/
$ COSMO_NPX=1 COSMO_NPY=8 COSMO_NPIO=0 ./run_eu
```

Collaboration proposal

KernelGen team is seeking for opportunities to:

- 1 Help research groups to evaluate KernelGen in different applications on GPU-enabled HPC facilities
- Encourage contributions to existing development plan (tiling, parallelism detection in sparse data algorithms, and many more) and new proposals involving LLVM, Polly/CLooG, NVPTX and AsFermi
- Offer entire open-source GPU compiler framework as a unified platform for compiler optimizations research

It is also possible to use KernelGen as a base for OpenACC compiler development!



Download link for this presentation: http://kernelgen.org/gtc2013/

Project mailing list: kernelgen-devel@lists.hpcforge.org

Thank you!





