Intel® AVX-512 and its support in LLVM

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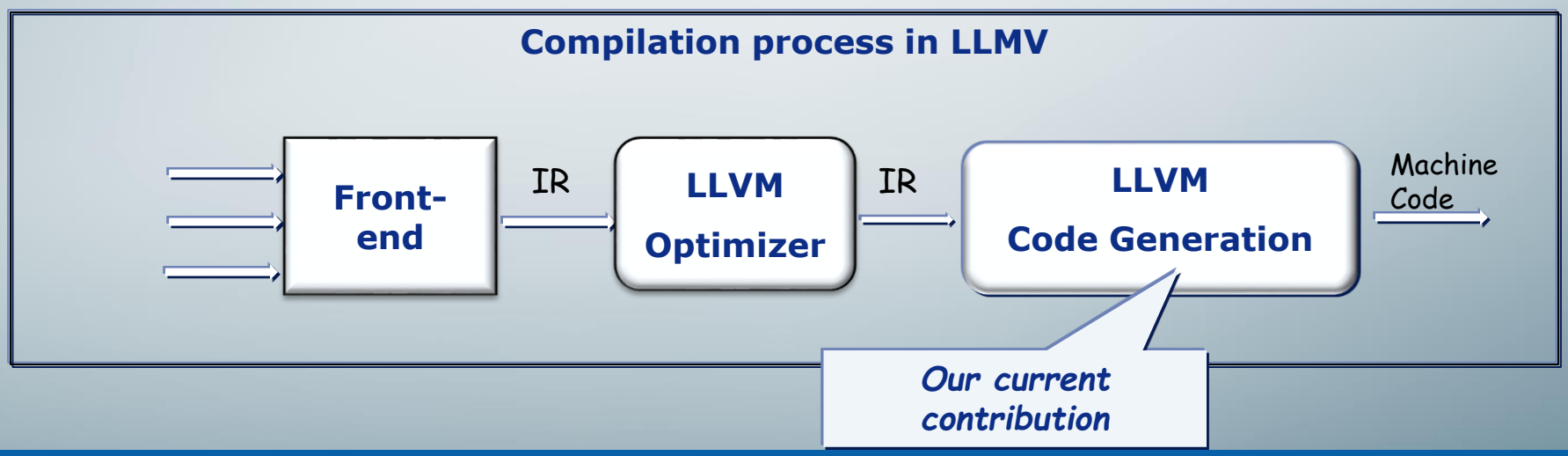
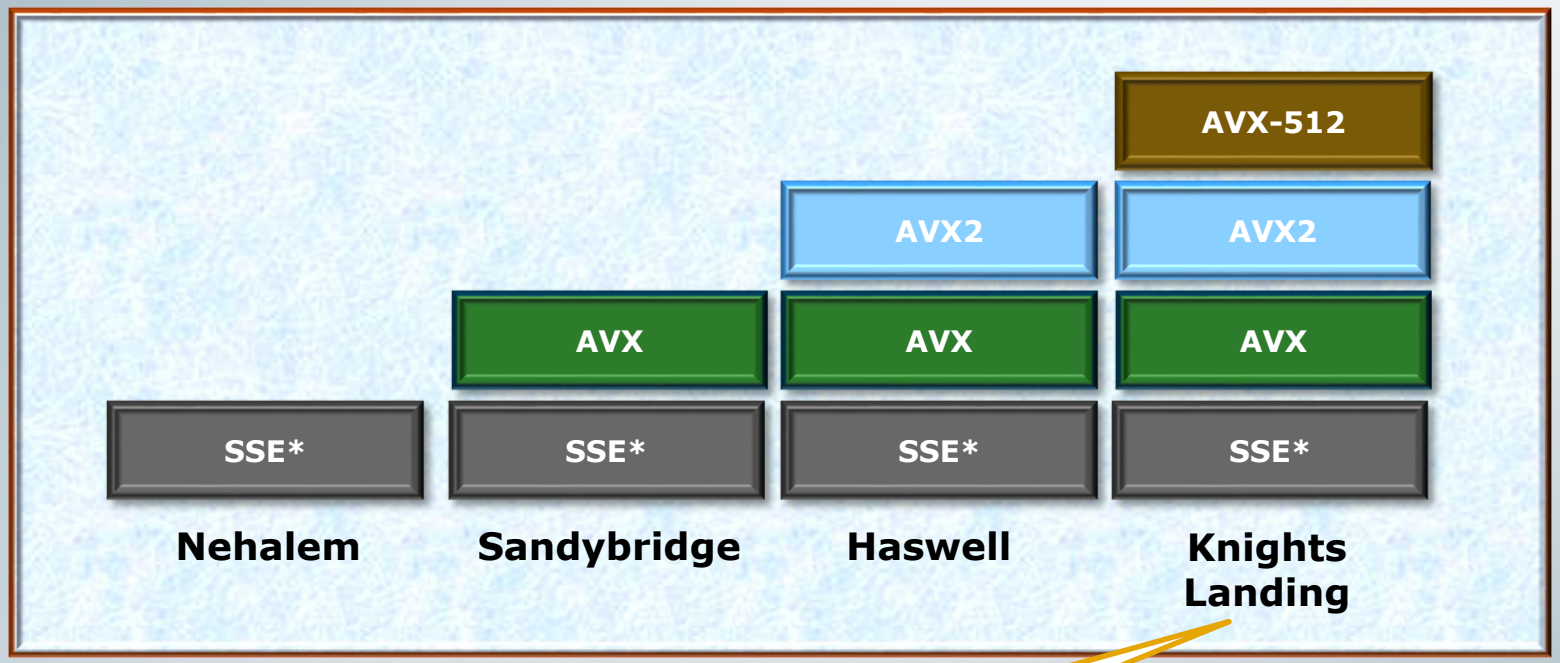
LLVM

- LLVM is a collection of modular and reusable compiler and toolchain technologies.
  - Open Source Project with many contributors
  - Supports many targets, including multiple generations of Intel® processors
- Our OpenCL CPU backend is based on LLVM
- We started adding AVX-512 ISA to LLVM since July 2013



Intel® AVX-512 – KNL processor

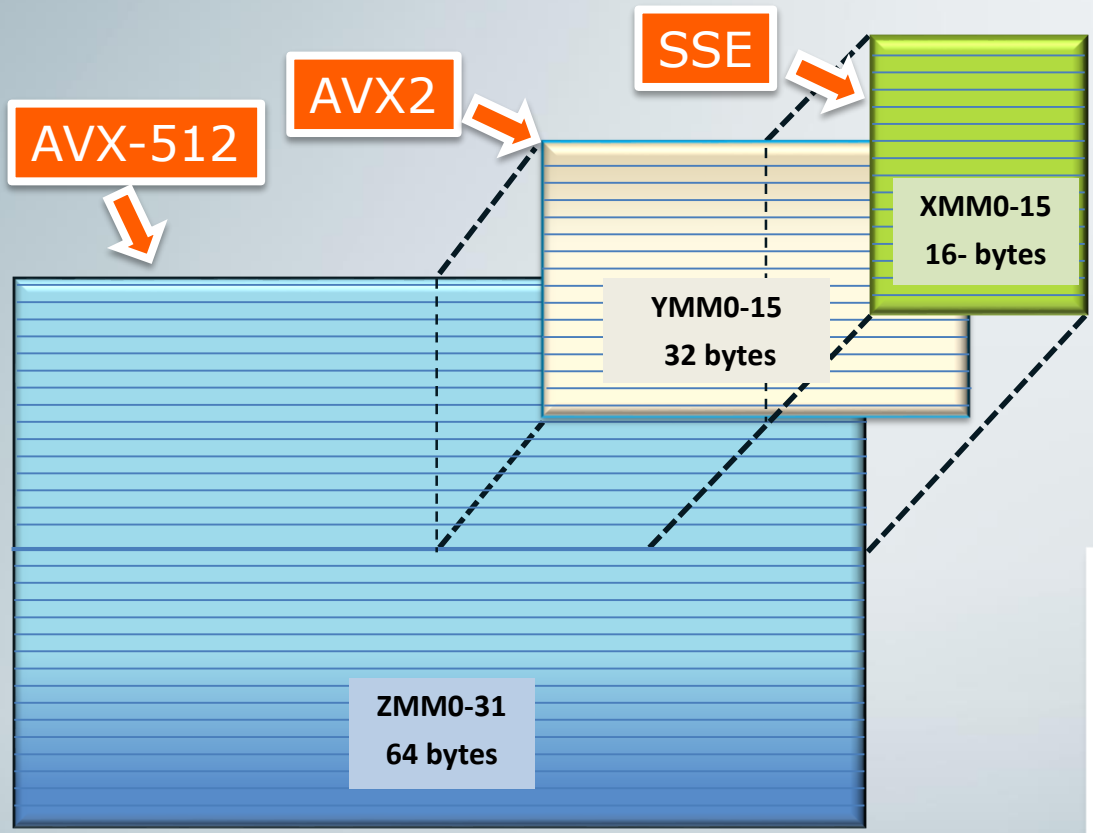


KNL – 2nd generation MIC architecture product

Intel® AVX-512 – Comprehensive vector extension for HPC

- ***Parallel computation***
  - ***More and wider SIMD registers***
  - ***Masking***
  - ***Gather and Scatter***
  - ***Compress and Expand***
  - ***Conflict Detection***
- ***Do more in one instruction***
  - ***FP rounding mode per instruction***
  - ***Embedded Broadcast***
  - ***2-source vector shuffles***
- ***Math support***
  - ***New math instructions***

Greatly increased register file



32 x 512 bit registers

Higher throughput

Greatly improved unrolling and inlining opportunities

Wider data vector

AVX2

```
float A[N], B[N], C[N]

for(i=0; i<8; i++)
{
      C[i] = A[i] + B[i];
}
```

```
VADDPS YMM0, YMM1, YMM2
```

16 x 256-bit registers
In each register:
8 float or 4 double
8 integer or 4 long

AVX-512

```
float A[N], B[N], C[

for(i=0; i<16; i++)
{
      C[i] = A[i] + B[i];
}
```

```
VADDPS ZMM0, ZMM1, ZMM2
```

32 x 512-bit registers
In each register:
16 float or 8 double
16 integer or 8 long

Supported in LLVM:

- AVX-512 instruction set
- New wide registers
- New data types
- Instruction selection algorithm

Masking

- 8 new 64-bits mask registers k0-k7

CMPPS k1, zmm21, zmm31

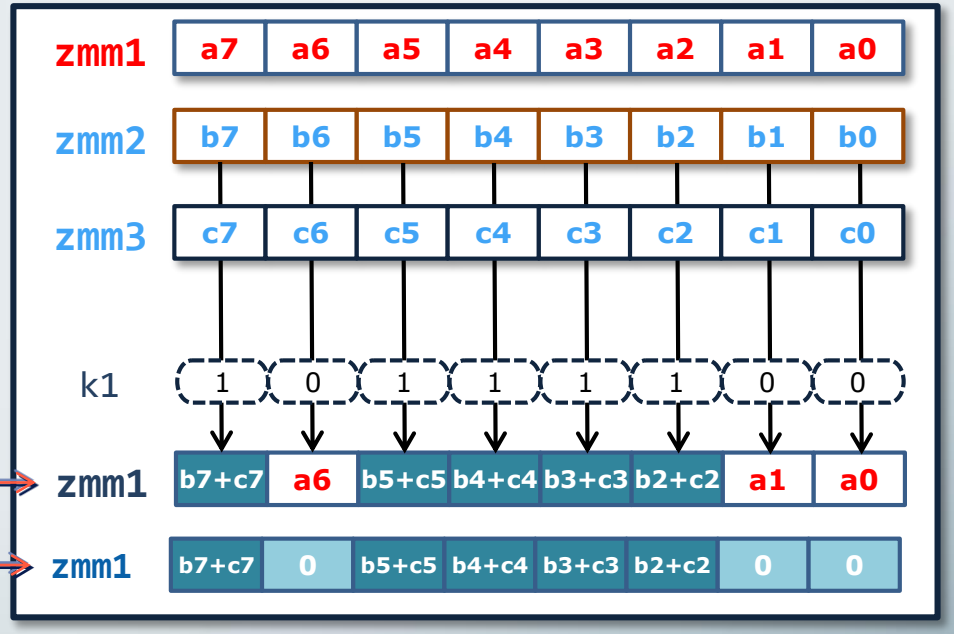
k1 = …0101100111

Unmasked elements remain unchanged:

VADDPD **zmm1** {k1}, zmm2, zmm3

Or zeroed:

VADDPD zmm1 {k1} {z}, zmm2, zmm3



Why masking?

- Memory fault suppression
  - if-conditional statements or loop remainders
- Avoid FP exceptions
- Zeroing/merging
  - Use zeroing to avoid false dependencies
  - Use merging to avoid extra blends

Code Example

```
float A[N], B[N], C[N];

for(i=0; i<16; i++)
{
  if (B[i] != 0)
    A[i] = A[i] / B[i];
  else
    A[i] = A[i] * C[i];
}
```

```
VMOVUPS zmm2, A[16]
VCMPPS k1, zmm0, B
VDIVPS  zmm1 {k1}{z}, zmm2, B
KNOT k2, k1
VMULPS  zmm1 {k2}, zmm2, C
VMOVUPS A[16], zmm1
```

Supported in LLVM:

- Mask registers and data types
- Generation and encoding of masked instructions

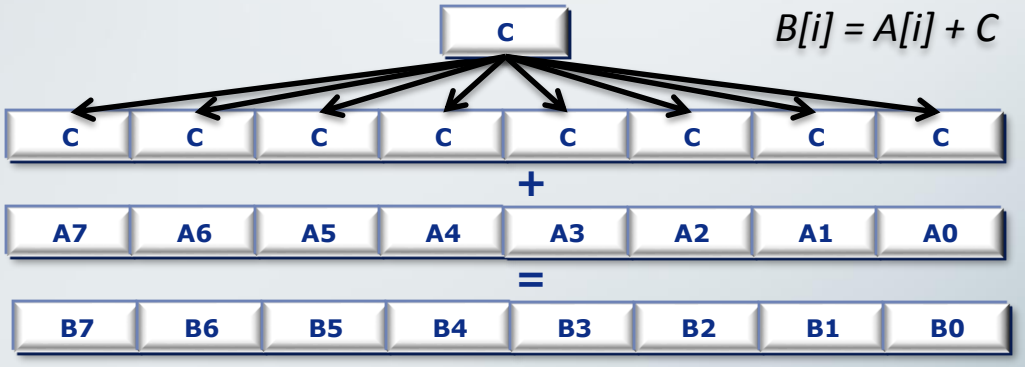
Code with masks is not generated by LLVM yet

Embedded Broadcast

Broadcast one scalar from memory into all vector elements

```
long A[N], B[N], C

for(i=0; i<8; i++)
{
  B[i] = A[i] + C;
}
```




```
vpbroadcastq zmm3, [rax]
vpaddq zmm1, zmm2, zmm3
```

```
vpaddq zmm1, zmm2, [rax] {1to8}
```

Supported in LLVM:

- Logic for folding broadcast into another operation

Compressed Store and Expanded Load

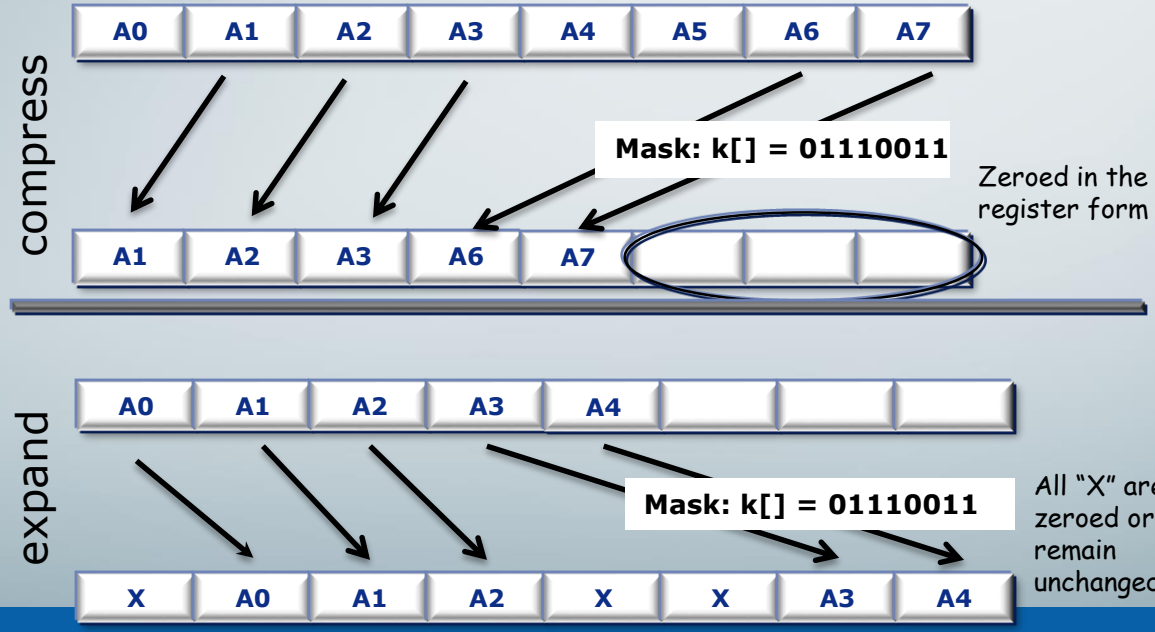
```
double A[N], B[N], C[N];

for(i=0; i<8; i++)
{
  if (B[i] != 0)
    *dst++ = A[i];
}
```

```
VMOVUPD zmm2, A[8]

VCMPPD k1, zmm0, B

VCOMPRESSPD [dst] {k1}, zmm2
```



LLVM:

- Compress/Expand algorithm is not supported yet

Conflict detection

Sparse computations are hard for vectorization

```
for(i=0; i<16; i++)
{
  j = B[i];
  A[j] = C[i] + D[i];
}
```

```
j = vload &B[i]          // Load 16 B[i]
val_A = C + D            // Compute new val
vscatter A, j, val_A     // Update A[j]
```

```
for(i=0; i<16; i++)
{
 j = B[i];
 A[j]++;
}
```

```
j = vload &B[i]          // Load 16 B[i]
val_A = vgather A, j     // Grab A[B[i]]
val_A++                  // Compute new val
vscatter A, j, val_A     // Update A[B[i]]
```

! Code above is wrong if any values within B[i] are duplicated

Conflict Detection – how does it work?

Conflict Free Code

```
for(i=0; i<16; i++)
{
  j = B[i];
  A[j]++;
}
```

```
j = vload &B[i]
pending_elts = 0xFFFF;
do {
  mask = conflict_free(j, pending_elts)
  val_A = vgather {mask} A, j            // Grab A[j]
  val_A++                                // Compute new values
  vscatter A {mask}, j, val_A            // Update A[j]
  pending_elts ^= mask                   // remove done idx
} while (pending_elts)
```

LLVM:

- Conflict detection is not supported yet - a task for a loop vectorizer

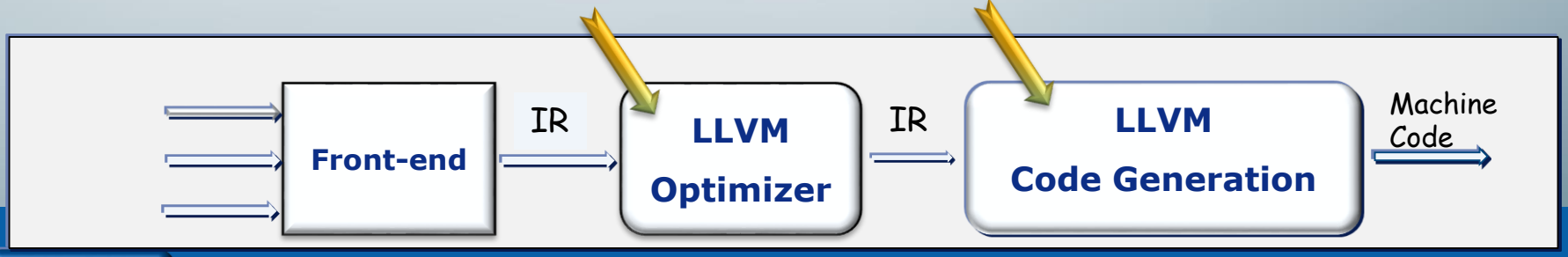
Summary

Currently available

- 99% of the new AVX-512 instructions
- New LLVM data types for wide vectors and masks
- EVEX encoding, instructions with masks and broadcast
- Instruction selection algorithm

Future opportunities – Performance

1. **In the LLVM optimizer**
   - Learn vectorizer to use the conflict detector
   - Use compress and expand capabilities
2. **In code generator**
   - Optimize instruction scheduling
   - Enhance instruction selection algorithm
   - Late machine code optimization phase - set masks to avoid extra blends.



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Embedded Rounding Control & SAE (Suppress All Exceptions)

Static (per instruction) Rounding Mode .

Ignoring the value of RM bits in MXCSR.

```
VADDPS          zmm7 {k6}, zmm2, zmm4 {rd}
VCVTDQ2PS       zmm1, zmm2 {ru}
```

SAE is always implied by using embedded rounding mode

Why?

- Avoid MXCSR access – slow and cumbersome

- Set rounding mode per instruction
  - Simplifies development of high performance math software sequences