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Roy Chan Specialties in ASIC Design and Verification from front-end to back-end activities, including RTL coding, verification (testbench development, testcase generation and test regression), logic synthesis, static timing analysis, Place and route, power analysis, ECO and final tapeout process.

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1. Answer questions in ff_reset_verilog.v and discuss with your TA. Divider RTL design in Verilog Objective This module will introduce you to RTL coding style for state machine and datapath coding. It will also further your understanding of basic Verilog syntax (case, if-else, always, assign, etc.).

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