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Sushanth KJ, Asst. Pr of. Dept. of ECE, BIT, Mangaluru Page 8 VLSI Lab Viva questions and answers Hold Time: The after the active clock edge of the flip-flop, the input should be stable. If the signal changes during this interval, the output of that flip-flop cannot be predictable (called metastable).

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Low Power Circuits and Systems Ajit Pal Professor ... Q1. Why low power has become an important issue in the present day VLSI circuit realization? Q2. How reliability of a VLSI circuit is related to its power dissipation? Q3. How environment is affected by the power ... Answer to Questions of LecAnswer to Questions of Lec--1 Q1. Why low power ...

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