Quaid-e-Awam University of Engineering, Science and Technology

بسم الله الرحمن الرحيم

In the name of Allah, the Most Merciful, the Most Kind

Date: 19-11-2021

BCS 103
Digital Logic & Computer Architecture

Lecture 35 and 36

Department of Computer Science

LAST LECTURE

In the Last Lecture

- **Sequential Logic Circuits**
- **SR Flip-Flop**
- **RS Flip-Flop**
- **Clocked SR/ RS Flip-Flop**

TODAY'S LECTURE

Today we will discuss about:

- **JK Flip-Flop**
- **T Flip-Flop**
- **D Flip-Flop**

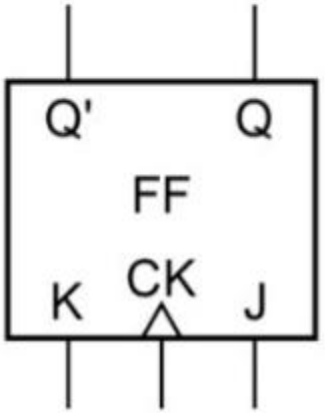
JK Flip Flop

JK Flip-Flop

- The JK Flip-Flop has three inputs
  - Clock (Ck) --- denoted by the small arrowhead
  - J and K
- Similar to the SR Flip-Flop
  - J corresponds to S: $J = 1 \rightarrow Q^+ = 1$
  - K corresponds to R: $K = 1 \rightarrow Q^+ = 0$
- Different from the SR Flip-Flop in that the input combination J = 1, K = 1 is allowed.
  - J = K = 1 causes the Q output to toggle after an active clock edge.

JK Flip-Flop

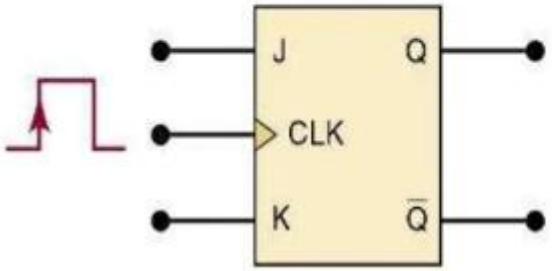
J	K	Q	Q^+	
0	0	0	0	$Q^+ = Q$ store
0	0	1	1	
0	1	0	0	$Q^+ = 0$ reset
0	1	1	0	
1	0	0	1	$Q^+ = 1$ set
1	0	1	1	
1	1	0	1	$Q^+ = Q'$ toggle
1	1	1	0	



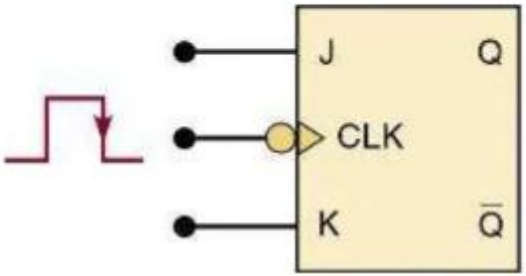
Characteristic Equation:

$Q^+ = J.Q' + K'.Q$

JK Flip Flop



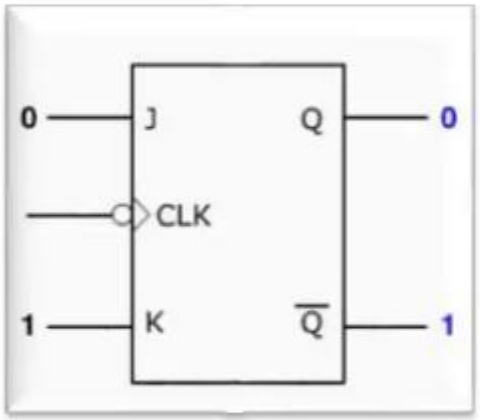
J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q_0}$ (toggles)

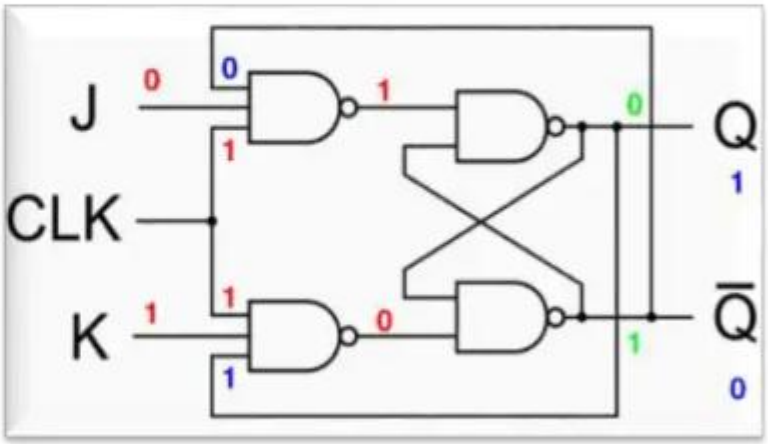


J	K	CLK	Q
0	0	↓	Q_0 (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	$\overline{Q_0}$ (toggles)

Mode of Operation: Reset

Reset: Q = 0.

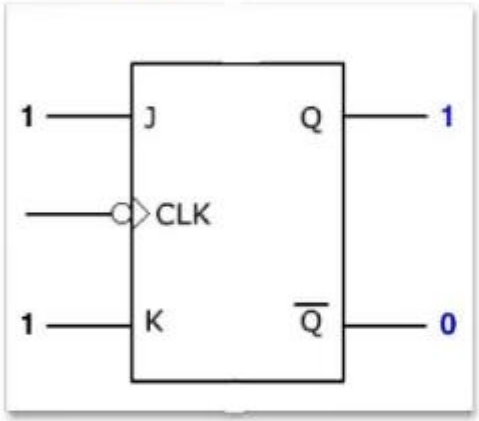


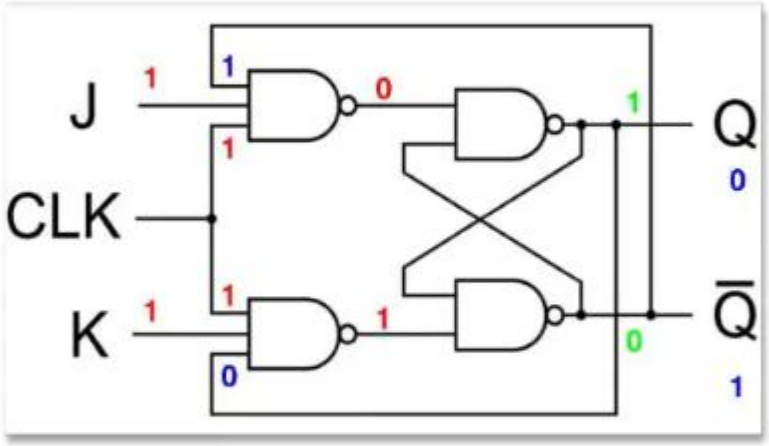


J	K	Q	Q'	Orig. Q	Orig. Q'
0	1	0	1	1	0

Mode of Operation: Toggle

Toggle: Q = Q'.

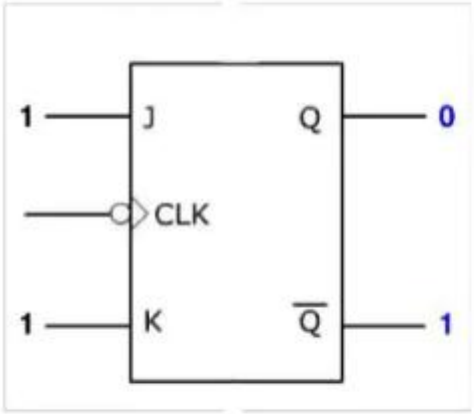


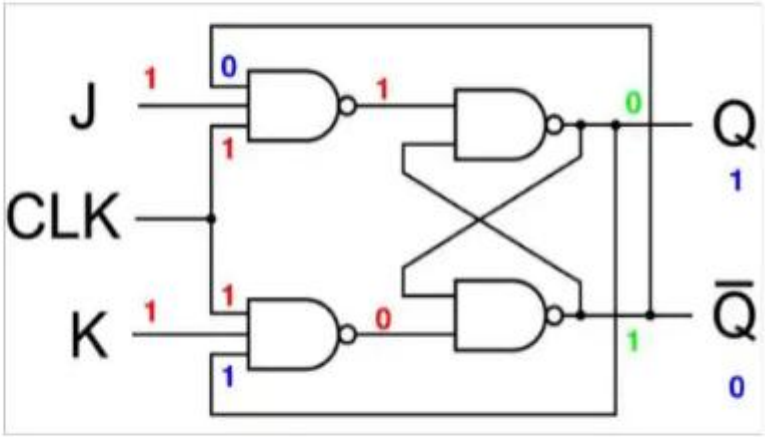


J	K	Q	Q'	Orig. Q	Orig. Q'
1	1	1	0	0	1

Mode of Operation: Toggle again

Toggle: Q = Q'.





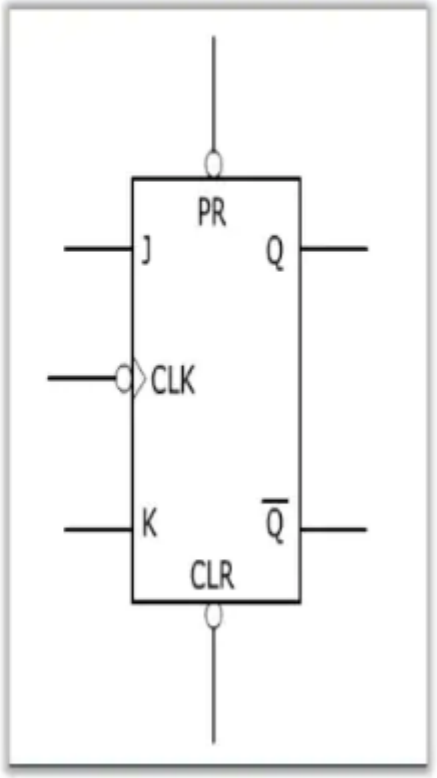
J	K	Q	Q'	Orig. Q	Orig. Q'
1	1	0	1	1	0

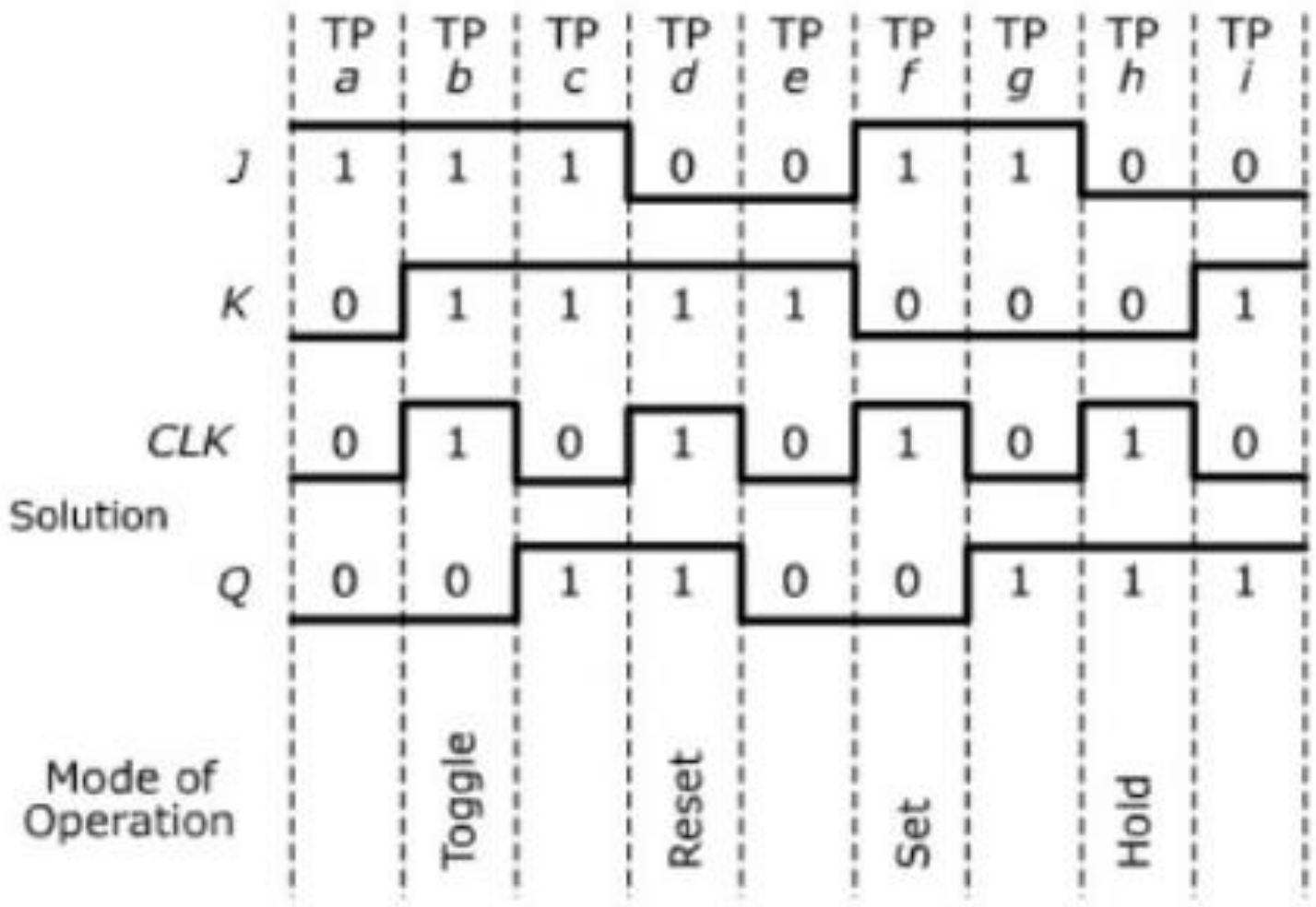
Characteristic Equation

$$Q(t+1) = J.Q' + K'.Q$$

Q is the primary output.

J	K	Q	Q'	Mode
0	0	Q	Q'	Hold
1	0	1	0	Sets
0	1	0	1	Resets
1	1	Q'	Q	Toggle



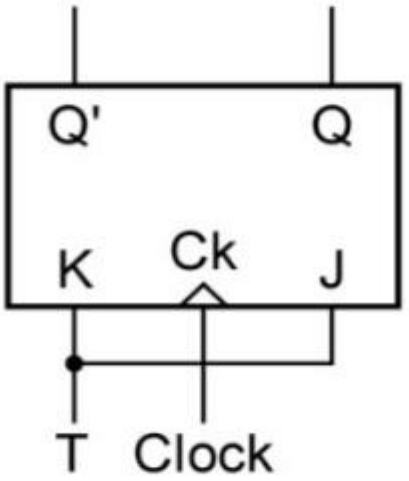

TP a
TP b
TP c
TP d
TP e
TP f
TP g
TP h
TP i
J 1 1 1 0 0 1 1 0 0
K 0 1 1 1 1 0 0 0 1
CLK 0 1 0 1 0 1 0 1 0
Solution
Q 0 0 1 1 0 0 1 1 1
Mode of Operation
Toggle
Reset
Set
Hold

T Flip Flop

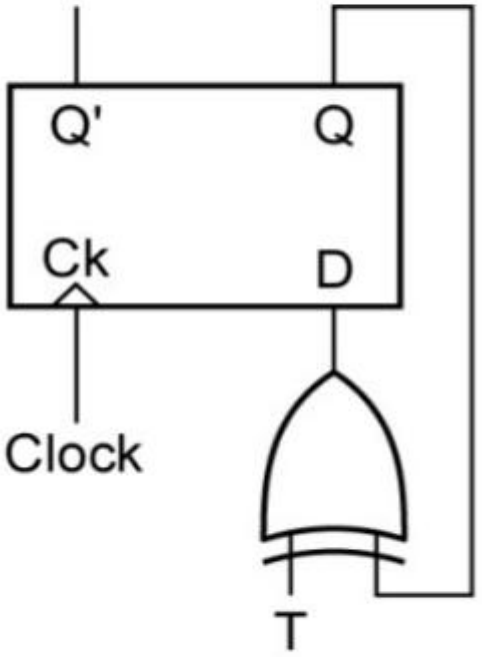
T Flip-Flop

- The Toggle (T) Flip-Flop has two inputs
  - Clock (Ck) --- denoted by the small arrowhead
  - Toggle (T)
- The T input controls the state change
  - when T = 0, the state does not change ($Q^+ = Q$)
  - when T = 1, the state changes following an active clock edge ($Q^+ = Q'$)
- T Flip-Flops are often used in the design of counters.

Building a T Flip-Flop

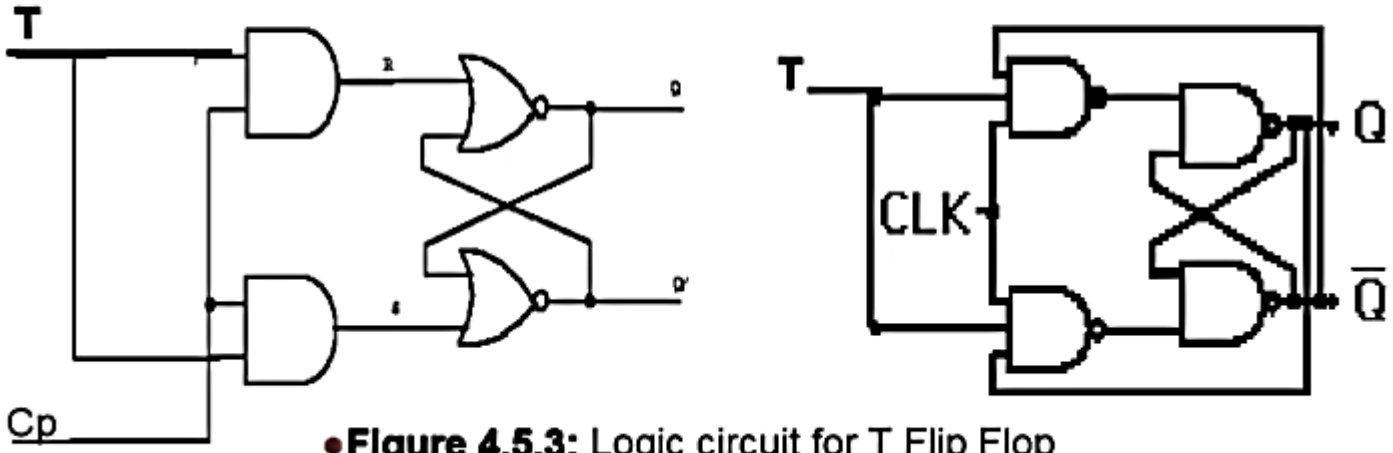


(a) Conversion of J-K to T



(b) Conversion of D to T

T Flip Flop



- **Figure 4.5.3:** Logic circuit for T Flip Flop

T Flip Flop

- **Figure 4.5.1:** Symbol for T Flip Flop

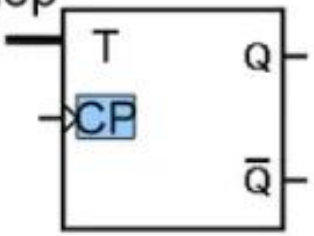
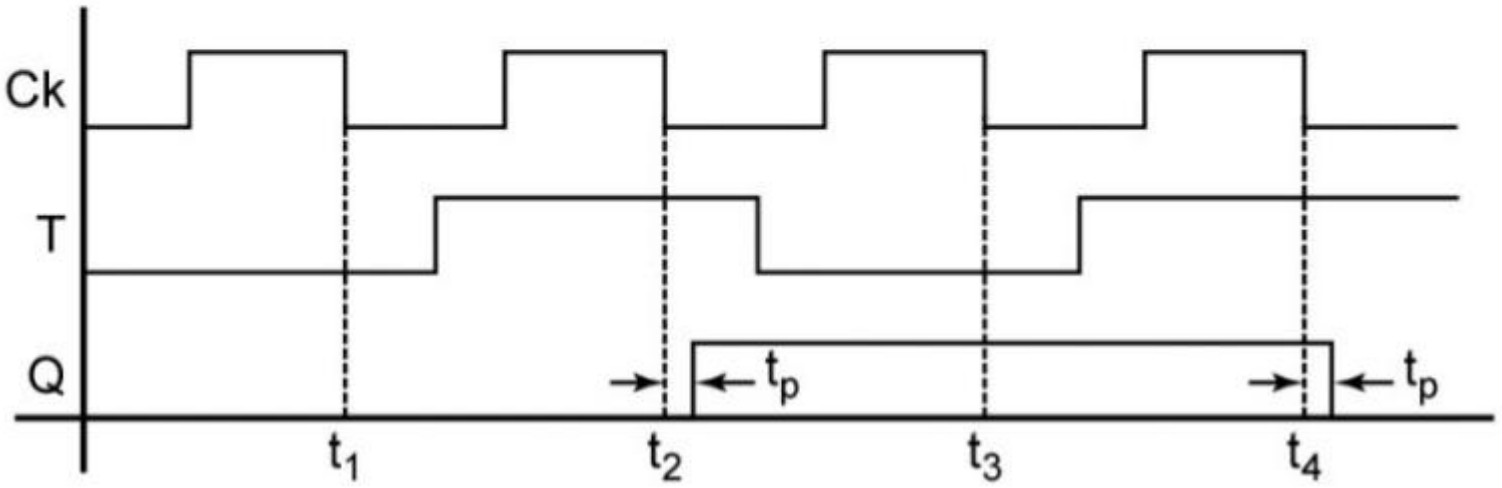


Figure 4.5.2 :Truth Table for T Flip Flop

T	clock	Q	$\overline{Q}$	status
0	↑	Q	$\overline{Q}$	HOLD
1	↑	$\overline{Q}$	Q	TOGOL

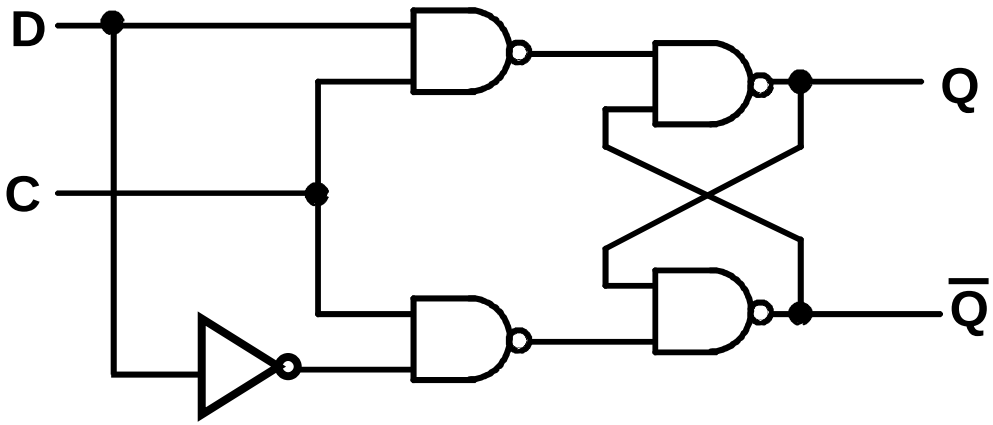
T Flip-Flop: Timing Diagram



D Flip Flop

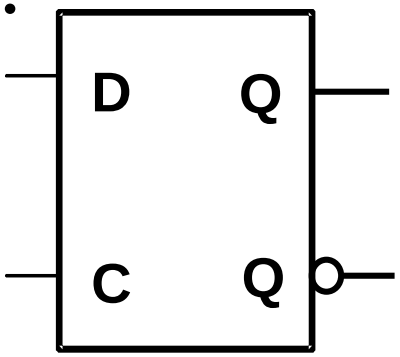
D Flip-Flop

- Adding an inverter to the S-R Latch, gives the D Latch:
- Note that there are no “indeterminate” states!

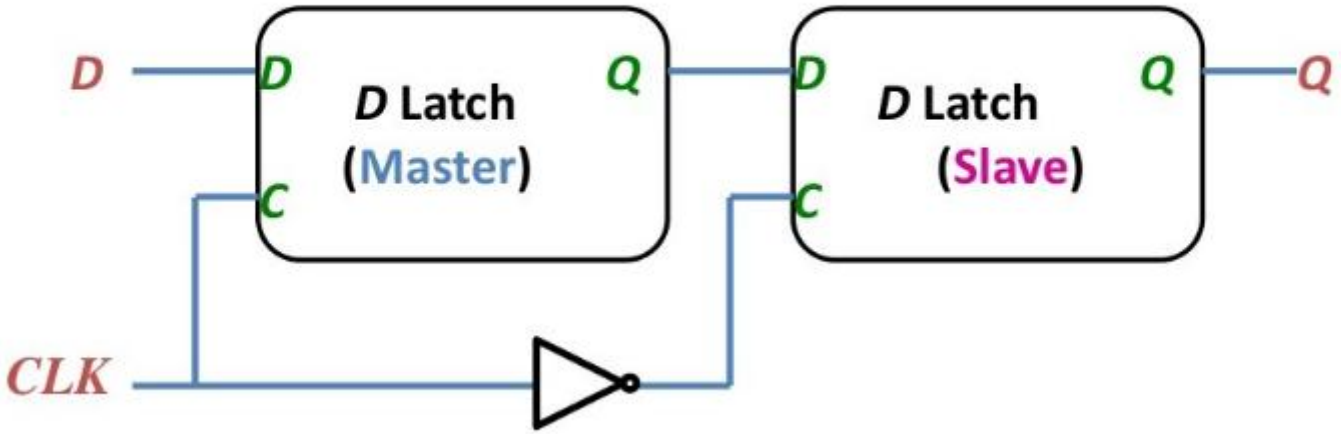


Q	D	Q(t+1)	Comment
0	0	0	No change
0	1	1	Set Q
1	0	0	Clear Q
1	1	1	No Change

The graphic symbol for a D Latch is:



Master-Slave Edge-Triggered Flip-Flop



Thanks