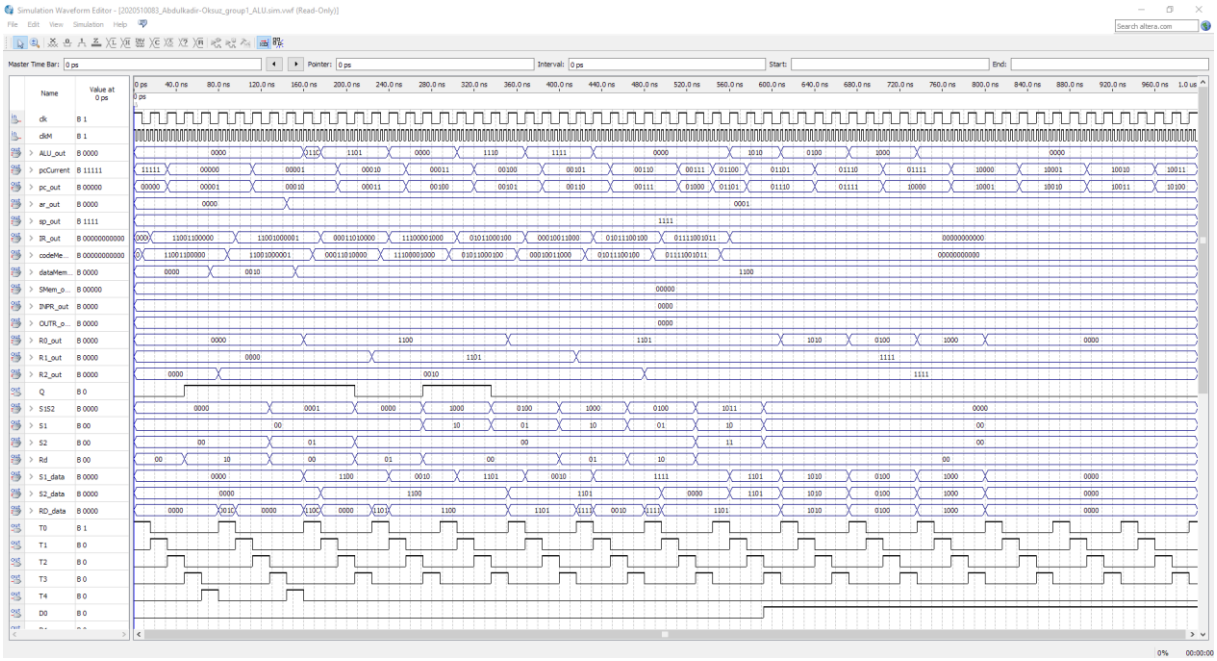
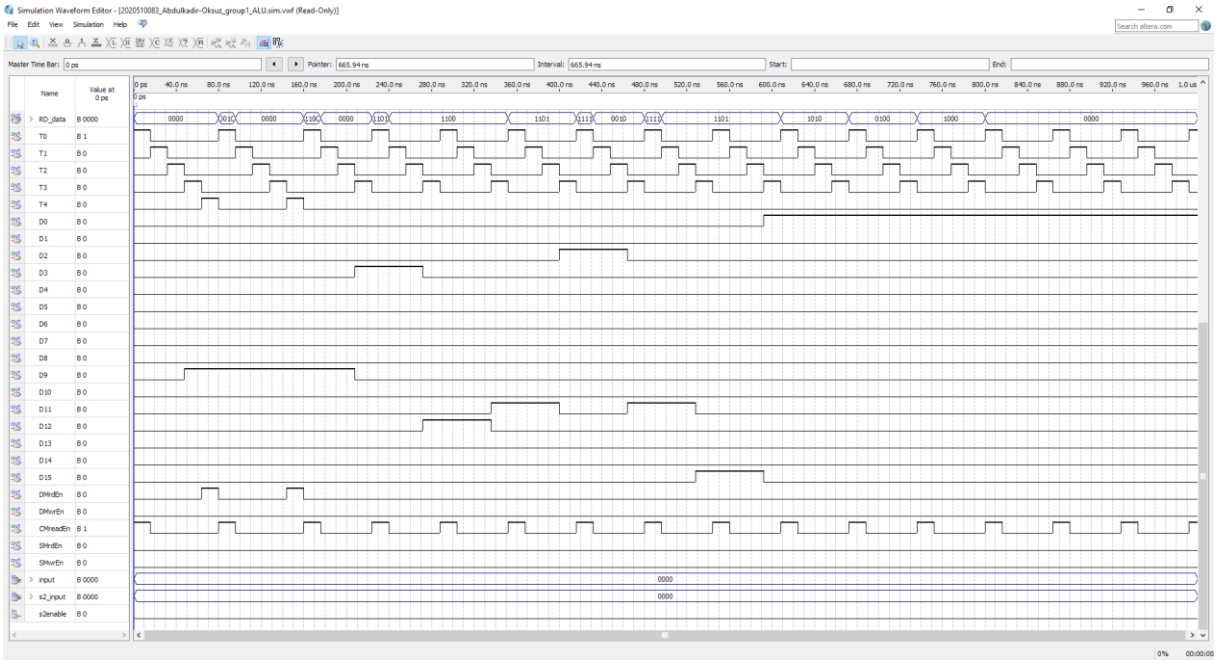
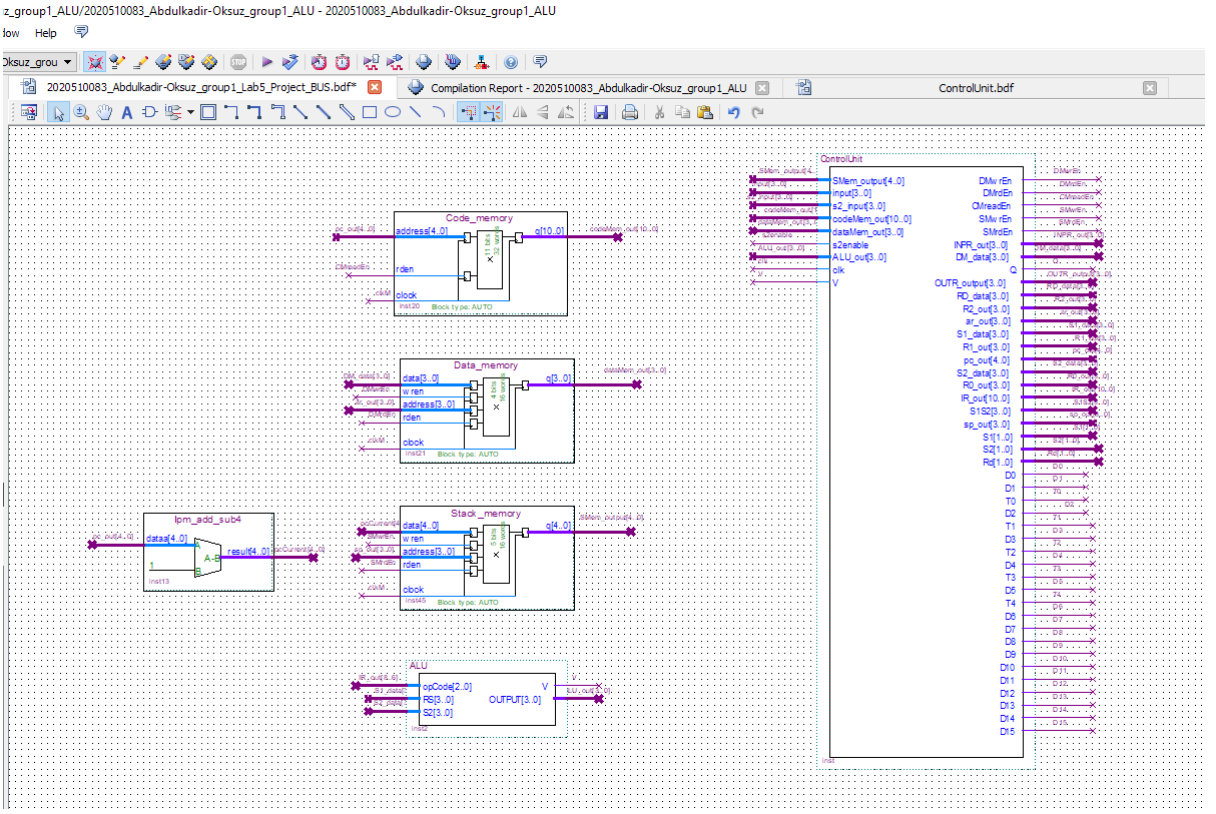
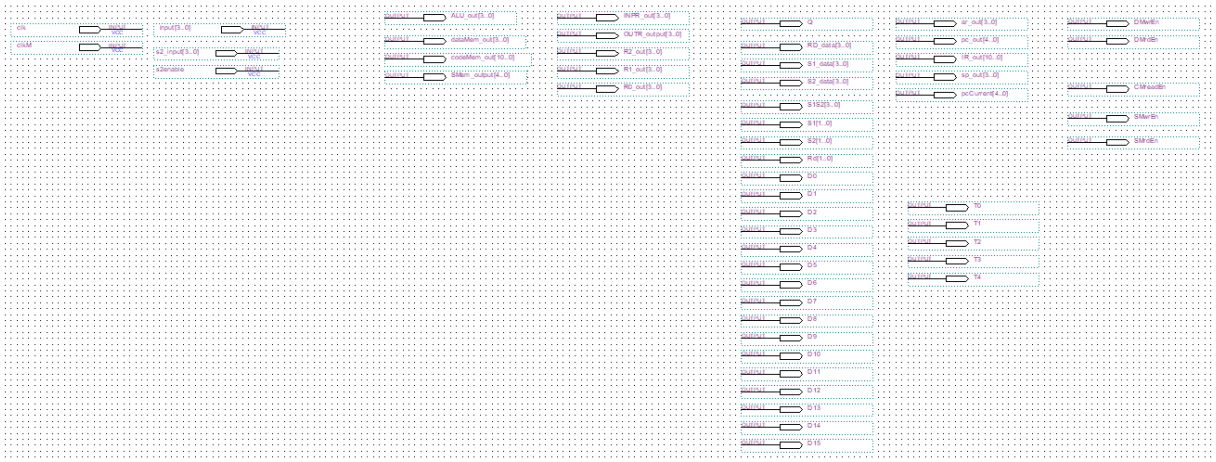
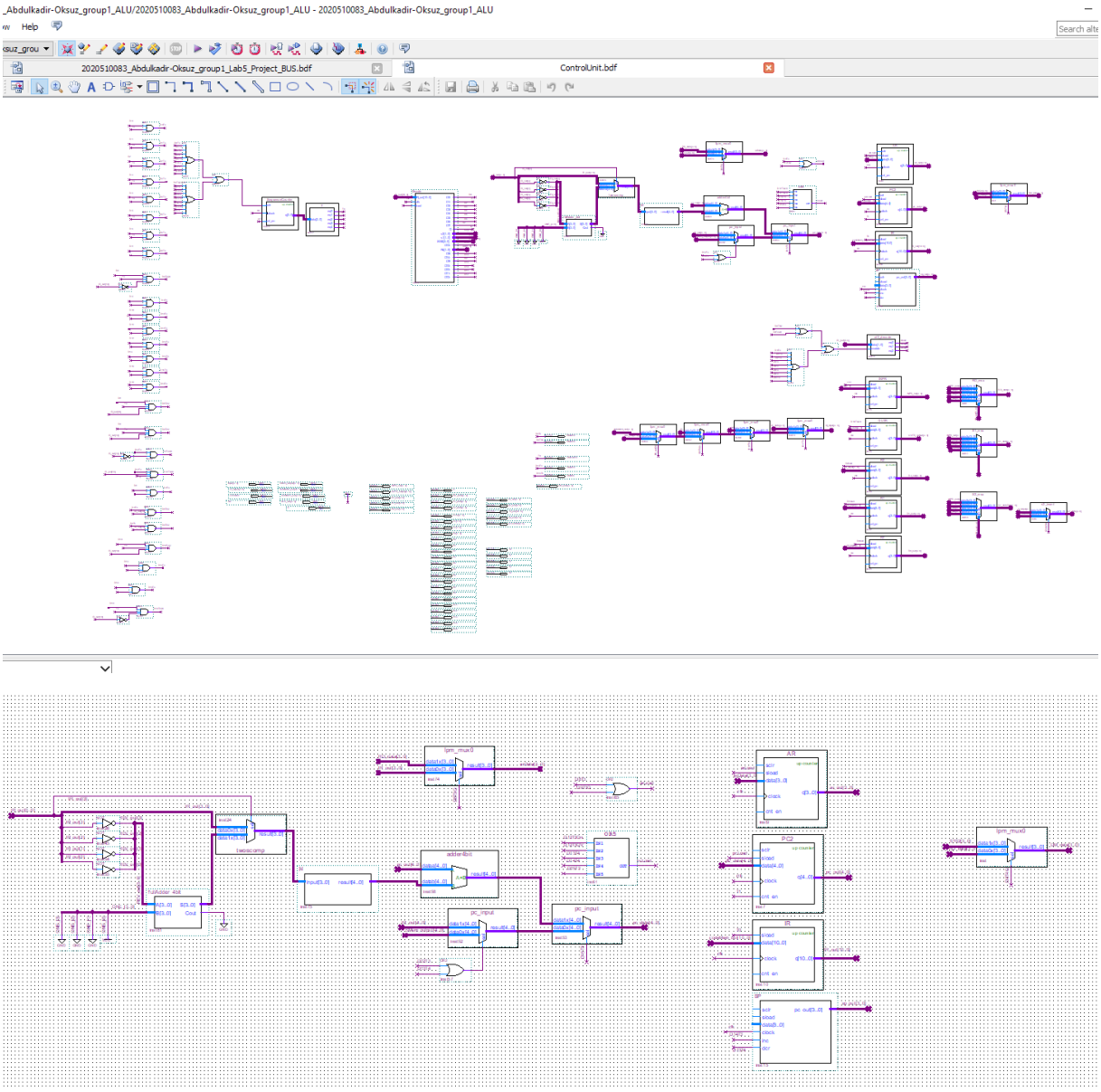

Simulation Waveform Editor - [2020510083_Abdulkadir-Oksuz_group1_ALU.sim.vwf (Read-Only)]
File Edit View Simulation Help
Master Time Bar: 0 ps
Pointer: 0 ps
Interval: 0 ps
Start:
End:
Name
Value at 0 ps
clk
clkM
ALU_out
pcCurrent
pc_out
ar_out
sp_out
IR_out
codeMe...
dataMem...
SMem_o...
INPR_out
OUTR_o...
R0_out
R1_out
R2_out
Q
SIS2
S1
S2
Rd
S1_data
S2_data
RD_data
T0
T1
T2
T3
T4
D0

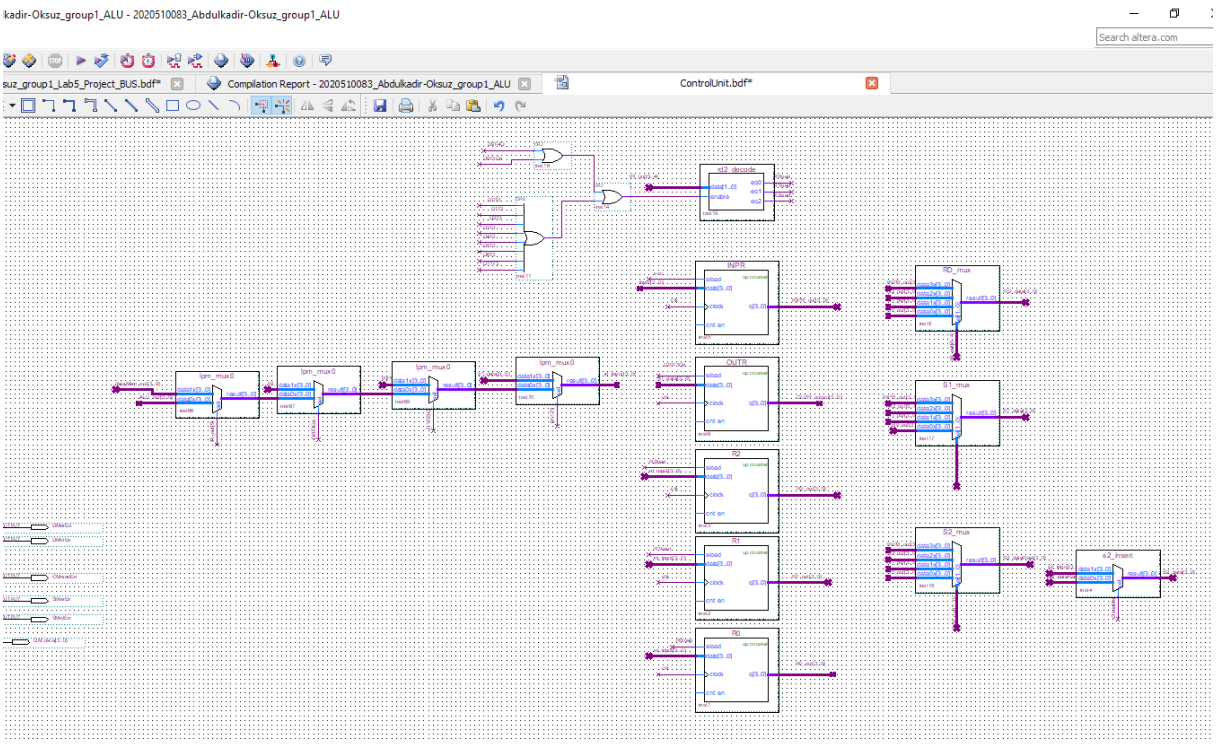

Simulation Waveform Editor - [2020510083_Abdulkadir-Oksuz_group1_ALU.sim.vwf (Read-Only)]
File Edit View Simulation Help
Master Time Bar: 0 ps
Pointer: 665.94 ns
Interval: 665.94 ns
Start:
End:
Name
Value at 0 ps
RD_data
T0
T1
T2
T3
T4
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
DMrdEn
DMwrEn
CMreadEn
SMrdEn
SMwrEn
input
s2_input
s2enable





Control unit bdf:


_Abdulkadir-Oksuz_group1_ALU/2020510083_Abdulkadir-Oksuz_group1_ALU - 2020510083_Abdulkadir-Oksuz_group1_ALU
Help
2020510083_Abdulkadir-Oksuz_group1_Lab5_Project_BUS.bdf
ControlUnit.bdf



Microoperations Table

Fetch	T0:	IR <- IM[PC]
	T1:	PC <- PC + 1
Decode	T2:	Q <- IR(10)

D0,....,D15 <- Decode IR(9-6), Rd <- IR(5-4), S1<- IR(3-2), S2 <- IR(1-0), S1S2 <- IR(3-0)

Execution:

Arithmetic and Logic Operations:

DBL	D0T3:	Rd <- S1 << 2, sc <– 0
DBT	D1T3:	Rd <- S1 >> 2, sc <– 0
ADD	D2T3:	Rd <- S1+S2, sc <– 0
INC	D3T3:	Rd <- S1+1, sc <– 0
AND	D4T3:	Rd <- S1^S2, sc <– 0
NOT	D5T3:	Rd <- S1', sc <– 0
XOR	D6T3:	Rd <- S1 XOR S2, sc <– 0

Q: 1 (SİNYAL)

Data Transfer

ST D8Q'T3: AR <- IR[3..0]

D8Q'T4: DM[AR] <- Rd , sc <-- 0

D8QT3: AR <- Rd (Rd 2 ise 2. register içindeki değer)

D8QT4: DM[AR] <- IR[3..0] , sc <-- 0

LD D9QT3: AR <- S1S2

D9QT4: Rd <- DM[AR] (DM read sinyali), sc <- 0

D9Q'T3: Rd <- S1S2, sc <- 0

IO D10Q'T3: OUTR <- S1

D10QT3: Rd <- INPR, sc <- 0

İmlecin olduğu yere sc 0 ataması olcak

TSF D11T3: Rd <- S1, sc <- 0

Program Control

JMP D12Q'T3: PC <- IR[4..0], sc <- 0

D12QVT3: PC <- IR[4..0], sc <- 0

CAL D13T3: SM[sp] <- PC

D13T4: PC <- IR[4..0], SP <- SP -1, sc <- 0

RET D14T3: sp <- sp + 1,

D14T4: PC <- SM[sp], sc <- 0

JMR D15T3: PC <- PC + IR[3..0], sc <- 0