

Hardware and virtual machines

21/3/2025

Question 1

- 5 Complete these **three** statements about computer processors.

A processor with a few simple fixed-length instructions that have a small number of instruction formats is called a reduced instruction set processor.

A processor with many complex variable-length instructions that has many instruction formats is called a complex instruction set processor.

Instruction-level parallelism, applied to the execution of instructions during the fetch-execute cycle, is called pipelining

(2)

[3]

Question 2

- 5 Complete these statements about a virtual machine.

A virtual machine is Program that emulates a different computer system.

10 4

A virtual machine allows multiple guests operating systems to run on one computer using a host operating system.

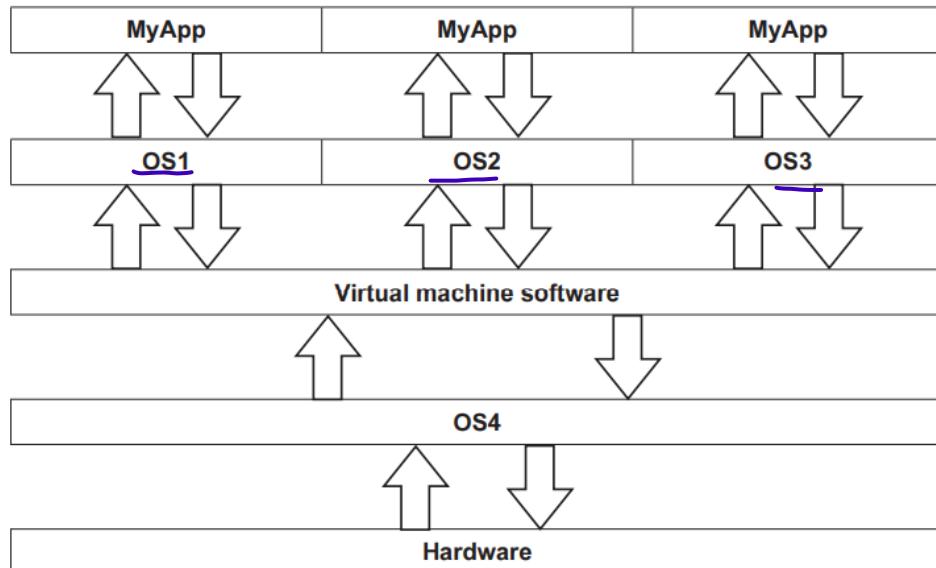
[4]

Question 3

- 6 Mahmoud is developing a new application, MyApp, that needs to work with three different operating systems (OS1, OS2 and OS3).

He has decided to use virtual machine software to test MyApp with these three different operating systems.

The diagram shows MyApp running on three virtual machines.



- (a) Describe the roles of the **four** operating systems (OS1, OS2, OS3 and OS4) shown in the diagram.

OS1, OS2, OS3 -> are guest OS allowing
Mahmoud his App to run on different systems
OS4 -> is the host OS managing the VM
software and directly interacts with the hardware [3]

- (b) Describe the role of the virtual machine software in the testing of MyApp.

Create/edits/delete a virtual soft machine
Manages the resources of Guest OS and allows
multiple instances to host OS
Allows multiple hardware emulation
protects each VM
allows to run multiple instances of MyApp to be tested [3]

- (c) Explain one benefit and one drawback of this approach to testing MyApp.

Benefit May be cheaper than buying dedicated machines to host their software. The

Drawback The performance takes a hit as there is always b/w the OS & my program. The App may not run in its full functionality / perform degraded

[4]

Question 4

- 7 (a) RISC (Reduced Instruction Set Computing) and CISC (Complex Instruction Set Computing) are two types of processor.

Tick (✓) **one** box in each row to show if the statement applies to RISC or CISC processors.

Statement	RISC	CISC
Larger instruction set		✓
Variable length instructions	.	✓
Smaller number of instruction formats	✓	.
Pipelining is easier	✓	
Microprogrammed control unit		✓
Multi-cycle instructions		✓

[3]

- (b) In parallel processing, a computer can have multiple processors running in parallel.

- (i) State the **four** basic computer architectures used in parallel processing.

- 1 SISD
- 2 SIMD
- 3 MIMD
- 4 SIMD

[4]

- (ii) Describe what is meant by a **massively parallel computer**.

It is a super comp large no. of processors working collaboratively together they communicate via a msg interface.

[3]

Question 5

- 9 (a) The following incomplete table shows descriptions relating to computer architectures.

Complete the table by inserting the appropriate terms.

	Description	Term
A	<ul style="list-style-type: none"> There are several <u>processors</u>. <u>m</u> Each processor executes different sets of <u>instructions</u> on one set of data at the same time. 	<u>MISD</u>
B	<ul style="list-style-type: none"> The processor has several ALUs. Each ALU executes the same set of instructions on different sets of data at the same time. 	<u>SIMD</u>
C	<ul style="list-style-type: none"> There is only one processor. The processor executes one set of instructions on one set of data. 	<u>SISD</u>
D	<ul style="list-style-type: none"> There are several processors. Each processor executes a different set of instructions. Each processor operates on different sets of data. 	<u>MIMD</u>

[4]

- (b) State **three** characteristics of massively parallel computers.

1 *large number of processors control together*

2 *control them via msg interface by sending msg*

3 *works collaboratively / coordinated simultaneous processing*

[3]

Question 6

- 5 (a) Most desktop or laptop computers use CISC (Complex Instruction Set Computing) architecture. Most smartphones and tablets use RISC (Reduced Instruction Set Computing).

State **four** features that are different for the CISC and RISC architectures.

1 Smaller Instruction Sets

2 Simple Instructions

3 Single Cycle Processor

4 Allows for pipeline / Reg. Registers

[4]

- (b) In a RISC processor, four instructions (**A, B, C, D**) are processed using pipelining.

The following table shows five stages that take place when instructions are fetched and executed. In time interval 1, instruction **A** has been fetched.

- (i) In the table, write the instruction labels (**A, B, C, D**) in the correct time interval for each stage. Each operation only takes one time interval.

Stage	Time interval								
	1	2	3	4	5	6	7	8	9
Fetch instruction	A	B	C	D					
Decode instruction		A	B	C	D				
Execute instruction			A	B	C	D			
Access operand in memory				A	B	C	D		
Write result to register					A	B	C	D	

[3]

Pipeline Cycle \rightarrow 8

Instruction Pipeline \rightarrow 20

$$\text{No. of cycles} = \frac{20}{8} = 2.5$$

- (ii) When completed, the table in **part (b)(i)** shows how pipelining allows instructions to be carried out more rapidly. Each time interval represents one clock cycle.

Calculate how many clock cycles are saved by using pipelining in the example in **part (b)(i)**.

Show your working.

Working

.....

.....

Answer

[3]

- (c) The table shows four statements about computer architecture.

Put a tick (\checkmark) in each row to identify the computer architecture associated with each statement.

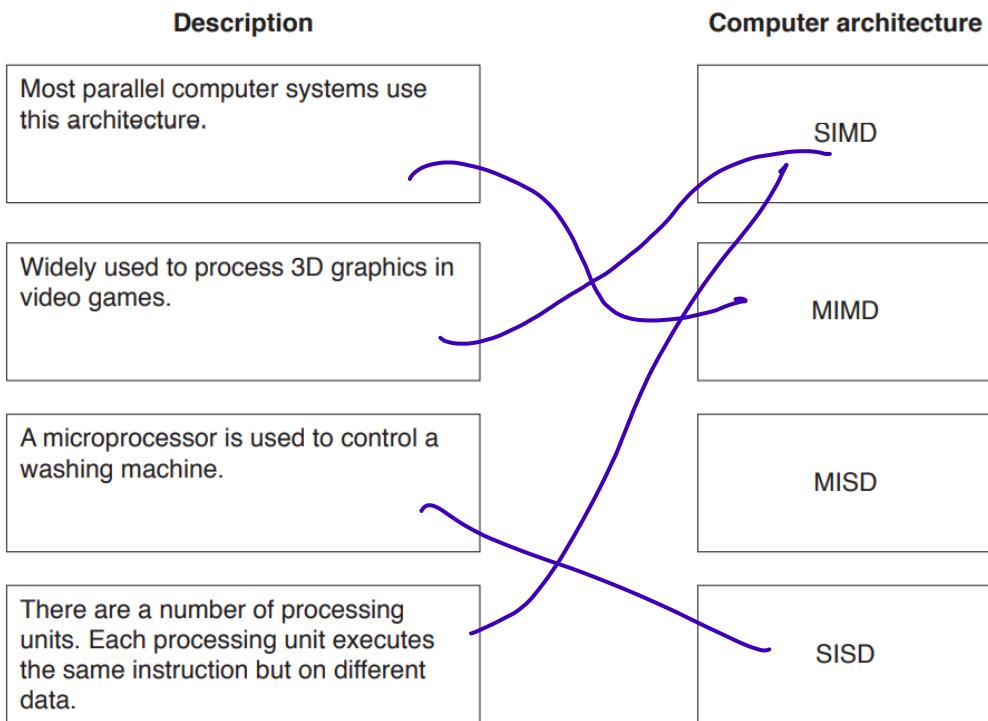
Statement	Architecture		
	SIMD	MIMD	SISD
Each processor executes a different instruction		<input checked="" type="checkbox"/>	
There is only one processor			<input checked="" type="checkbox"/>
Each processor executes the same instruction input using data available in the dedicated memory	<input checked="" type="checkbox"/>		
Each processor typically has its own partition within a shared memory		<input checked="" type="checkbox"/>	

[4]

Question 7

- 2 (a) The following diagram shows four descriptions and four types of computer architecture.

Draw lines to connect each description to the appropriate computer architecture.



[4]

- (b) A computer has a single processor that contains four processing units.

Explain why this is **not** an example of a massively parallel computer.

*: four small programs
be called on
PU are share the same bus*

[2]

- (c) An application has previously executed on a single computer. The application will be transferred onto a massively parallel computer.

The program code used in the application will need to be updated to ensure that the power of the massively parallel computer is fully used.

Explain what changes will be required to the program code.

.....
.....
.....

[2]

- (d) Explain **one** of the hardware issues that will have to be overcome if a massively parallel computer is to function successfully.

.....
.....
.....

[2]

Question 8

- 2 (a) The following diagram shows four descriptions and two types of processor.

Draw lines to connect each description to the appropriate type of processor.

Description	Type of processor
It has a simplified set of instructions.	
Emphasis is on the hardware rather than the software.	CISC
It makes extensive use of general purpose registers.	RISC
Many instruction formats are available.	

[4]

- (b) In a RISC processor, instructions are processed using pipelining.

- (i) Explain what is meant by pipelining.

The process of executing and feeding multiple instructions in parallel.

[2]

- (ii) The following table shows the five stages that occur when instructions are fetched and executed. The table also shows a number of time intervals.

Two instructions, D followed by E, are fetched and executed. The 'E' in the incomplete table shows that instruction E has been fetched in time interval 2.

Complete each row of the table.

Stage	Time interval							
	1	2	3	4	5	6	7	8
Fetch instruction		E						
Read registers and decode instruction								
Execute instruction								
Access operand in memory								
Write result to register								

[3]

- (c) The instruction set for a RISC processor that allows pipelining includes the following instruction.

Instruction		Explanation
Op code	Operands	
ADD	<dest>, <op1>, <op2>	Add the integers in registers op1 and op2. Place the result in register dest.

A program contains the following three instructions.

ADD r3, r2, r1

ADD r5, r4, r3

ADD r10, r9, r8

- (i) Explain why pipelining fails for the first two instructions.

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[2]

- (ii) The instructions were produced by a compiler after translation of a high-level language program.

The compiler is not capable of code optimisation.

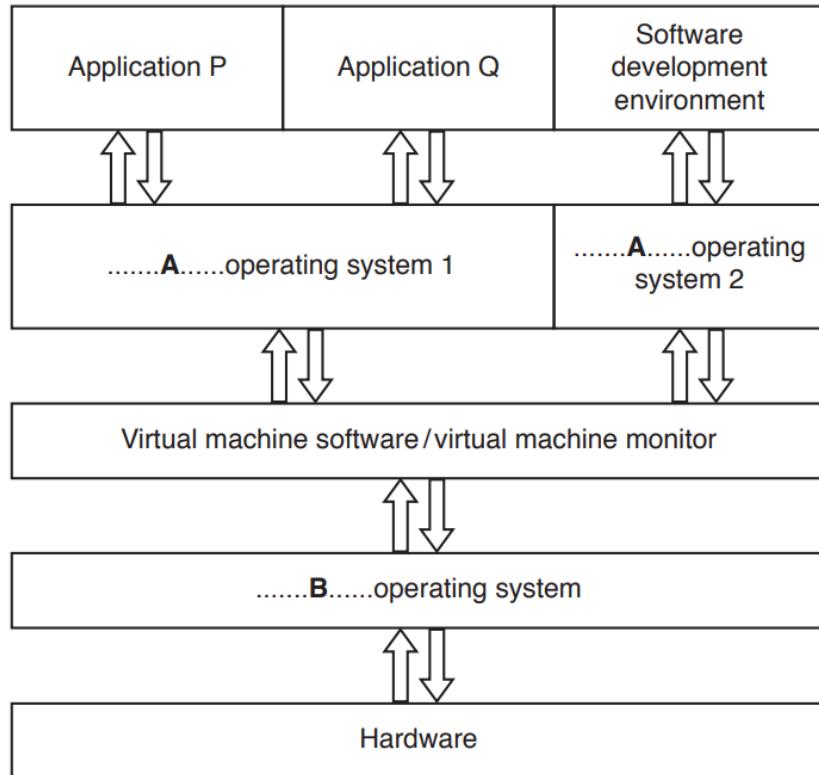
State how the code from the compiler could have been optimised to overcome the problem in part (c)(i).

.....
.....

[1]

Question 9

- 3 (a) This diagram shows how applications P, Q and a software development environment can be run on a virtual machine system.



- (i) State the operating systems labelled **A** and **B** in the diagram.

A

B

[2]

- (ii) Application P is executing and requests data from a file.

Describe what happens after**A**.....operating system 1 has received the data request from the application.

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[3]

- (b) A software development company uses virtual machines to produce software.

- (i) State **one** benefit to the company.

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[1]

- (ii) Explain **two** limitations of this approach.

Limitation 1

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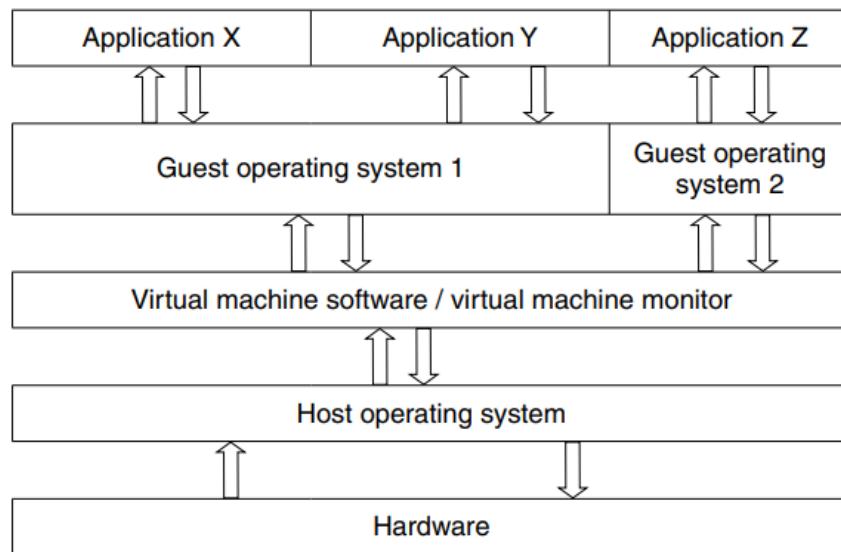
Limitation 2

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[4]

Question 10

- 3 (a) The following diagram shows how applications X, Y and Z can run on a virtual machine system.



- (i) The virtual machine software undertakes many tasks.

Describe **two** of these tasks.

Task 1

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Task 2

..... [2]

- (ii) Explain the difference between a **guest operating system** and a **host operating system**.

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..... [2]

- (b) A company uses a computer as a web server. The manufacturer will no longer support the computer's operating system (OS) in six months' time. The company will then need to decide on a replacement OS.

The company is also considering changing the web server software when the OS is changed.

Whenever any changes are made, it is important that the web server service is not disrupted.

In developing these changes, the company could use virtual machines.

- (i) Describe **two** possible uses of virtual machines by the company.

Use 1

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Use 2

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[4]

The web server often has to handle many simultaneous requests.

- (ii) The company uses a virtual machine to test possible solutions to the changes that they will need to make.

Explain **one** limitation of this approach.

.....
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.....
.....

[2]

Question 11

- 4 (a) Three descriptions and two types of processor are shown below.

Draw a line to connect each description to the appropriate type of processor.

Description	Type of processor
Makes extensive use of general purpose registers	RISC
Many addressing modes are available	CISC
Has a simplified set of instructions	

[3]

- (b) In a RISC processor three instructions (A followed by B, followed by C) are processed using pipelining.

The following table shows the five stages that occur when instructions are fetched and executed.

- (i) The 'A' in the table indicates that instruction A has been fetched in time interval 1.

Complete the table to show the time interval in which each stage of each instruction (A, B, C) is carried out.

Stage	Time interval								
	1	2	3	4	5	6	7	8	9
Fetch instruction	A								
Decode instruction									
Execute instruction									
Access operand in memory									
Write result to register									

[3]

- (ii) The completed table shows how pipelining allows instructions to be carried out more rapidly. Each time interval represents one clock cycle.

Calculate how many clock cycles are saved by the use of pipelining in the above example.

Show your working.

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[3]

Question 12

- 4 (a) Four descriptions and four types of computer architecture are shown below.

Draw a line to connect each description to the appropriate type of computer architecture.

Description	Computer architecture
A computer that does not have the ability for parallel processing.	SIMD
The processor has several ALUs. Each ALU executes the same instruction but on different data.	MISD
There are several processors. Each processor executes different instructions drawn from a common pool. Each processor operates on different data drawn from a common pool.	SISD
There is only one processor executing one set of instructions on a single set of data.	MIMD

[4]

- (b) In a massively parallel computer explain what is meant by:

(i) Massive
.....
..... [1]

(ii) Parallel
.....
..... [1]

- (c) There are both hardware and software issues that have to be considered for parallel processing to succeed.

Describe **one** hardware and **one** software issue.

Hardware

.....

.....

Software

.....

.....

[4]

Answers

Answer 1

5	<ul style="list-style-type: none"> • RISC / reduced instruction set computer • CISC / complex instruction set computer • Pipelining 	3
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Answer 2

5	<p>Software / a program Physical / different Guest Host</p>	4
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Answer 3

6(a)	<p>Max three, one mark for role, one mark for expansion OS1, OS2 and OS3 are guest operating systems ... secondary to the one installed on the hardware OS4 is the host operating system ... interacts directly with the machine hardware MyApp needs to run on all three guest operating systems with identical results</p>	3
6(b)	<p>Any three from Create/delete/manage virtual machine Translate instructions used by guest operating system to that required by host operating system Hardware emulation Protecting each virtual machine ... so instances of MyApp can be tested together</p>	3
6(c)	<p>One mark for benefit and one mark for relevant explanation One mark for drawback one mark for relevant explanation</p> <p>For example:</p> <p>Benefit: multiple operating systems can exist simultaneously ... allowing for testing using the same hardware only one set of hardware required ... reduces cost of producing the app // no need to set up more than one computer</p> <p>Drawback: execution of extra code ... so performance is degraded // more time taken to execute the app // cannot make judgements about response time etc</p>	4

Answer 4

7(a)	<p>1 mark for 2/3 rows correct 2 marks for 4/5 rows correct 3 marks for 6 correct rows</p> <table border="1"> <thead> <tr> <th>Statement</th><th>RISC</th><th>CISC</th></tr> </thead> <tbody> <tr> <td>Larger instruction set</td><td></td><td>✓</td></tr> <tr> <td>Variable length instructions</td><td></td><td>✓</td></tr> <tr> <td>Smaller number of instruction formats</td><td>✓</td><td></td></tr> <tr> <td>Pipelining is easier</td><td>✓</td><td></td></tr> <tr> <td>Microprogrammed control unit</td><td></td><td>✓</td></tr> <tr> <td>Multi-cycle instructions</td><td></td><td>✓</td></tr> </tbody> </table>	Statement	RISC	CISC	Larger instruction set		✓	Variable length instructions		✓	Smaller number of instruction formats	✓		Pipelining is easier	✓		Microprogrammed control unit		✓	Multi-cycle instructions		✓	3
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Pipelining is easier	✓																						
Microprogrammed control unit		✓																					
Multi-cycle instructions		✓																					
7(b)(i)	<p>1 mark per bullet point</p> <ul style="list-style-type: none"> ∞ SISD // Single instruction single data ∞ SIMD // Single instruction multiple data ∞ MISD // Multiple instruction single data ∞ MIMD // Multiple instruction multiple data 	4																					
7(b)(ii)	<p>1 mark per bullet point (max 3)</p> <ul style="list-style-type: none"> ∞ Large number of processors ∞ ... working collaboratively on the same program ∞ ... working together simultaneously on the same program ∞ ... communicating via a messaging interface 	3																					

Answer 5

9(a)	<p>1 mark for each correct term</p> <table border="1"> <thead> <tr> <th>Description</th><th>Term</th></tr> </thead> <tbody> <tr> <td> <ul style="list-style-type: none"> • There are several processors. • Each processor executes different sets of instructions on one set of data at the same time. </td><td>MISD</td></tr> <tr> <td> <ul style="list-style-type: none"> • The processor has several ALUs. • Each ALU executes the same set of instructions on different sets of data at the same time. </td><td>SIMD</td></tr> <tr> <td> <ul style="list-style-type: none"> • There is only one processor. • The processor executes one set of instructions on one set of data. </td><td>SISD</td></tr> <tr> <td> <ul style="list-style-type: none"> • There are several processors. • Each processor executes a different set of instructions. • Each processor operates on different sets of data. </td><td>MIMD</td></tr> </tbody> </table>	Description	Term	<ul style="list-style-type: none"> • There are several processors. • Each processor executes different sets of instructions on one set of data at the same time. 	MISD	<ul style="list-style-type: none"> • The processor has several ALUs. • Each ALU executes the same set of instructions on different sets of data at the same time. 	SIMD	<ul style="list-style-type: none"> • There is only one processor. • The processor executes one set of instructions on one set of data. 	SISD	<ul style="list-style-type: none"> • There are several processors. • Each processor executes a different set of instructions. • Each processor operates on different sets of data. 	MIMD	4
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9(b)	<p>1 mark per bullet point to max 3</p> <ul style="list-style-type: none"> • A large number of processors • Collaborative processing // coordinated simultaneous processing • Network infrastructure • Communicate using a message interface / by sending messages 	3
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Answer 6

5(a)	<p>1 mark per bullet point to max 4:</p> <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;"> <ul style="list-style-type: none"> • RISC has fewer instructions • RISC has many registers • RISC's instructions are simpler • RISC has a few instruction formats • RISC usually uses single-cycle instructions • RISC uses fixed-length instructions • RISC has better pipelineability • RISC requires less complex circuits • RISC has fewer addressing modes • RISC makes more use of RAM • RISC has a hard-wired control unit • RISC only uses load and store instructions to address memory </td><td style="width: 50%;"> <ul style="list-style-type: none"> // CISC has more instructions // CISC has few registers // CISC's instructions are more complex // CISC has many instruction formats // CISC uses multi-cycle instructions // CISC uses variable-length instructions // CISC has poorer pipelineability // CISC requires more complex circuits // CISC has more addressing modes // CISC makes more use of cache/less use of RAM // CISC has a programmable control unit </td></tr> </table>	<ul style="list-style-type: none"> • RISC has fewer instructions • RISC has many registers • RISC's instructions are simpler • RISC has a few instruction formats • RISC usually uses single-cycle instructions • RISC uses fixed-length instructions • RISC has better pipelineability • RISC requires less complex circuits • RISC has fewer addressing modes • RISC makes more use of RAM • RISC has a hard-wired control unit • RISC only uses load and store instructions to address memory 	<ul style="list-style-type: none"> // CISC has more instructions // CISC has few registers // CISC's instructions are more complex // CISC has many instruction formats // CISC uses multi-cycle instructions // CISC uses variable-length instructions // CISC has poorer pipelineability // CISC requires more complex circuits // CISC has more addressing modes // CISC makes more use of cache/less use of RAM // CISC has a programmable control unit
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5(b)(i)	<p>1 mark per bullet point:</p> <ul style="list-style-type: none"> • Completing the As correctly • B in column 2, row 1 no other Bs in row 1 • Remainder correctly completed 	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th rowspan="2" style="text-align: center; padding: 2px;">Stage</th><th colspan="9" style="text-align: center; padding: 2px;">Time interval</th></tr> <tr> <th style="text-align: center; padding: 2px;">1</th><th style="text-align: center; padding: 2px;">2</th><th style="text-align: center; padding: 2px;">3</th><th style="text-align: center; padding: 2px;">4</th><th style="text-align: center; padding: 2px;">5</th><th style="text-align: center; padding: 2px;">6</th><th style="text-align: center; padding: 2px;">7</th><th style="text-align: center; padding: 2px;">8</th><th style="text-align: center; padding: 2px;">9</th></tr> </thead> <tbody> <tr> <td style="text-align: left; padding: 2px;">Fetch instruction</td><td style="text-align: center; padding: 2px;">A</td><td style="text-align: center; padding: 2px;">B</td><td style="text-align: center; padding: 2px;">C</td><td style="text-align: center; padding: 2px;">D</td><td style="text-align: center; padding: 2px;"></td><td style="text-align: center; padding: 2px;"></td><td style="text-align: center; padding: 2px;"></td><td style="text-align: center; padding: 2px;"></td><td style="text-align: center; padding: 2px;"></td></tr> <tr> <td style="text-align: left; padding: 2px;">Decode instruction</td><td style="text-align: center; padding: 2px;"></td><td style="text-align: center; padding: 2px;">A</td><td style="text-align: center; padding: 2px;">B</td><td style="text-align: center; padding: 2px;">C</td><td style="text-align: center; padding: 2px;">D</td><td style="text-align: center; padding: 2px;"></td><td style="text-align: center; padding: 2px;"></td><td style="text-align: center; padding: 2px;"></td><td style="text-align: center; padding: 2px;"></td></tr> <tr> <td style="text-align: left; padding: 2px;">Execute instruction</td><td style="text-align: center; padding: 2px;"></td><td style="text-align: center; padding: 2px;"></td><td style="text-align: center; padding: 2px;">A</td><td style="text-align: center; padding: 2px;">B</td><td style="text-align: center; padding: 2px;">C</td><td style="text-align: center; padding: 2px;">D</td><td style="text-align: center; padding: 2px;"></td><td style="text-align: center; padding: 2px;"></td><td style="text-align: center; padding: 2px;"></td></tr> <tr> <td style="text-align: left; padding: 2px;">Access operand in memory</td><td style="text-align: center; padding: 2px;"></td><td style="text-align: center; padding: 2px;"></td><td style="text-align: center; padding: 2px;"></td><td style="text-align: center; padding: 2px;">A</td><td style="text-align: center; padding: 2px;">B</td><td style="text-align: center; padding: 2px;">C</td><td style="text-align: center; padding: 2px;">D</td><td style="text-align: center; padding: 2px;"></td><td style="text-align: center; padding: 2px;"></td></tr> <tr> <td style="text-align: left; padding: 2px;">Write result to register</td><td style="text-align: center; padding: 2px;"></td><td style="text-align: center; padding: 2px;"></td><td style="text-align: center; padding: 2px;"></td><td style="text-align: center; padding: 2px;"></td><td style="text-align: center; padding: 2px;">A</td><td style="text-align: center; padding: 2px;">B</td><td style="text-align: center; padding: 2px;">C</td><td style="text-align: center; padding: 2px;">D</td><td style="text-align: center; padding: 2px;"></td></tr> </tbody> </table>	Stage	Time interval									1	2	3	4	5	6	7	8	9	Fetch instruction	A	B	C	D						Decode instruction		A	B	C	D					Execute instruction			A	B	C	D				Access operand in memory				A	B	C	D			Write result to register					A	B	C	D	
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5(b)(ii)	<p>1 mark per bullet point:</p> <ul style="list-style-type: none"> • Correct number of cycles for pipelining 8 • Correct number of cycles without pipelining $4 \times 5 = 20$ • No of cycles saved $20 - 8 = 12$
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5(c)	<p>1 mark for each row</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th rowspan="2" style="text-align: left; padding: 5px;">Statement</th><th colspan="3" style="text-align: center; padding: 5px;">Architecture</th></tr> <tr> <th style="text-align: center; padding: 5px;">SIMD</th><th style="text-align: center; padding: 5px;">MIMD</th><th style="text-align: center; padding: 5px;">SISD</th></tr> </thead> <tbody> <tr> <td style="padding: 5px;">Each processor executes a different instruction</td><td style="text-align: center; padding: 5px;">✓</td><td style="text-align: center; padding: 5px;"></td><td style="text-align: center; padding: 5px;"></td></tr> <tr> <td style="padding: 5px;">There is only one processor</td><td style="text-align: center; padding: 5px;"></td><td style="text-align: center; padding: 5px;"></td><td style="text-align: center; padding: 5px;">✓</td></tr> <tr> <td style="padding: 5px;">Each processor executes the same instruction input using data available in the dedicated memory</td><td style="text-align: center; padding: 5px;">✓</td><td style="text-align: center; padding: 5px;"></td><td style="text-align: center; padding: 5px;"></td></tr> <tr> <td style="padding: 5px;">Each processor typically has its own partition within a shared memory</td><td style="text-align: center; padding: 5px;"></td><td style="text-align: center; padding: 5px;">✓</td><td style="text-align: center; padding: 5px;"></td></tr> </tbody> </table>	Statement	Architecture			SIMD	MIMD	SISD	Each processor executes a different instruction	✓			There is only one processor			✓	Each processor executes the same instruction input using data available in the dedicated memory	✓			Each processor typically has its own partition within a shared memory		✓	
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Answer 7

2(a)	<table border="0" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%; text-align: center; padding: 5px;">Description</th><th style="width: 50%; text-align: center; padding: 5px;">Computer architecture</th><th style="width: 10%; text-align: right; padding: 5px;">4</th></tr> </thead> <tbody> <tr> <td style="padding: 5px;">Most parallel computer systems use this architecture.</td><td style="text-align: center; padding: 5px;">SIMD</td><td></td></tr> <tr> <td style="padding: 5px;">Widely used to process 3D graphics in video games.</td><td style="text-align: center; padding: 5px;">MIMD</td><td></td></tr> <tr> <td style="padding: 5px;">A microprocessor is used to control a washing machine.</td><td style="text-align: center; padding: 5px;">MISD</td><td></td></tr> <tr> <td style="padding: 5px;">There are a number of processing units. Each processing unit executes the same instruction but on different data</td><td style="text-align: center; padding: 5px;">SISD</td><td></td></tr> </tbody> </table> <p style="text-align: right; margin-top: -10px;">1 mark for each correct line</p>	Description	Computer architecture	4	Most parallel computer systems use this architecture.	SIMD		Widely used to process 3D graphics in video games.	MIMD		A microprocessor is used to control a washing machine.	MISD		There are a number of processing units. Each processing unit executes the same instruction but on different data	SISD		
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2(b)	<ul style="list-style-type: none"> ∞ Only one (separate) processor / not many separate processors (is not massively parallel) 1 ∞ Quad core computer system // processing units share the same bus 1 <p style="text-align: right; margin-top: -10px;">1 mark for each point, max 2</p>	2															
2(c)	<ul style="list-style-type: none"> ∞ Split into blocks of code ∞ ... that can be processed simultaneously ... ∞ ... instead of sequentially ∞ Each block is processed by a different processor ∞ which allows each of the many processors to simultaneously process the different blocks of code independently ∞ Requires both parallelism and co-ordination <p style="text-align: right; margin-top: -10px;">1 mark for each point, max 2</p>	2															

2(d)	<p>1 mark for identification of hardware issue, for example:</p> <ul style="list-style-type: none"> ∞ Communication between the different processors is the issue <p>1 mark for further explanation from:</p> <ul style="list-style-type: none"> ∞ Each processor needs a link to every other processor ∞ Many processors require many of these links ∞ Challenging topology 	2
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Answer 8

2(a)	<table style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; width: 50%;">Description</th><th style="text-align: center; width: 50%;">Type of processor</th></tr> </thead> <tbody> <tr> <td style="border: 1px solid black; padding: 5px;">It has a simplified set of instructions.</td><td style="border: 1px solid black; padding: 5px; text-align: center;">CISC</td></tr> <tr> <td style="border: 1px solid black; padding: 5px;">Emphasis is on the hardware rather than the software.</td><td style="border: 1px solid black; padding: 5px; text-align: center;">RISC</td></tr> <tr> <td style="border: 1px solid black; padding: 5px;">It makes extensive use of general purpose registers.</td><td style="border: 1px solid black; padding: 5px; text-align: center;">RISC</td></tr> <tr> <td style="border: 1px solid black; padding: 5px;">Many instruction formats are available.</td><td style="border: 1px solid black; padding: 5px; text-align: center;">CISC</td></tr> </tbody> </table> <p style="text-align: center;">1 mark for each correct line</p>	Description	Type of processor	It has a simplified set of instructions.	CISC	Emphasis is on the hardware rather than the software.	RISC	It makes extensive use of general purpose registers.	RISC	Many instruction formats are available.	CISC	4
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2(b)(i)	<p>One mark per point – max 2</p> <ul style="list-style-type: none"> ∞ Pipelining is instruction level parallelism ∞ Execution (A: processing) of an instruction is split into a number of stages ∞ When first stage for an instruction is completed the first stage of the next instruction can start executing ∞ Another instruction can start executing before the previous one is finished ∞ Processing of a number of instructions can be concurrent / simultaneous 	2										

2(b)(ii)	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th rowspan="2">Stage</th><th colspan="8">Time Interval</th></tr> <tr> <th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th><th>8</th></tr> </thead> <tbody> <tr> <td>Fetch instruction</td><td>D</td><td>E</td><td></td><td></td><td></td><td></td><td></td><td></td></tr> <tr> <td>Read registers and decode instruction</td><td></td><td>D</td><td>E</td><td></td><td></td><td></td><td></td><td></td></tr> <tr> <td>Execute instruction</td><td></td><td></td><td>D</td><td>E</td><td></td><td></td><td></td><td></td></tr> <tr> <td>Access operand in memory</td><td></td><td></td><td></td><td>D</td><td>E</td><td></td><td></td><td></td></tr> <tr> <td>Write result to register</td><td></td><td></td><td></td><td></td><td>D</td><td>E</td><td></td><td></td></tr> </tbody> </table>	Stage	Time Interval								1	2	3	4	5	6	7	8	Fetch instruction	D	E							Read registers and decode instruction		D	E						Execute instruction			D	E					Access operand in memory				D	E				Write result to register					D	E			3
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D and E in second row (in that order) (1)																																																																
Remainder completed correctly (1)																																																																
2(c)(i)	Two from: <ul style="list-style-type: none"> ∞ The result of the first addition is not stored in (register) r3 (1) ∞ Before the next instruction needs to load value from r3 (1) ∞ There is a data dependency issue (1) ∞ r3 is being fetched and stored on the same clock pulse (1) 	2																																																														
2(c)(ii)	The third instruction is not dependent on the first two, therefore, instruction 2 and 3 need to be swapped	1																																																														

Abswer 9

3(a)(i)	A: Guest (operating system) (1) B: Host (operating system) (1)	2
3(a)(ii)	One mark for each valid point, max 3 <ul style="list-style-type: none"> ∞ Guest OS (A) handles request as if it were running on its own physical machine // guest OS (A) is not aware it is running on a virtual platform ∞ Guest OS (A) handles the request as usual ∞ I/O requests are translated by the virtual machine software ∞ Into instructions executed by host OS (B) ∞ Host OS (B) retrieves the data from the file ∞ Host OS (B) passes the data to the virtual machine software ∞ The virtual machine software passes the data to the guest OS (A) ∞ Guest OS passes the data to the application 	3
3(b)(i)	One mark from: <ul style="list-style-type: none"> ∞ Because software can be tried on different OS using same hardware ∞ Because no need to purchase / request all sorts of different hardware ∞ Easier to recover if software causes system crash ∞ VM provides protection to other software / host OS from malfunctioning software 	1

3(b)(ii)	<p>Max 2 marks per limitation, max 2 limitations – max 4 marks</p> <p>Virtual machine may not be able to emulate some hardware ... So that hardware cannot be tested using a virtual machine ... By relevant example, e.g. developing hardware drivers</p> <p>Using virtual machine means execution of extra code // processing time increased ... so cannot accurately test speed of real performance</p> <p>A virtual machine might not be as efficient ... By relevant example, e.g. might not be able to access sufficient memory</p>	4
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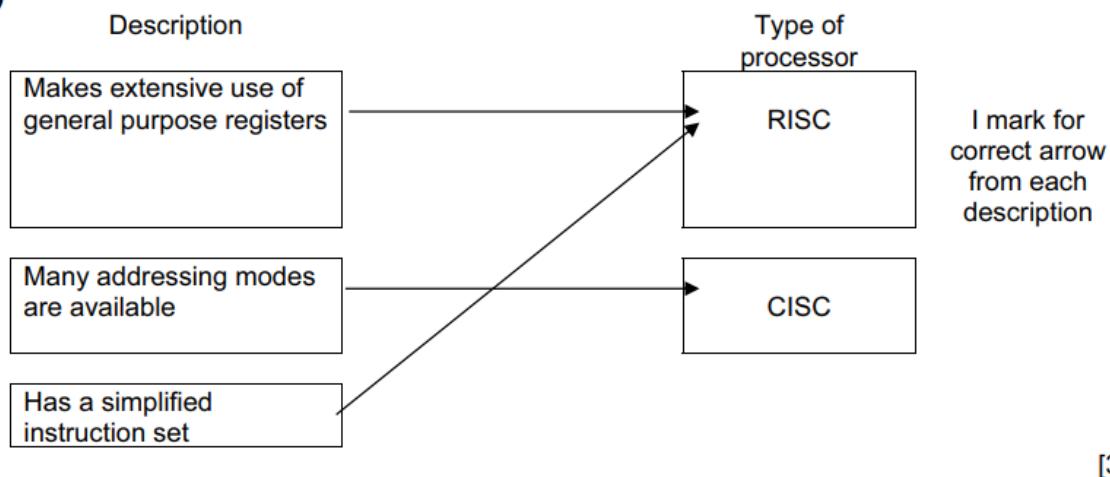
Answer 10

3 (a) (i)	<p>Examples: Create / delete virtual machine Existing hardware made available to guest OS // hardware emulation Ensures each virtual machine is protected from actions of another virtual machine</p>	1 1 1 Max 2
(ii)	<p>Guest operating system: An operating system running in a virtual machine // Controls virtual hardware // OS is being emulated</p> <p>Host operating system: The operating system that is actually controlling the physical hardware // the operating system for the physical machine// the OS running the VM software</p> <p>Guest OS is running under the Host OS software</p>	1 1 1 Max 2
(b) (i)	<p>Examples: Trial/use alternative replacement operating system(s) ... Test to identify possible problems Much easier to create VM with a new OS than create new computer system</p> <p>Trial/use alternative replacement web server software ... Test to identify possible problems Easier to try alternative new software <u>and</u> new OS combinations</p> <p>To provide some additional service(s) Trial/test its use - description e.g. a print server</p> <p>General description point – to provide a safe environment during testing (which does not disrupt the web server service)</p>	Two marks for each use Maximum two uses Max 4

(ii)	<p>Examples: Using virtual machine means execution of extra code // emulation of some hardware ...</p> <p>Non-VM installation may not perform in the same way Execution speed slower than non-VM system Problems in judging actual response times at time of maximum traffic needs fastest possible speed</p> <p>Particular hardware may be difficult to emulate</p>	<p>1</p> <p>1</p> <p>1</p> <p>1</p> <p>1</p> <p>Max 2</p>
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Answer 11

4 (a)



(b) (i)

stage	Time Interval								
	1	2	3	4	5	6	7	8	9
Fetch instruction	A	B	C						
Decode instruction		A	B	C					
Execute instruction			A	B	C				
Access operand in memory				A	B	C			
Write result to register					A	B	C		

[3]

(ii) With pipelining no of cycles = 7

[1]

Without pipelining no of cycles = $3 * 5 = 15$

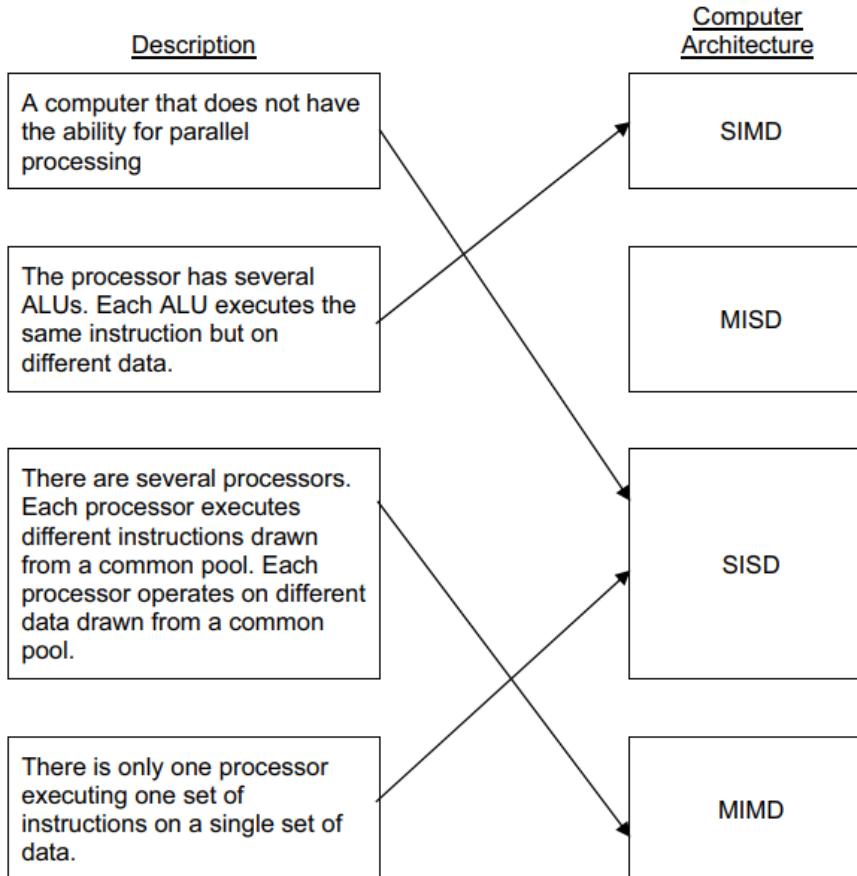
[1]

No of cycles saved = 8

[1]

Answer 12

4 (a) 1 mark for correct arrow from each description



[4]

- (b) (i) **Massive**: many/large number of processors // hundreds/thousands of processors [1]
- (ii) **Parallel**: to perform a set of coordinated computations in parallel/simultaneously [1]
- (c) processors need to be able to communicate ...
so that processed data can be transferred from one processor to another [1]
[1]
- suitable algorithm/program/software/design // appropriate programming language
which allows data to be processed by multiple processors simultaneously [1]
[1]