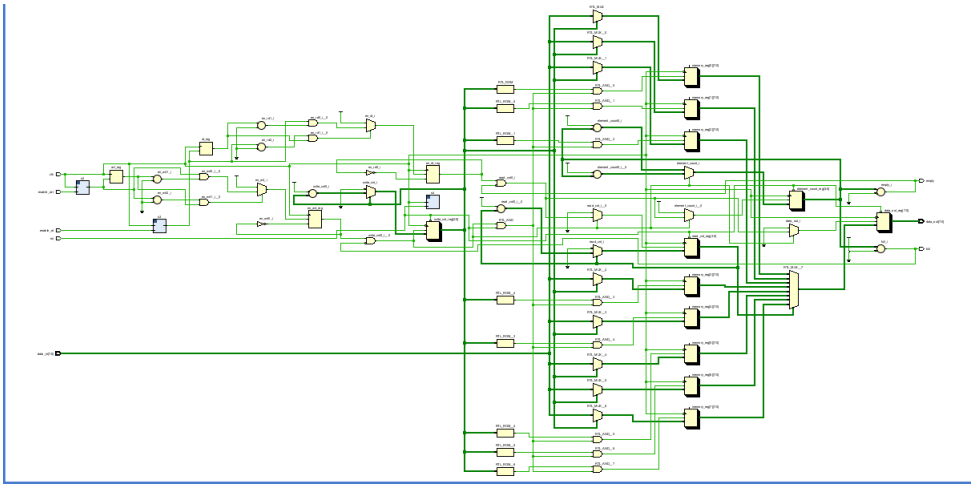
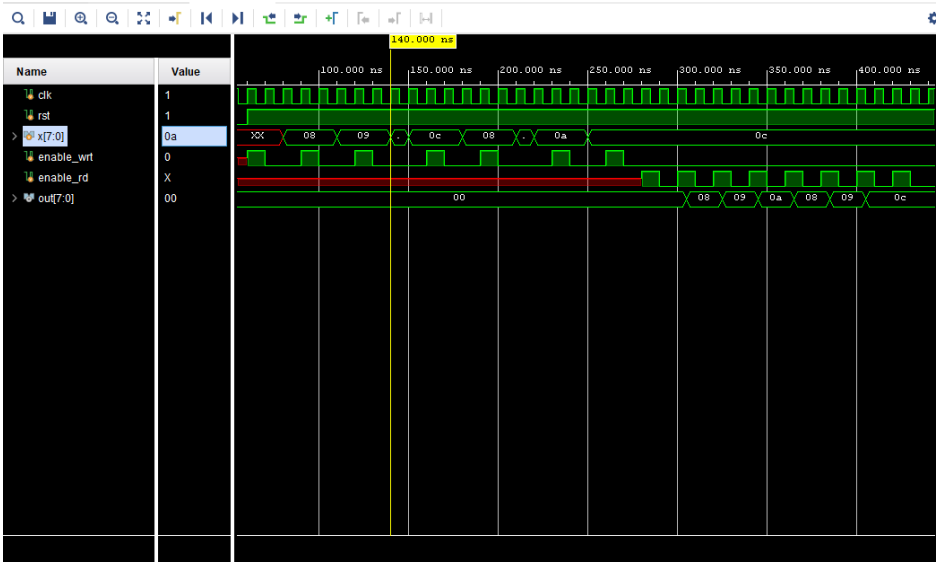
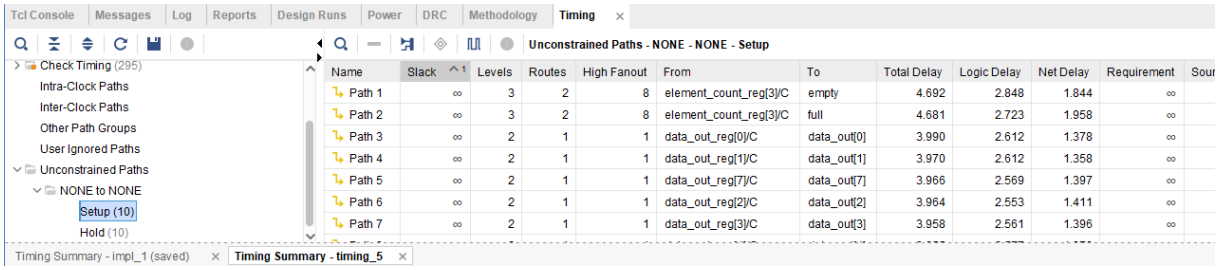
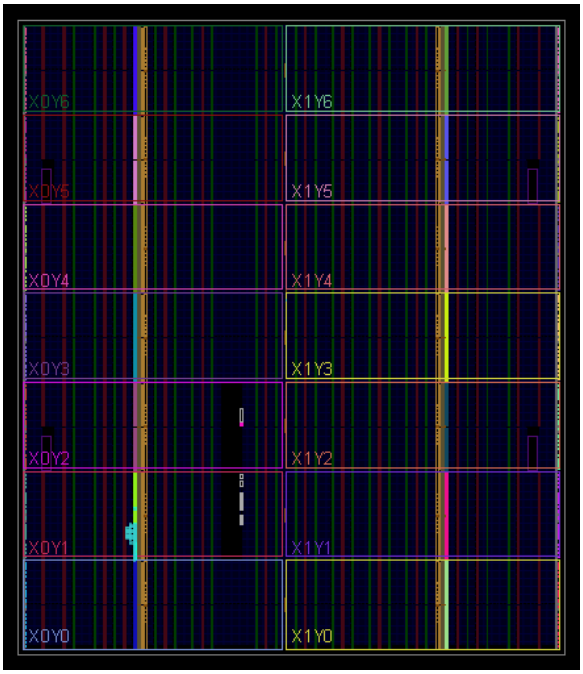
ASSİGNMENT 5

1) Bu görevde uzunluğu parametrik olan bir FİFO tasarladım.



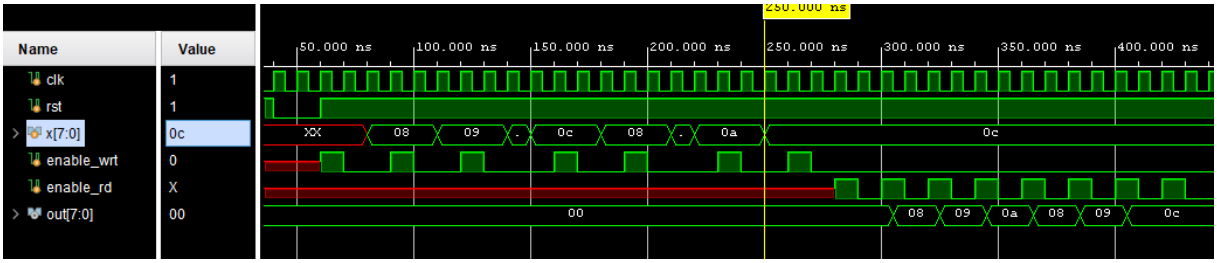


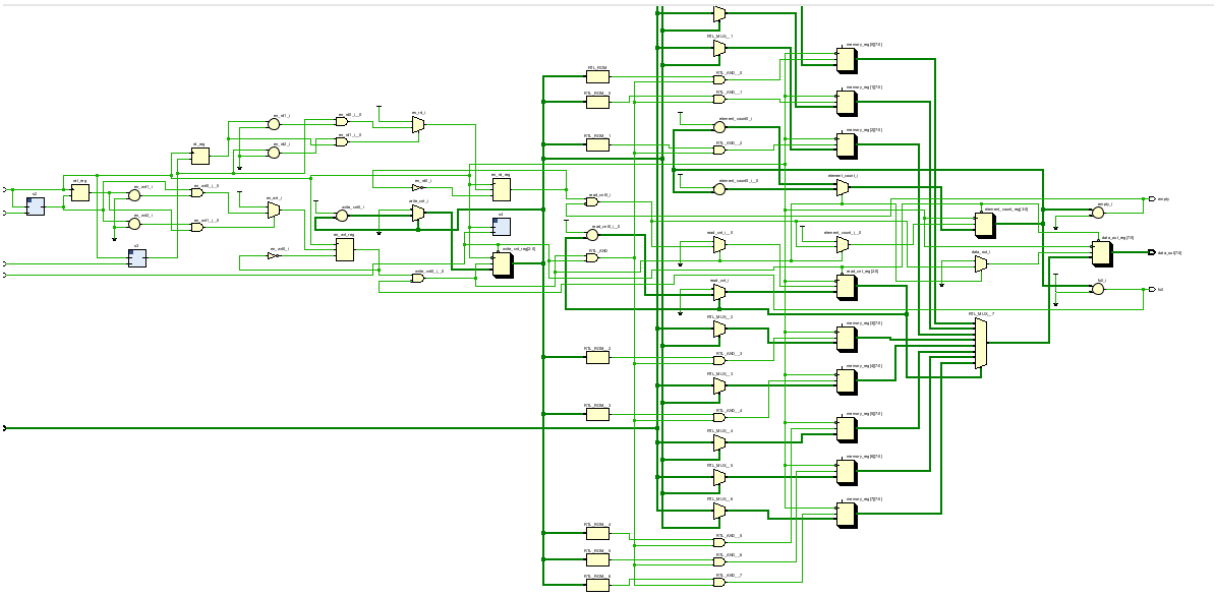


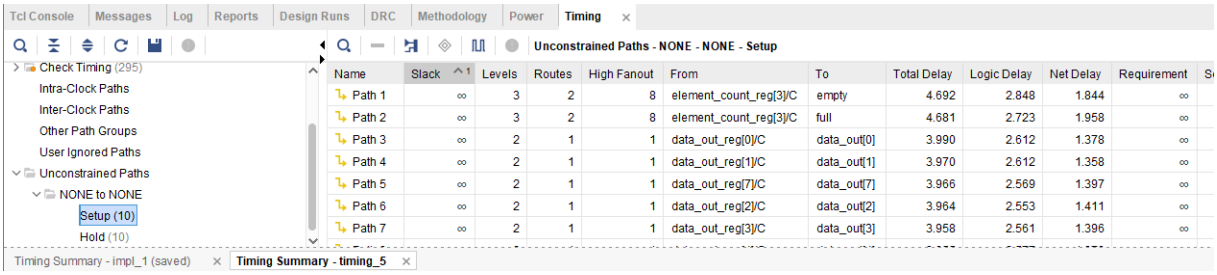



```
module fifo_tek_tb();

 reg clk=0,rst=0;
 reg   [7:0]x;
 reg   enable_wrt;
 reg   enable_rd;
 wire  [7:0]out;

fifo_tek dut (.data_in(x), .data_out(out),.clk(clk),.enable_wrt(enable_wrt),.rst(rst),. enable_rd(enable_rd));


always begin
clk=~clk;
#5;
end

initial begin
rst=0;
#20;
rst=1;
#20;
rst=0;
#20;
rst=1;


enable_wrt=1;
#10;
enable_wrt=0;
#10;
x=8'b1000;
#10;
enable_wrt=1;
#10;
enable_wrt=0;
#10;
x=8'b1010;
#10;
x=8'b1100;
#10;
enable_wrt=1;
#10;
enable_wrt=0;
#10;
x=8'b1000;
#10;
enable_wrt=1;
#10;
enable_wrt=0;
#10;
x=8'b1001;
#10;
x=8'b1010;
#10;
enable_wrt=1;
#10;
enable_wrt=0;
#10;
x=8'b1100;
#10;
enable_wrt=1;
#10;
enable_wrt=0;
#10;
```

2) Hem derinliği hem uzunluğunu parametrik olarak ayarlayabileceğimiz bir FİFO tasarladım.







Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 1	∞	3	2	8	element_count_reg[3]/C	empty	4.692	2.848	1.844	∞
Path 2	∞	3	2	8	element_count_reg[3]/C	full	4.681	2.723	1.958	∞
Path 3	∞	2	1	1	data_out_reg[0]/C	data_out[0]	3.990	2.612	1.378	∞
Path 4	∞	2	1	1	data_out_reg[1]/C	data_out[1]	3.970	2.612	1.358	∞
Path 5	∞	2	1	1	data_out_reg[7]/C	data_out[7]	3.966	2.569	1.397	∞
Path 6	∞	2	1	1	data_out_reg[2]/C	data_out[2]	3.964	2.553	1.411	∞
Path 7	∞	2	1	1	data_out_reg[3]/C	data_out[3]	3.958	2.561	1.396	∞

clk	Input	PIN_AF14	3B	B3B_N0	PIN_AF14	2.5 V		12mA
data_in[7]	Input	PIN_AC9	3A	B3A_N0	PIN_AC9	2.5 V		12mA
data_in[6]	Input	PIN_AE11	3A	B3A_N0	PIN_AE11	2.5 V		12mA
data_in[5]	Input	PIN_AD12	3A	B3A_N0	PIN_AD12	2.5 V		12mA
data_in[4]	Input	PIN_AD11	3A	B3A_N0	PIN_AD11	2.5 V		12mA
data_in[3]	Input	PIN_AF10	3A	B3A_N0	PIN_AF10	2.5 V		12mA
data_in[2]	Input	PIN_AF9	3A	B3A_N0	PIN_AF9	2.5 V		12mA
data_in[1]	Input	PIN_AC12	3A	B3A_N0	PIN_AC12	2.5 V		12mA
data_in[0]	Input	PIN_AB12	3A	B3A_N0	PIN_AB12	2.5 V		12mA
data_out[7]	Output	PIN_W20	5A	B5A_N0	PIN_W20	2.5 V		12mA
data_out[6]	Output	PIN_Y19	4A	B4A_N0	PIN_Y19	2.5 V		12mA
data_out[5]	Output	PIN_W19	4A	B4A_N0	PIN_W19	2.5 V		12mA
data_out[4]	Output	PIN_W17	4A	B4A_N0	PIN_W17	2.5 V		12mA
data_out[3]	Output	PIN_V18	4A	B4A_N0	PIN_V18	2.5 V		12mA
data_out[2]	Output	PIN_V17	4A	B4A_N0	PIN_V17	2.5 V		12mA
data_out[1]	Output	PIN_W16	4A	B4A_N0	PIN_W16	2.5 V		12mA
data_out[0]	Output	PIN_V16	4A	B4A_N0	PIN_V16	2.5 V		12mA
empty	Output	PIN_Y21	5A	B5A_N0	PIN_Y21	2.5 V		12mA
enable_rd	Input	PIN_W15	3B	B3B_N0	PIN_W15	2.5 V		12mA
enable_wrt	Input	PIN_AA15	3B	B3B_N0	PIN_AA15	2.5 V		12mA
full	Output	PIN_W21	5A	B5A_N0	PIN_W21	2.5 V		12mA
rst	Input	PIN_AA14	3B	B3B_N0	PIN_AA14	2.5 V		12mA
<<new node>>								