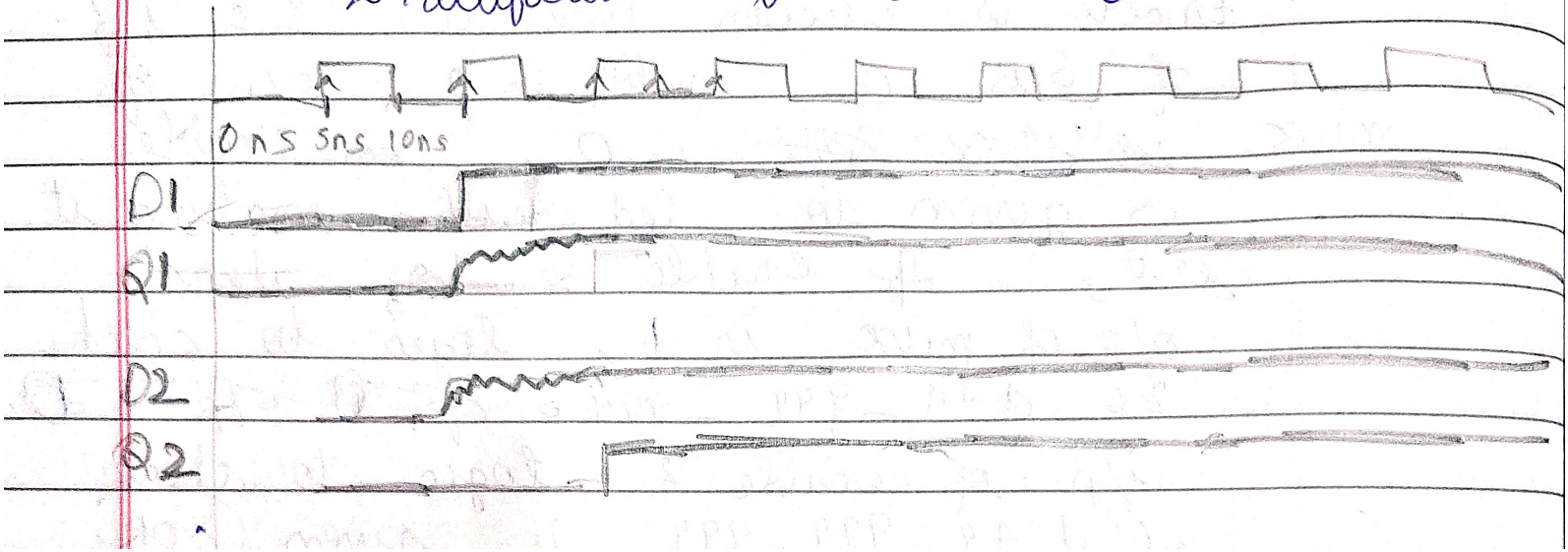
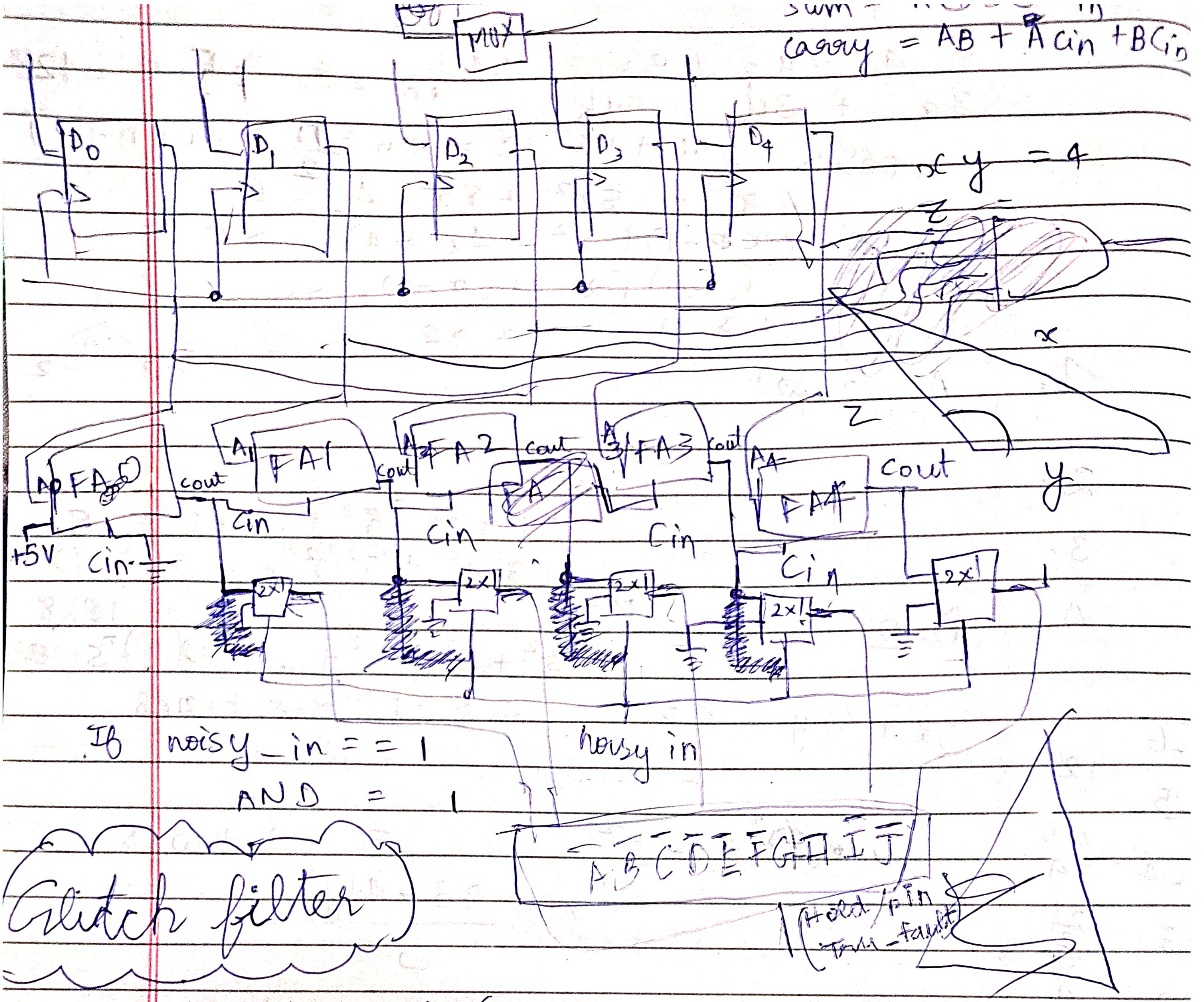
Synchronizer

Waveform showing metastably & rectification at ~~CDC~~ CDC



sum = ...

carry = AB + $\bar{A}$ cin + B Cin



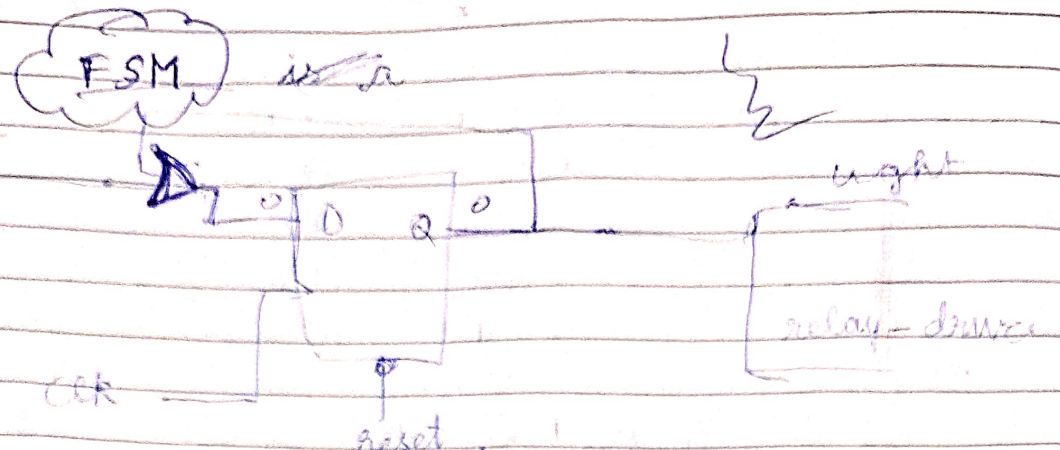
Glitch filter

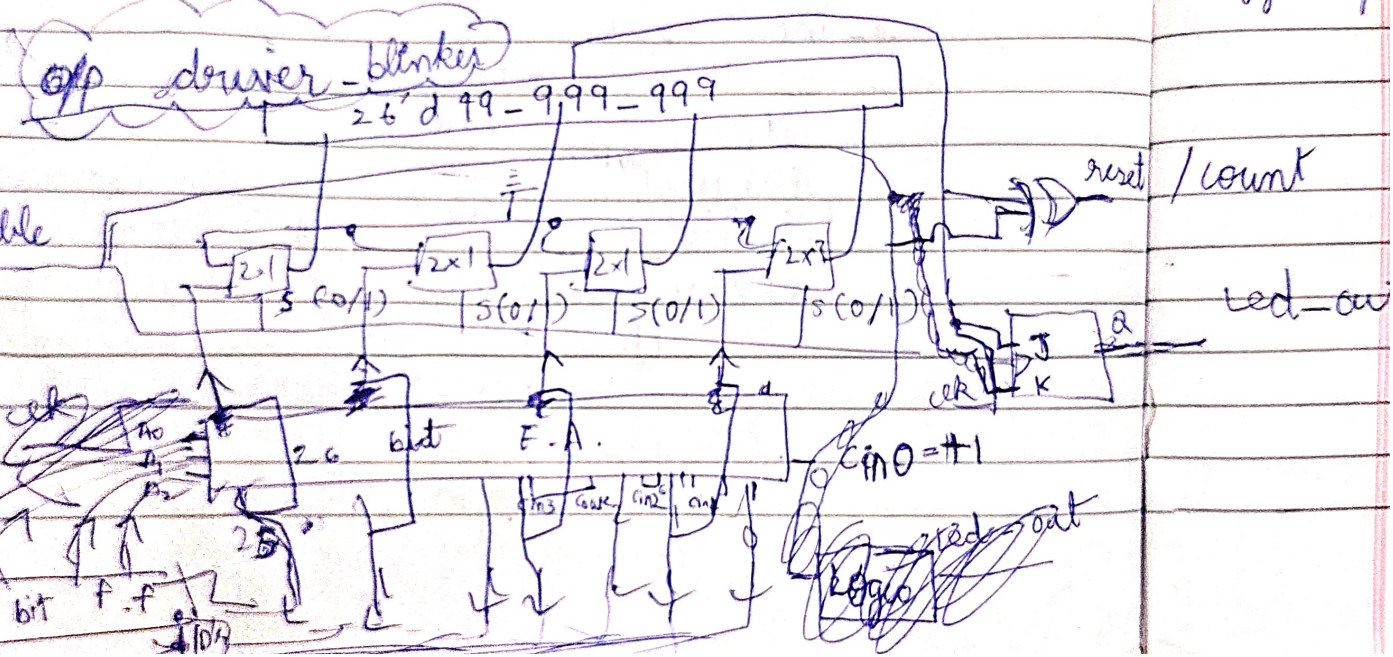
20 bit ff (PIPO) gives o/p to FA
20 bit F.A. where i/p of FA0 is +5V
(i.e. B0) so it adds +1 continuously, this o/p of F.A. is then fed back to register when clk is at pos edge it gets stored and cycle continues provided reset is 0. If
Between adder ~~and~~ o/p and register i/p there is a mux that gets i/p from ~~noisy_in if selection line of mux is~~
1 then i/p goes to register or ~~else o/p is 0~~ resetting FA, if selection line is 1, i.e. noisy_in == 1, then o/p's of muxes given to logic $\bar{A}$ $\bar{B}$ $\bar{C}$ $\bar{D}$ $\bar{E}$ F G $\bar{H}$ $\bar{I}$ $\bar{J}$
if o/p 1, hold is 1, trace_fault is 1 or else vice versa, o/p of mux is also taken & if 0, reset is 0

Note: $\bar{A}\bar{B}CDEFGH\bar{I}\bar{J}$ is 10 bit 1000

monitor ($time,

#0 temperature = ;





O/P - driver & blinker

$Z_L = R_L + jX$.

Enable is selection line for 2:6 d.f.
If S is 0 enable is 0 o/p of mux ~~selection line~~ is 0 ~~or~~ enable is given to led_out making it zero, If enable is 1 there. o/p of mux is 1, logic to check 26'd49_999_999 ~~if 0 o/p is 0~~.
i/p of enable & logic to check 26'd49_999_999 is given (XOR) gate. If o/p is 1 then reset is 0, f-f starts counting other wise if o/p is 0 then reset is 1, count = 0
Also ~~enable &~~ o/p of logic to check 26'd49_999_999 is given to JK f.f. If both i/p's are 1 it toggles LED blinks
J = logic of 26'd 49_999_999
K = ~~Enable~~ logic of 26'd 49_999_999
If 0, no change

Note:
Block with 26'd 49_999_999 is only logic to the count until 49,999,999
In ~~simulation~~ simulation. It has been updated.

~~Toggle f.f~~