Computer System Architecture

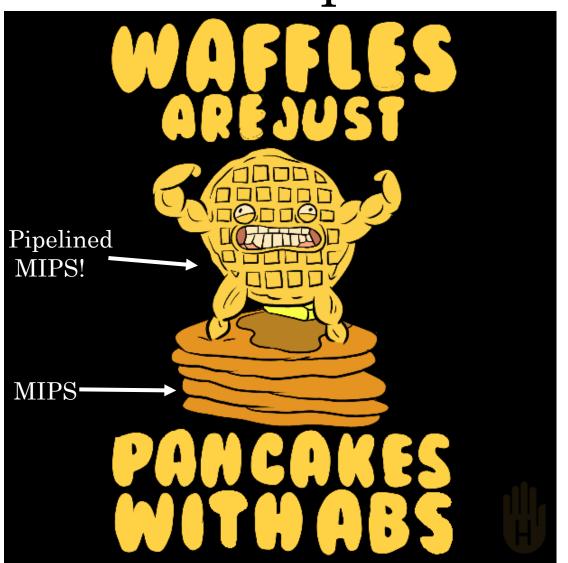
H. SOUBRA

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Lecture 9: Hardware Implementation

Pipelined MIPS!



Pipeline stages from last time?

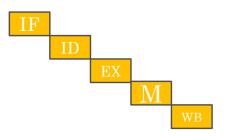
1. IF: Instruction fetch

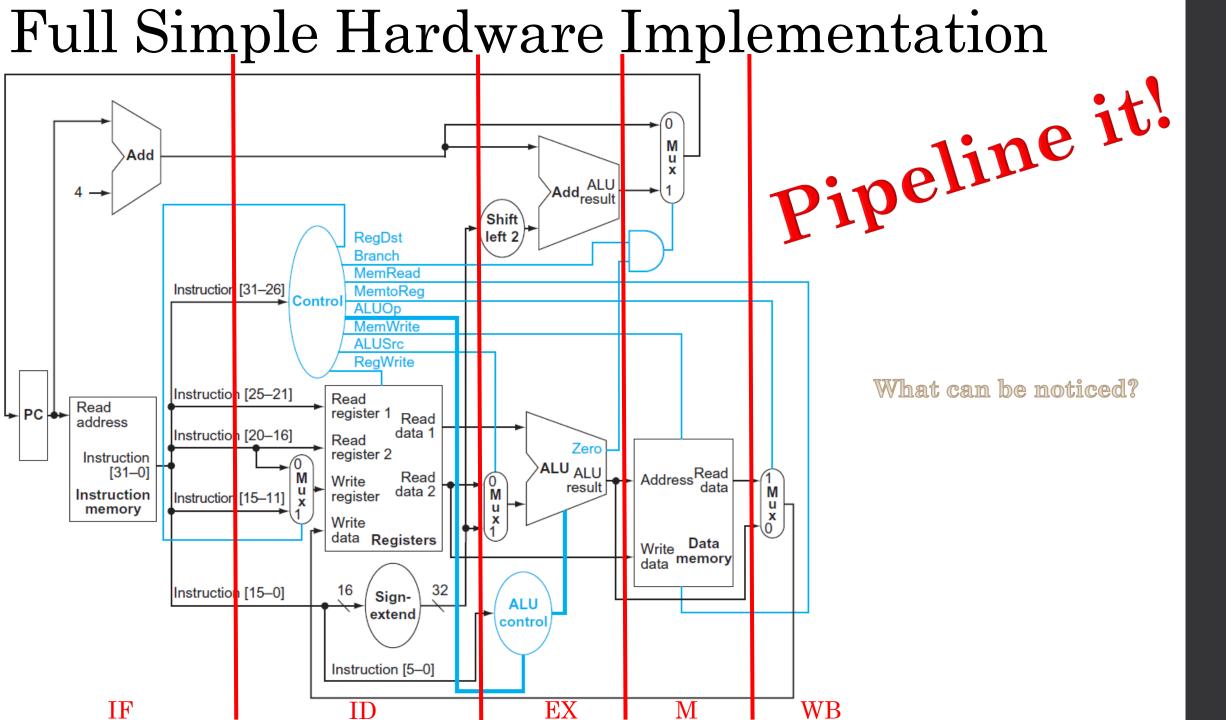
2. ID: Instruction decode and register file read

3. EX: Execution or address calculation

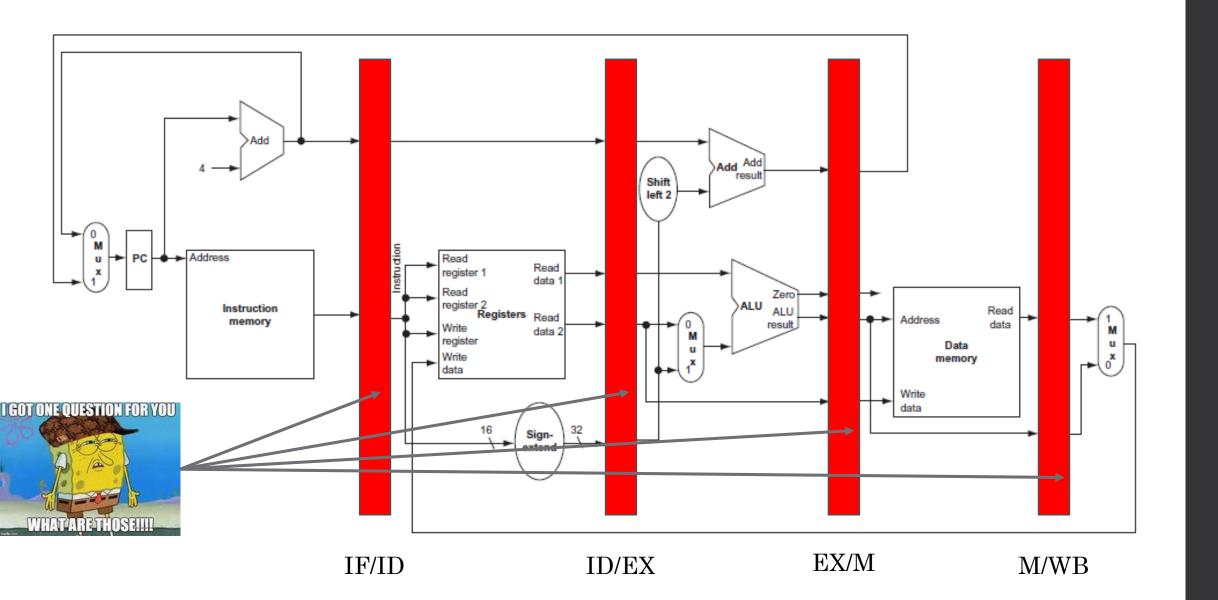
4. M: Data memory access

5. WB: Write back

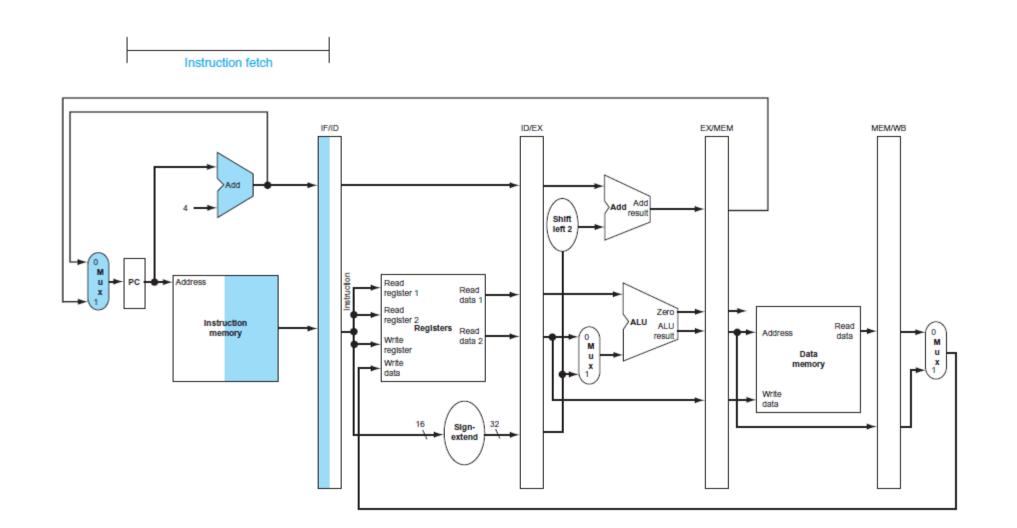




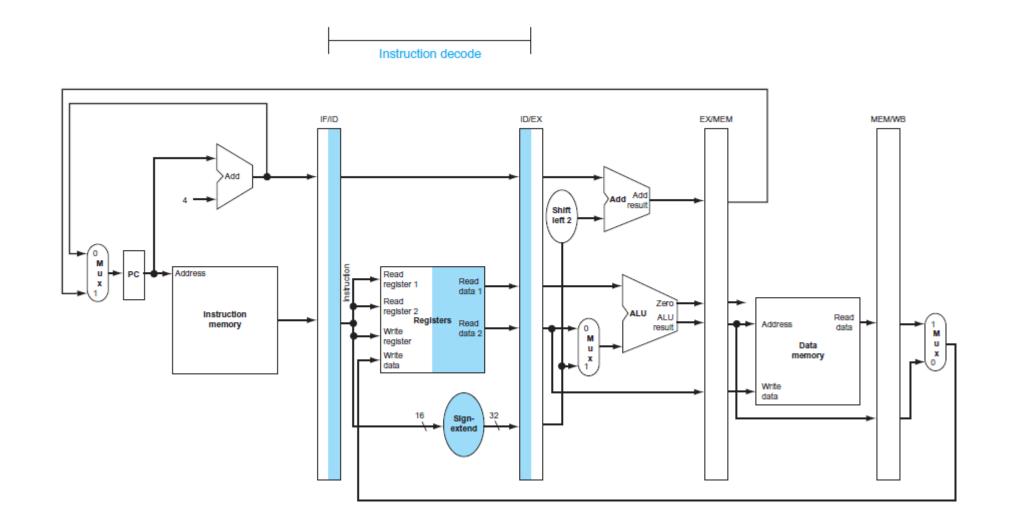
Pipelined version (no control)



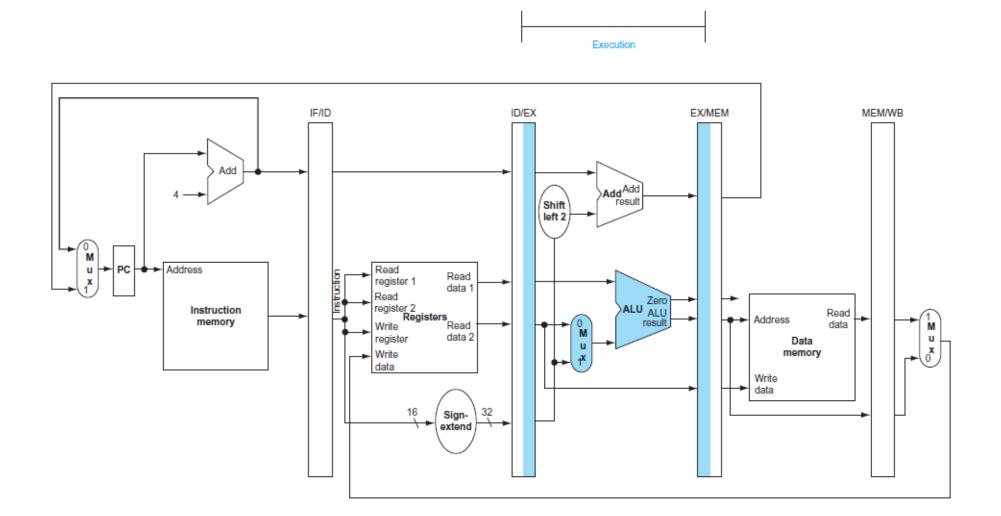
Walk-through of the Pipeline:IF



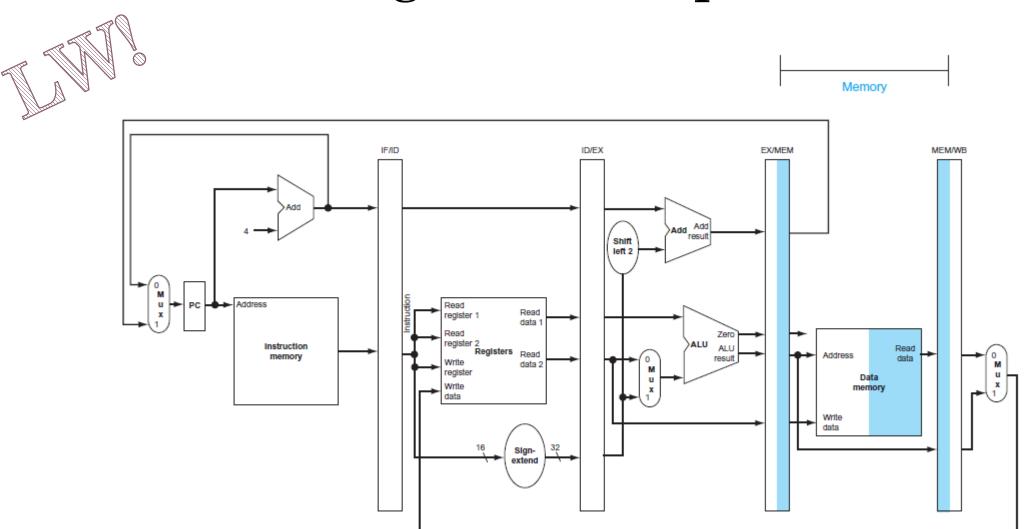
Walk-through of the Pipeline: ID



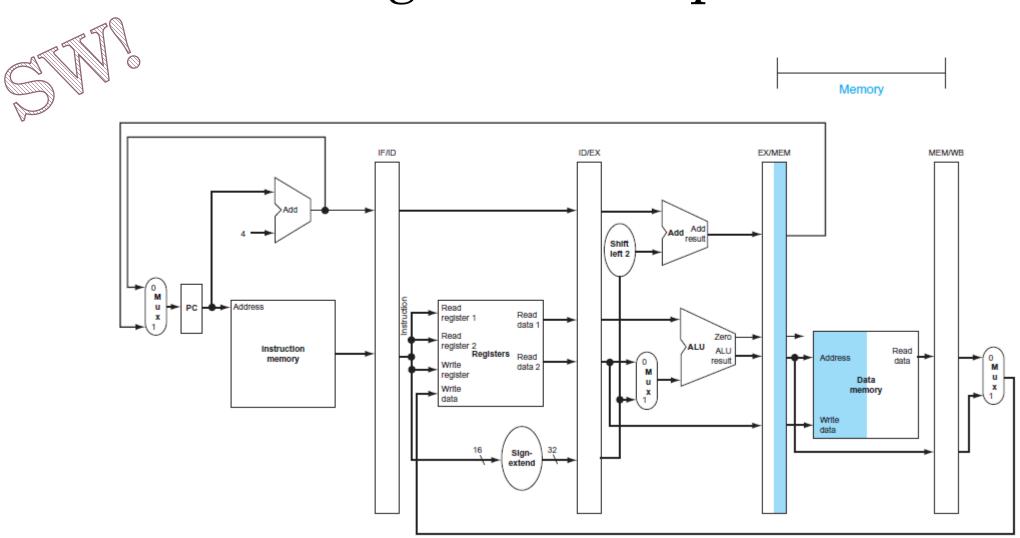
Walk-through of the Pipeline: EX



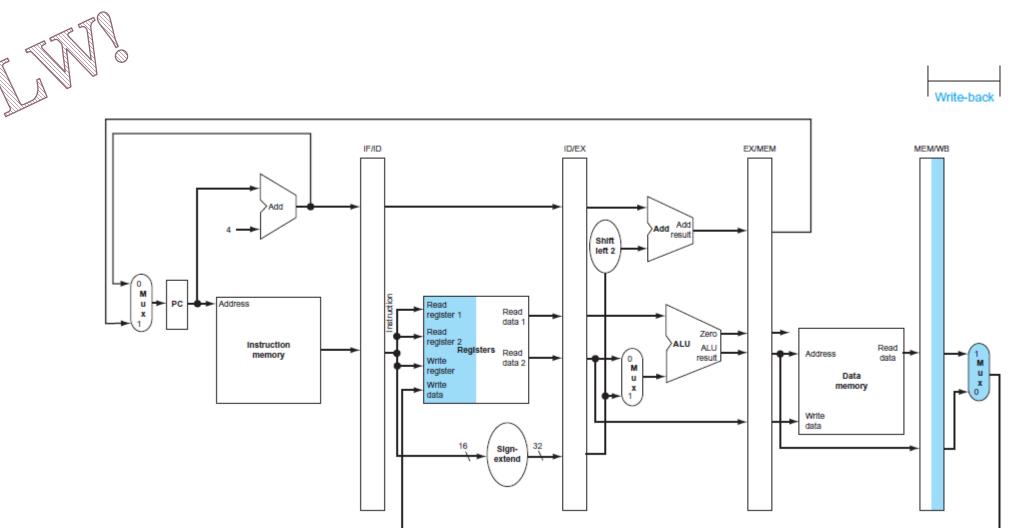
Walk-through of the Pipeline: M1



Walk-through of the Pipeline: M2

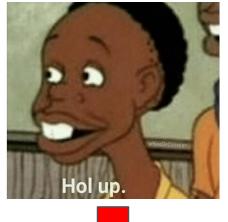


Walk-through of the Pipeline: WB

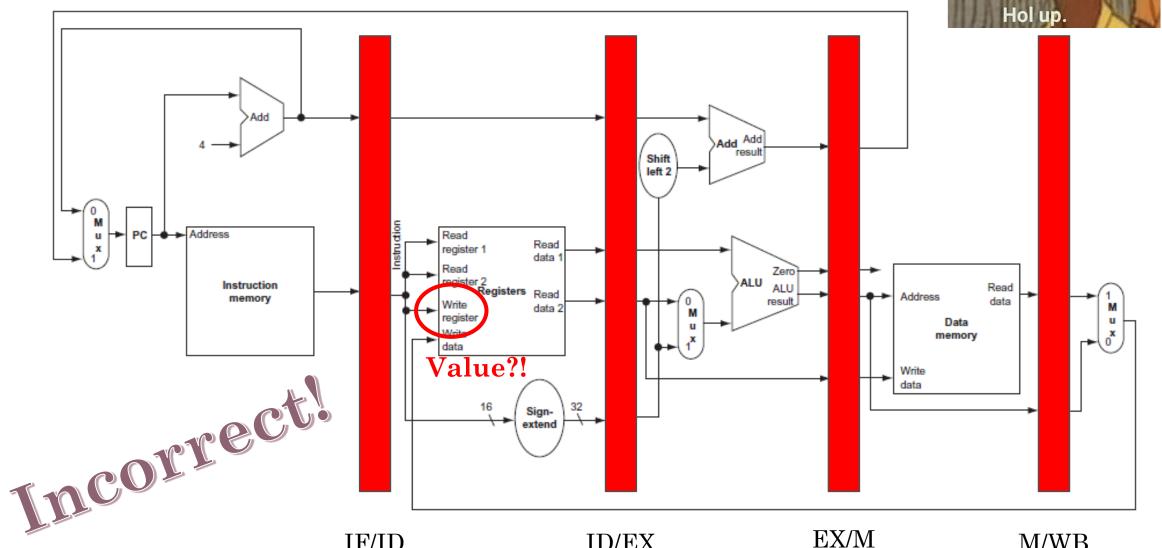


Pipelined version (no control)

IE/ID

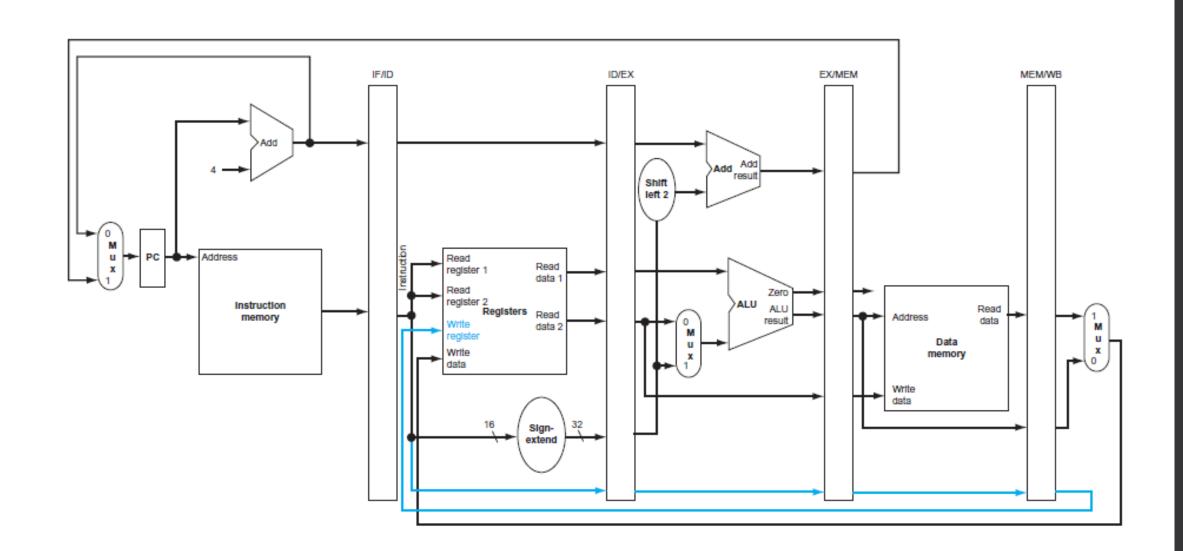


M/WB



ID/EX

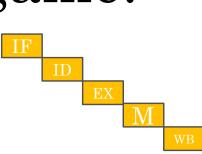
Pipelined version -corrected



- lw \$10, 20(\$1)
- sub \$11, \$2, \$3
- add \$12, \$3, \$4
- lw \$13, 24(\$1)
- add \$14, \$5, \$6

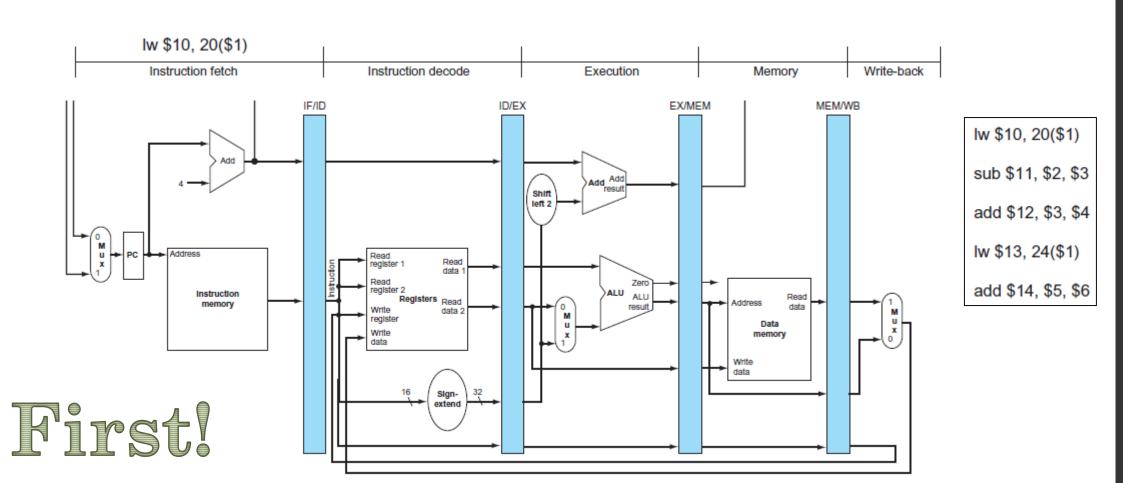
How many cycles to finish up?

Guess, in the next slides, in which cycle we are

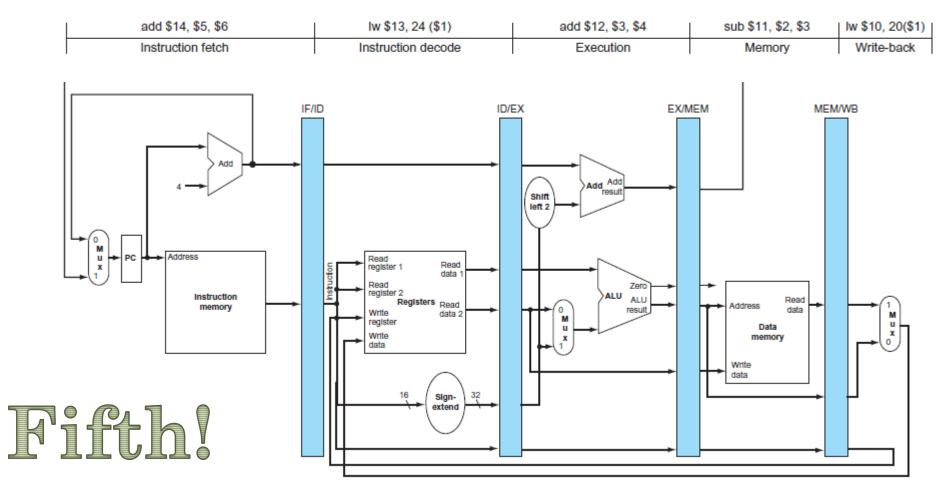








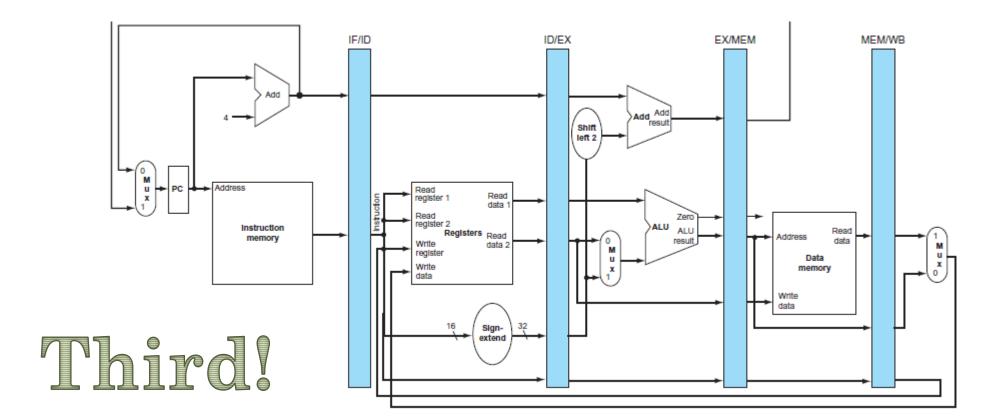




Iw \$10, 20(\$1) sub \$11, \$2, \$3 add \$12, \$3, \$4 Iw \$13, 24(\$1) add \$14, \$5, \$6







lw \$10, 20(\$1) sub \$11, \$2, \$3 add \$12, \$3, \$4 lw \$13, 24(\$1) add \$14, \$5, \$6

Research

• How much technology has influenced time spent in the different components?