PROJECT REPORT

Topic : FPGA-Based Traffic Light Controller with Priority System using Verilog

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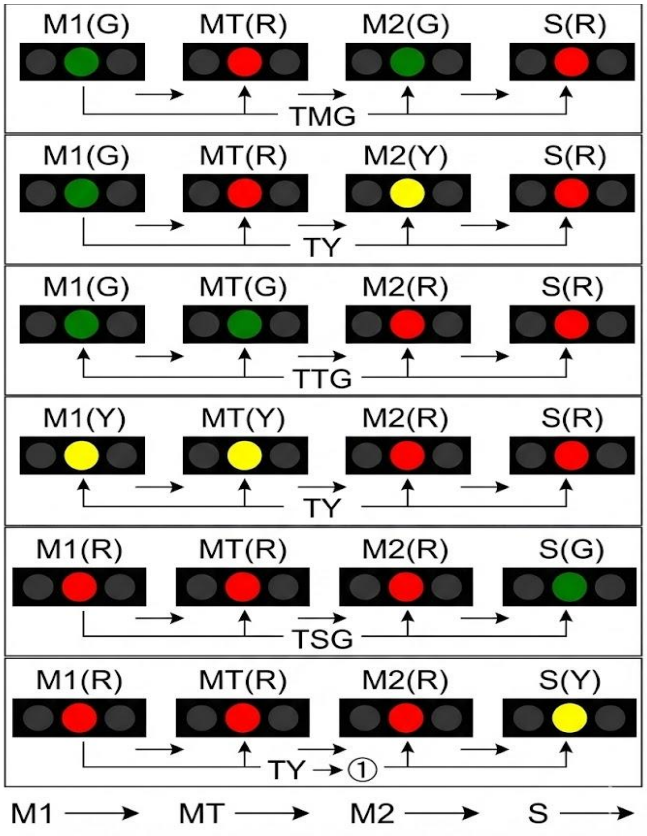
PROBLEM STATEMENT :

The aim of the project is to design a traffic controller for a T-intersection.

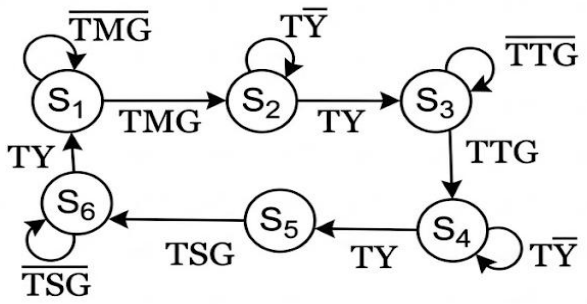
Let's understand the problem statement through the image given below.



The six cases present here eventually turn to the six states.

State Diagram :

TMG	**7s**
TY	**2s**
TTG	**5s**
TSG	**3s**



VERILOG CODE :

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 20.01.2026 10:53:25
// Design Name:
// Module Name: Traffic_Light_Controller
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module Traffic_Light_Controller(
input clk,rst,
output reg [2:0]light_M1,
```

```
output reg [2:0]light_S,
output reg [2:0]light_MT,
output reg [2:0]light_M2
);
parameter S1=0, S2=1, S3 =2, S4=3, S5=4,S6=5;
reg [3:0]count;
reg[2:0] ps;
parameter sec7=7,sec5=5,sec2=2,sec3=3;
always@(posedge clk or posedge rst)
begin
if(rst==1)
begin
ps<=S1;
count<=0;
end
else
case(ps)
S1: if(count<sec7)
begin
ps<=S1;
count<=count+1;
end
else
begin
ps<=S2;
count<=0;
```

```
end
S2: if(count<sec2)
begin
ps<=S2;
count<=count+1;
end
else
begin
ps<=S3;
count<=0;
end
S3: if(count<sec5)
begin
ps<=S3;
count<=count+1;
end
else
begin
ps<=S4;
count<=0;
end
S4:if(count<sec2)
begin
ps<=S4;
count<=count+1;
end
```

```
else
begin
ps<=S5;
count<=0;
end
S5:if(count<sec3)
begin
ps<=S5;
count<=count+1;
end
else
begin
ps<=S6;
count<=0;
end
S6:if(count<sec2)
begin
ps<=S6;
count<=count+1;
end
else
begin
ps<=S1;
count<=0;
end
default: ps<=S1;
```

```
endcase
end
always@(ps)
begin
case(ps)
S1:
begin
light_M1<=3'b001;
light_M2<=3'b001;
light_MT<=3'b100;
light_S<=3'b100;
end
S2:
begin
light_M1<=3'b001;
light_M2<=3'b010;
light_MT<=3'b100;
light_S<=3'b100;
end
S3:
begin
light_M1<=3'b001;
light_M2<=3'b100;
light_MT<=3'b001;
light_S<=3'b100;
end
```

```
S4:
begin
light_M1<=3'b010;
light_M2<=3'b100;
light_MT<=3'b010;
light_S<=3'b100;
end
S5:
begin
light_M1<=3'b100;
light_M2<=3'b100;
light_MT<=3'b100;
light_S<=3'b001;
end
S6:
begin
light_M1<=3'b100;
light_M2<=3'b100;
light_MT<=3'b100;
light_S<=3'b100;
end
default:
begin
light_M1<=3'b000;
light_M2<=3'b000;
light_MT<=3'b000;
```

```
light_S<=3'b010;
end
endcase
end
endmodule
```

****
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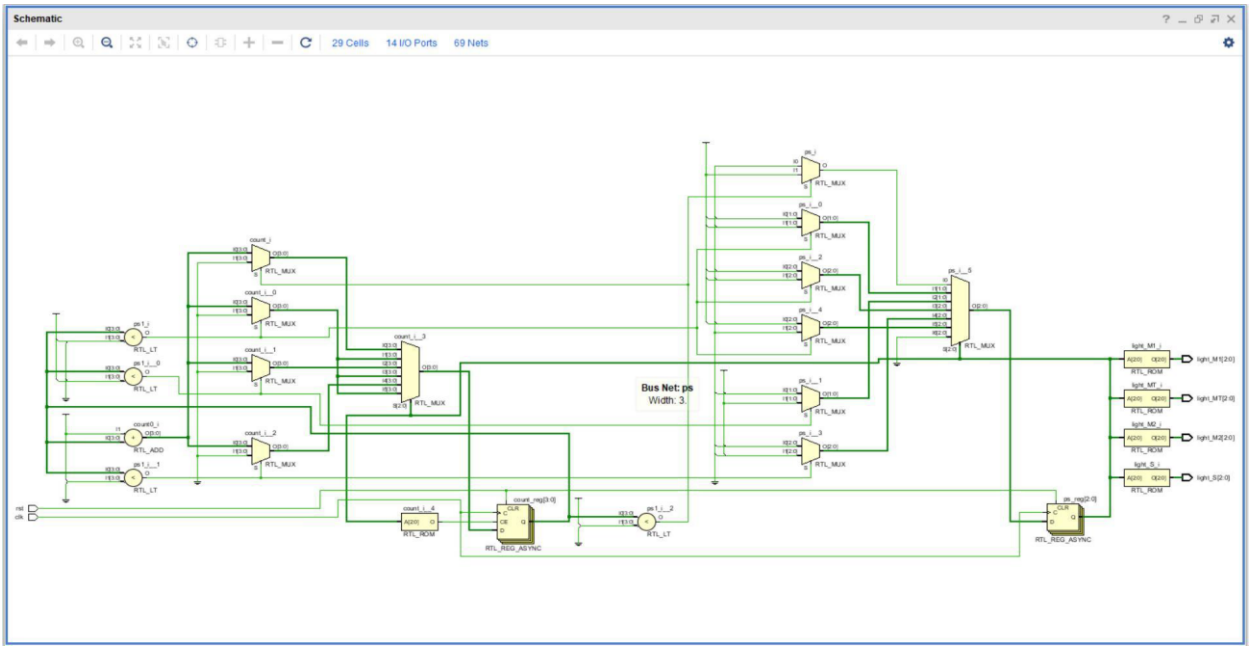
RTL-SCHEMATIC



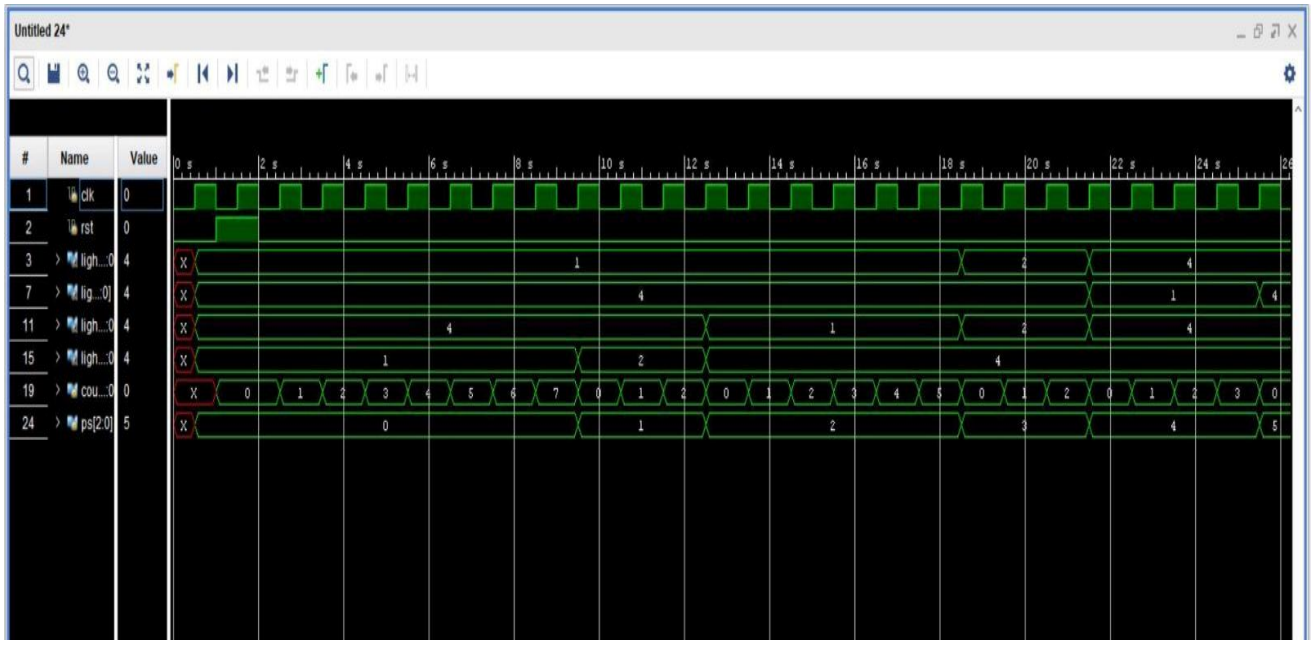
TESTBENCH :

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 20.01.2026 12:55:30
// Design Name:
// Module Name: Traffic_Light_Controller_TB
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module Traffic_Light_Controller_TB;
reg clk,rst;
wire [2:0]light_M1;
wire [2:0]light_S;
wire [2:0]light_MT;
```

```
wire [2:0]light_M2;
Traffic_Light_Controller dut(.clk(clk) , .rst(rst) , .light_M1(light_M1) ,
.light_S(light_S) ,.light_M2(light_M2),.light_MT(light_MT) );
initial
begin
clk=1'b0;
forever #(1000000000/2) clk=~clk;
end
initial
begin
rst=0;
#1000000000;
rst=1;
#1000000000;
rst=0;
#(1000000000*200);
$finish;
end
endmodule
```

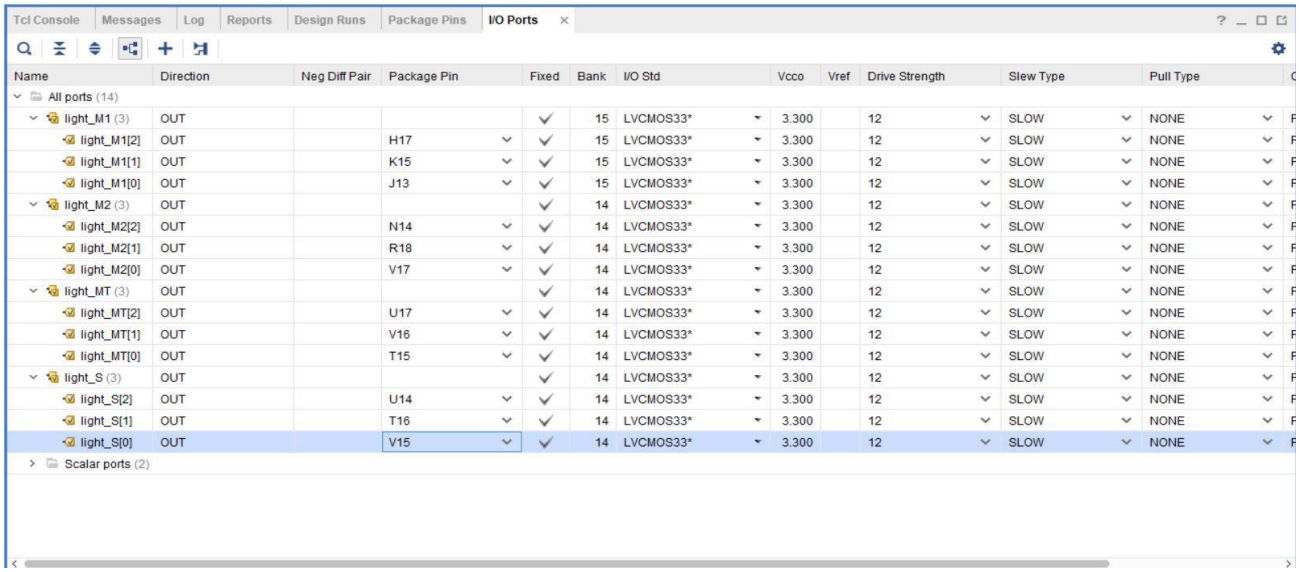
****
****

SIMULATED WAVEFORM :



Upon analysing the waveform we can clearly see that the FSM works perfectly.

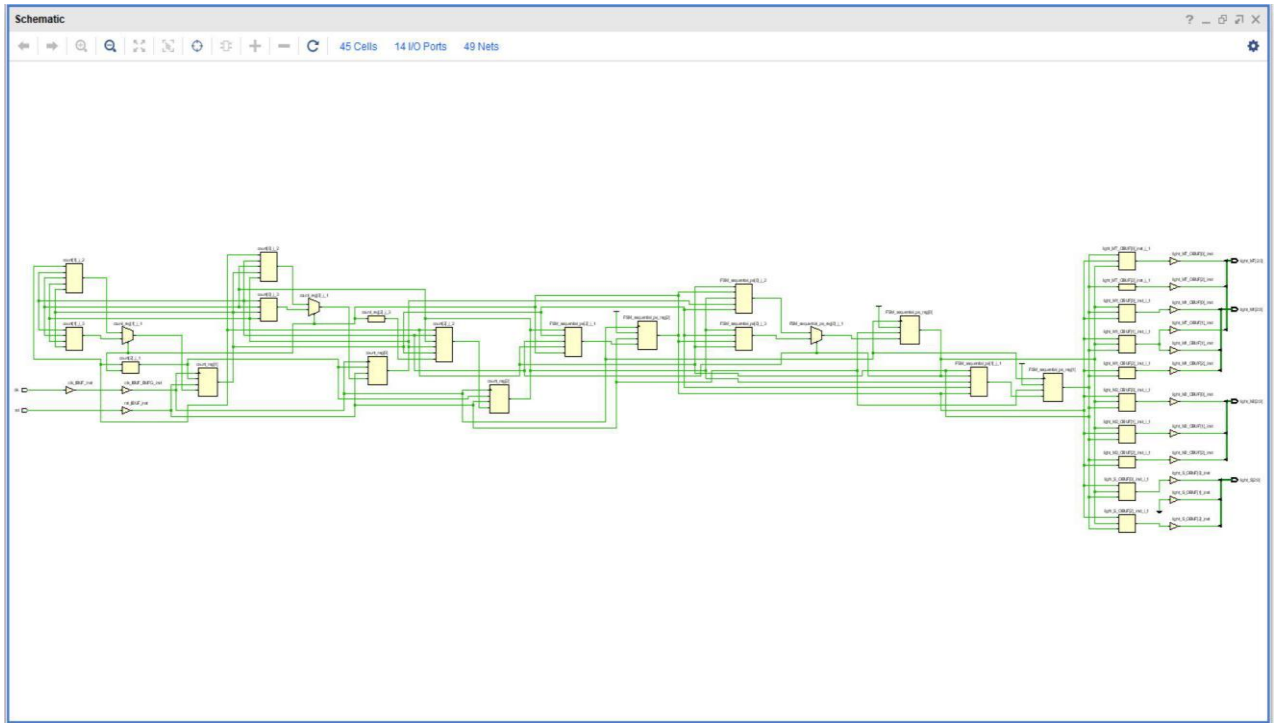
IO PORT ASSIGNMENT :



Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type
All ports (14)											
light_M1 (3)	OUT			✓	15	LVCMOS33*	3.300		12	SLOW	NONE
light_M1[2]	OUT		H17	✓	15	LVCMOS33*	3.300		12	SLOW	NONE
light_M1[1]	OUT		K15	✓	15	LVCMOS33*	3.300		12	SLOW	NONE
light_M1[0]	OUT		J13	✓	15	LVCMOS33*	3.300		12	SLOW	NONE
light_M2 (3)	OUT			✓	14	LVCMOS33*	3.300		12	SLOW	NONE
light_M2[2]	OUT		N14	✓	14	LVCMOS33*	3.300		12	SLOW	NONE
light_M2[1]	OUT		R18	✓	14	LVCMOS33*	3.300		12	SLOW	NONE
light_M2[0]	OUT		V17	✓	14	LVCMOS33*	3.300		12	SLOW	NONE
light_MT (3)	OUT			✓	14	LVCMOS33*	3.300		12	SLOW	NONE
light_MT[2]	OUT		U17	✓	14	LVCMOS33*	3.300		12	SLOW	NONE
light_MT[1]	OUT		V16	✓	14	LVCMOS33*	3.300		12	SLOW	NONE
light_MT[0]	OUT		T15	✓	14	LVCMOS33*	3.300		12	SLOW	NONE
light_S (3)	OUT			✓	14	LVCMOS33*	3.300		12	SLOW	NONE
light_S[2]	OUT		U14	✓	14	LVCMOS33*	3.300		12	SLOW	NONE
light_S[1]	OUT		T16	✓	14	LVCMOS33*	3.300		12	SLOW	NONE
light_S[0]	OUT		V15	✓	14	LVCMOS33*	3.300		12	SLOW	NONE
Scalar ports (2)											

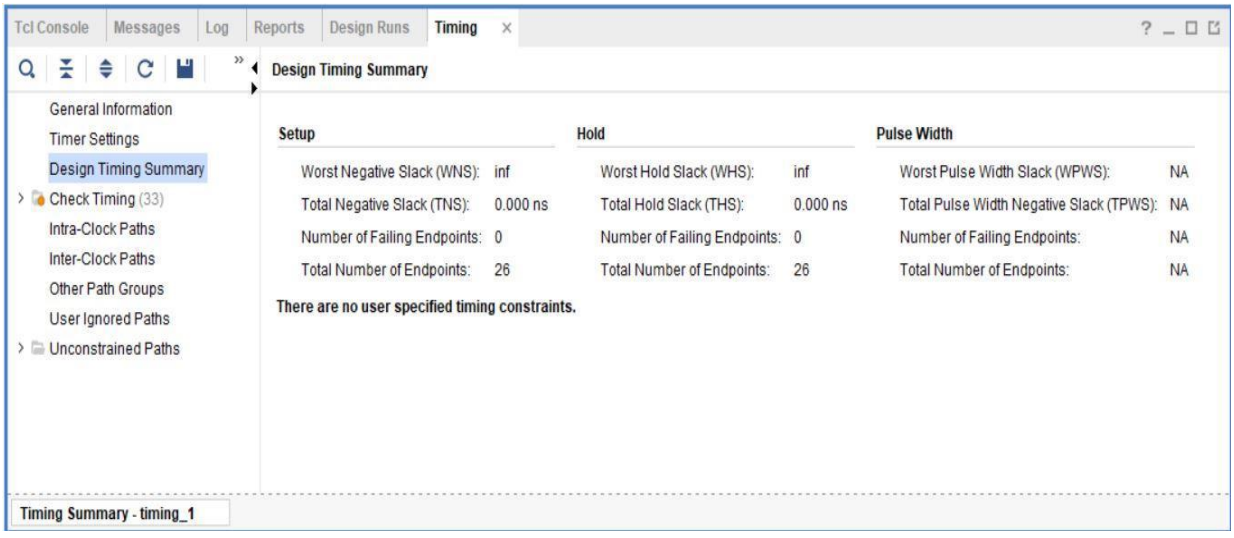
The ports are assigned from the ucf file.

SCHEMATIC AFTER SYNTHESIS :

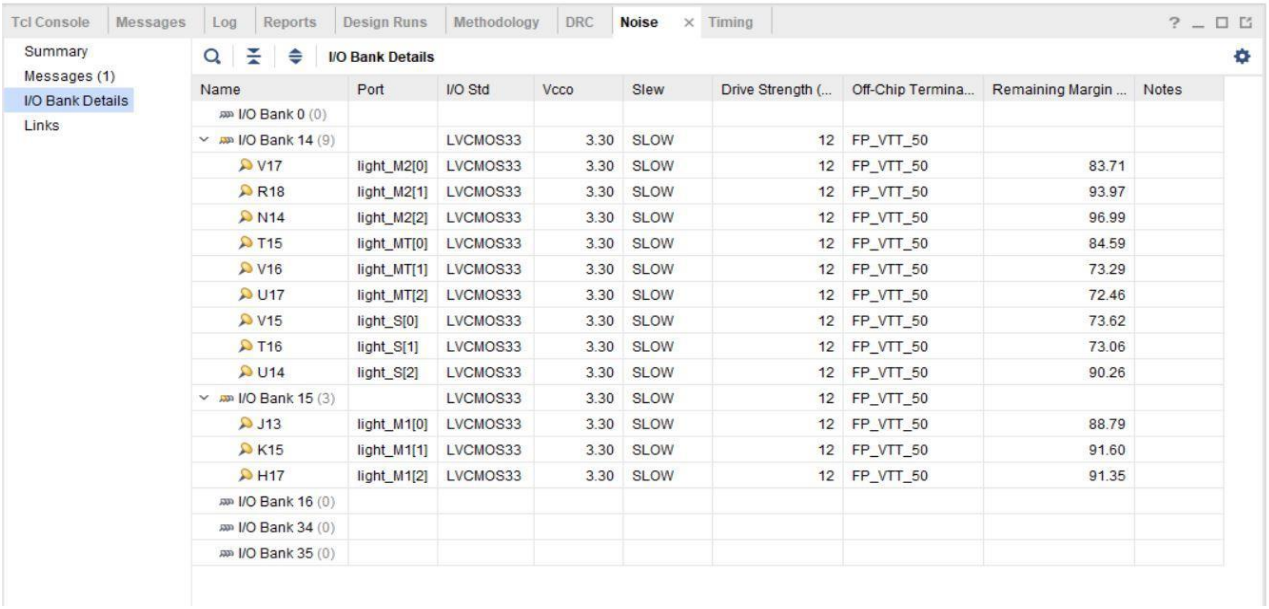


REPORTS AFTER SYNTHESIS :

1. TIMING REPORT :-



2. NOISE REPORT :-



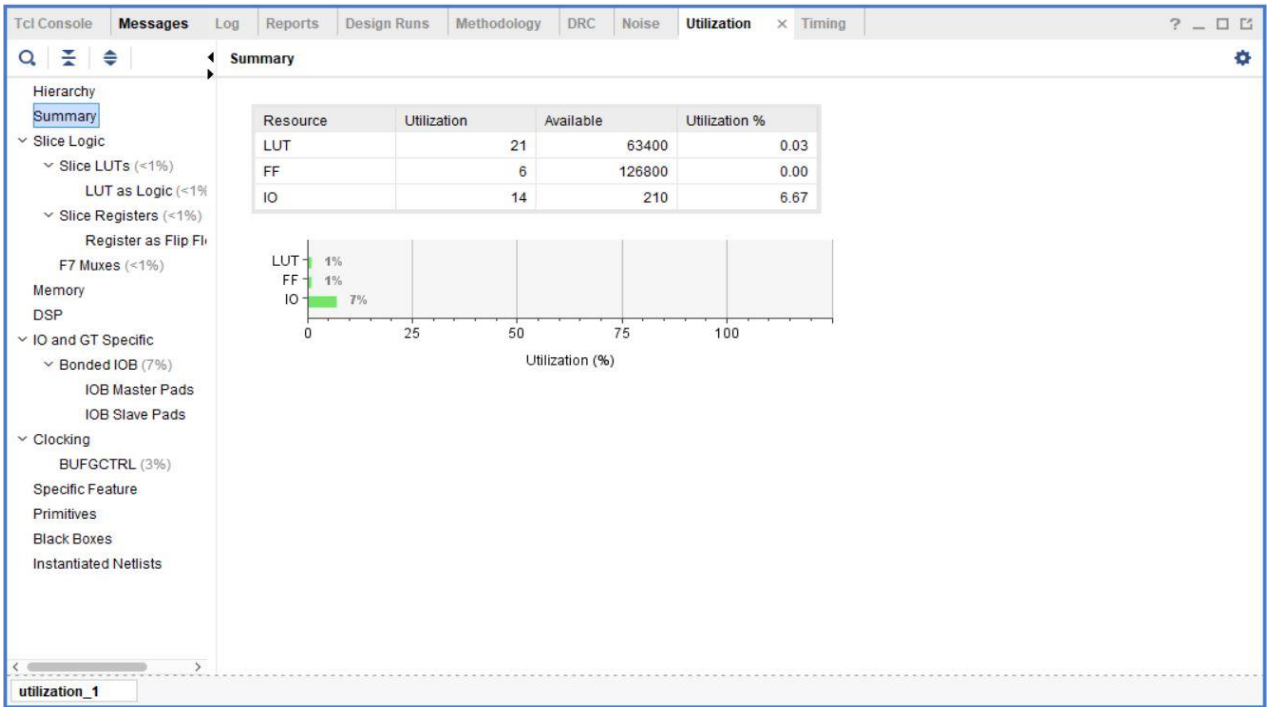
Tcl Console | Messages | Log | Reports | Design Runs | Methodology | DRC | Noise | Timing

Summary
Messages (1)
I/O Bank Details
Links

I/O Bank Details

Name	Port	I/O Std	Vcco	Slew	Drive Strength (...	Off-Chip Termina...	Remaining Margin ...	Notes
I/O Bank 0 (0)								
I/O Bank 14 (9)		LVCMOS33	3.30	SLOW	12	FP_VTT_50		
V17	light_M2[0]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	83.71	
R18	light_M2[1]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	93.97	
N14	light_M2[2]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	96.99	
T15	light_MT[0]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	84.59	
V16	light_MT[1]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	73.29	
U17	light_MT[2]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	72.46	
V15	light_S[0]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	73.62	
T16	light_S[1]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	73.06	
U14	light_S[2]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	90.26	
I/O Bank 15 (3)		LVCMOS33	3.30	SLOW	12	FP_VTT_50		
J13	light_M1[0]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	88.79	
K15	light_M1[1]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	91.60	
H17	light_M1[2]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	91.35	
I/O Bank 16 (0)								
I/O Bank 34 (0)								
I/O Bank 35 (0)								

3. UTILIZATION REPORT :-



Tcl Console | Messages | Log | Reports | Design Runs | Methodology | DRC | Noise | Utilization | Timing

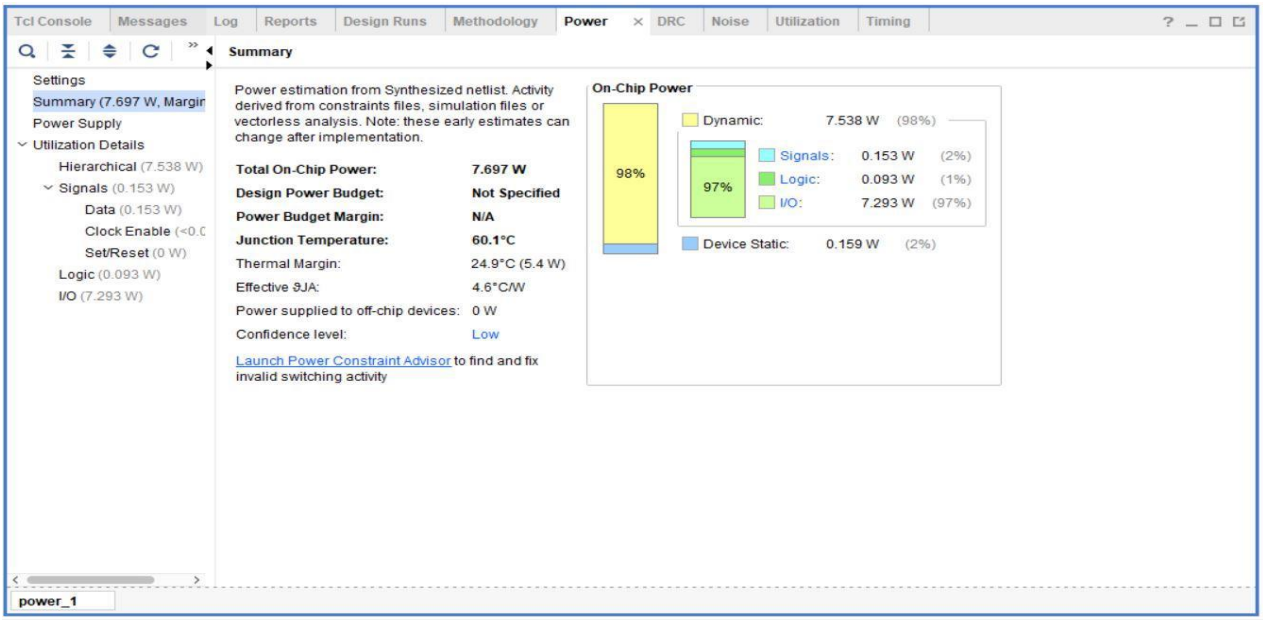
Summary

Hierarchy
Summary
Slice Logic
Slice LUTs (<1%)
LUT as Logic (<1%
Slice Registers (<1%)
Register as Flip Fl
F7 Muxes (<1%)
Memory
DSP
IO and GT Specific
Bonded IOB (7%)
IOB Master Pads
IOB Slave Pads
Clocking
BUFGCTRL (3%)
Specific Feature
Primitives
Black Boxes
Instantiated Netlists

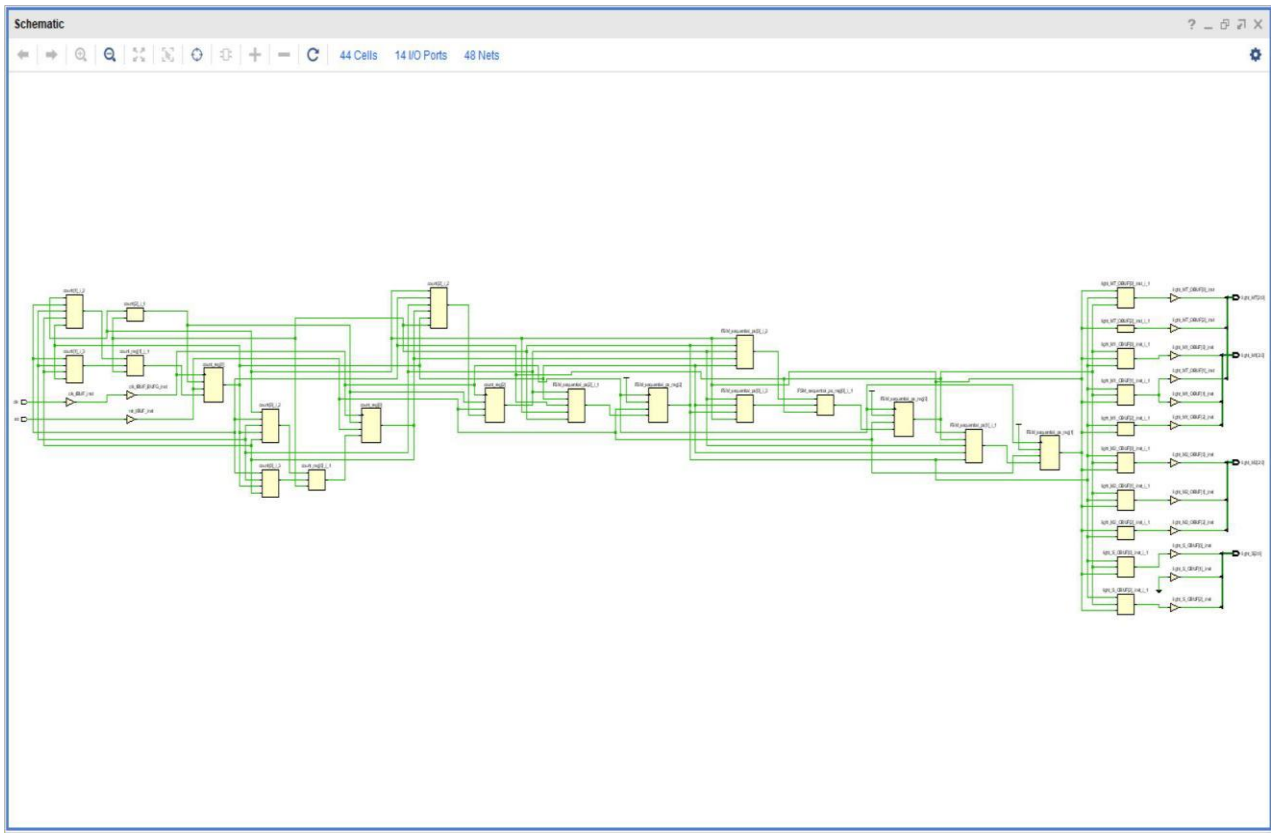
Resource	Utilization	Available	Utilization %
LUT	21	63400	0.03
FF	6	126800	0.00
IO	14	210	6.67

utilization_1

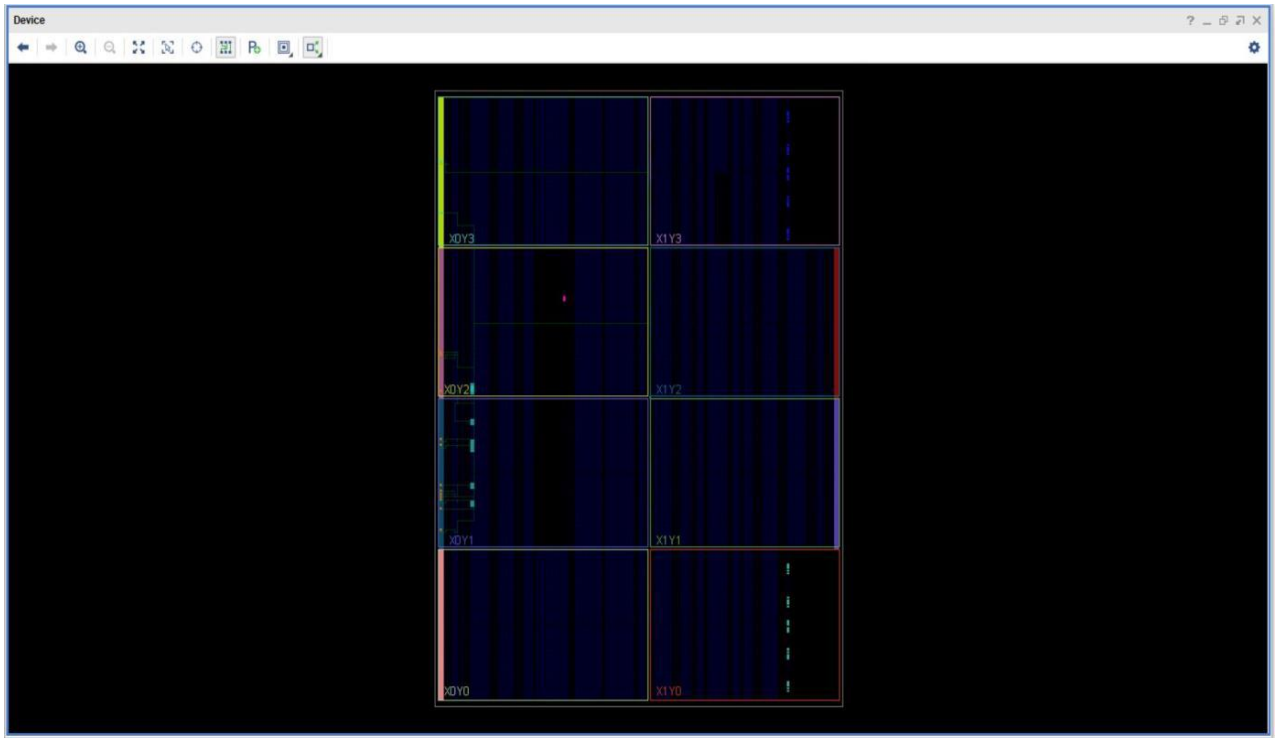
4. POWER REPORT :-



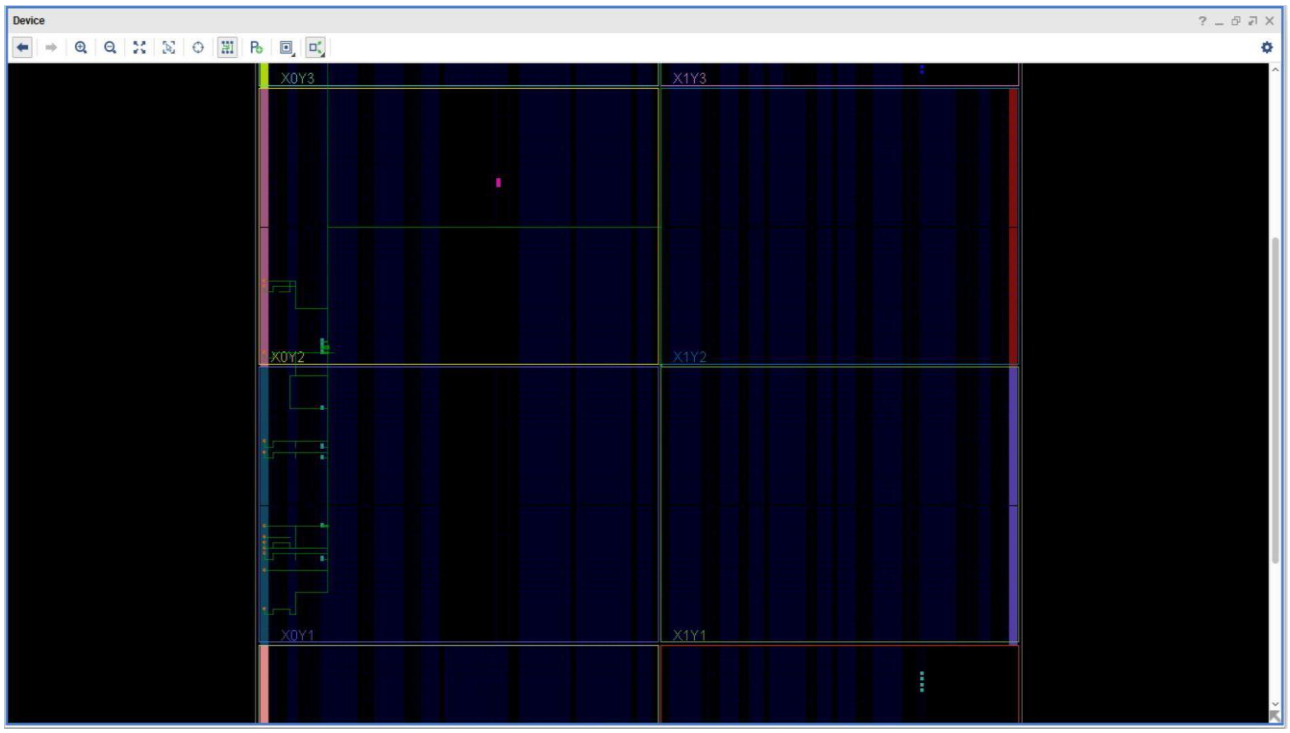
SCHEMATIC AFTER IMPLEMENTATION :



DEVICE LAYOUT AFTER IMPLEMENTATION :

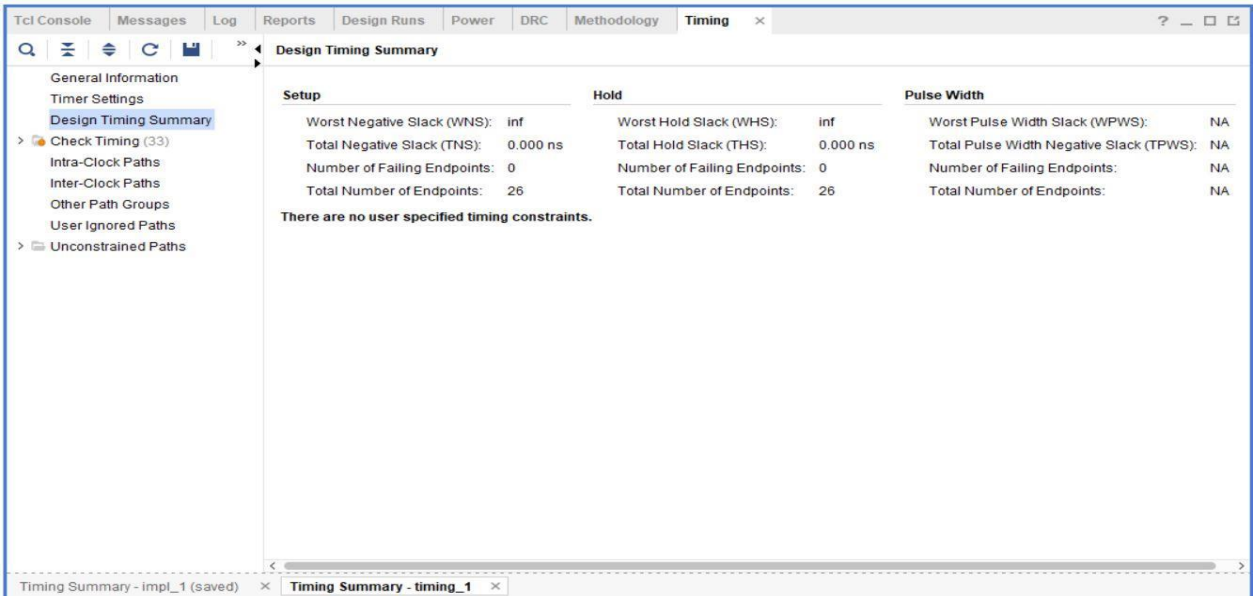


ZOOM IN VIEW :

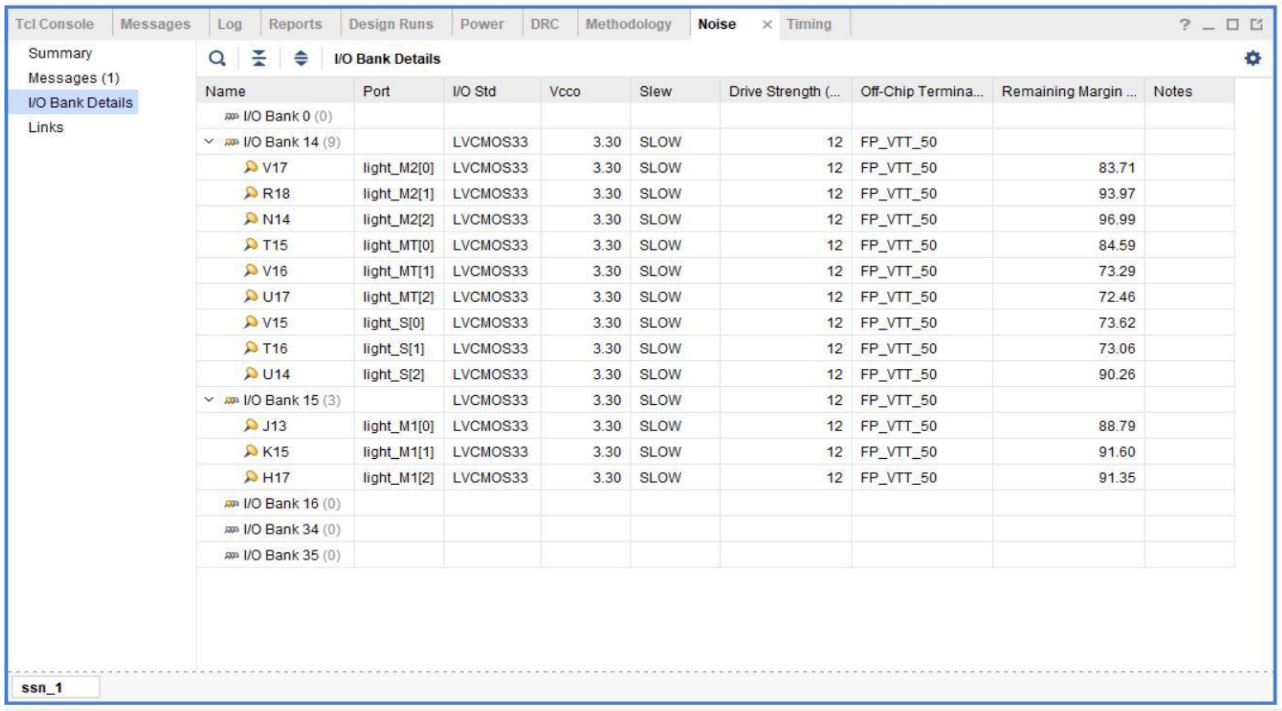


REPORTS AFTER IMPLEMENTATION :

A. TIMING REPORT :-



B. NOISE REPORT :-



Name	Port	I/O Std	Vcco	Slew	Drive Strength (...	Off-Chip Termina...	Remaining Margin ...	Notes
I/O Bank 0 (0)								
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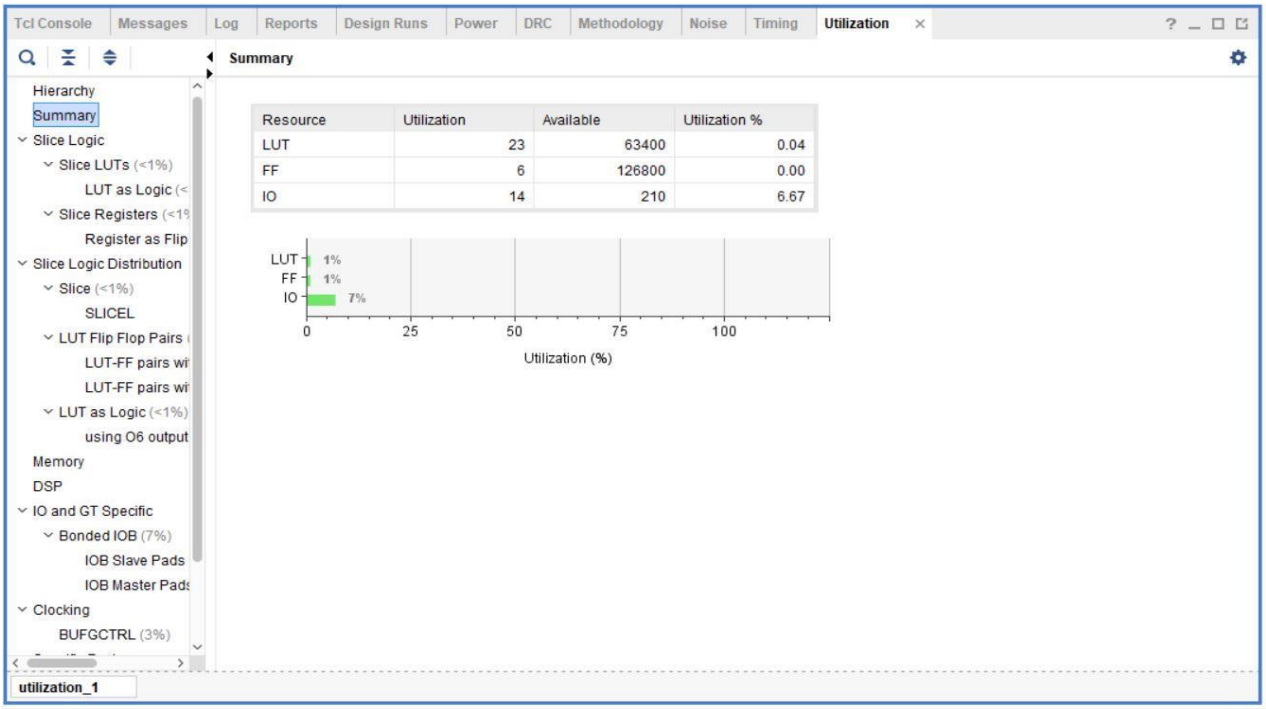
U17	light_MT[2]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	72.46	
V15	light_S[0]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	73.62	
T16	light_S[1]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	73.06	
U14	light_S[2]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	90.26	
I/O Bank 15 (3)		LVCMOS33	3.30	SLOW	12	FP_VTT_50		
J13	light_M1[0]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	88.79	
K15	light_M1[1]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	91.60	
H17	light_M1[2]	LVCMOS33	3.30	SLOW	12	FP_VTT_50	91.35	
I/O Bank 16 (0)								
I/O Bank 34 (0)								
I/O Bank 35 (0)								

C. UTILIZATION REPORT :-



D. POWER REPORT :-