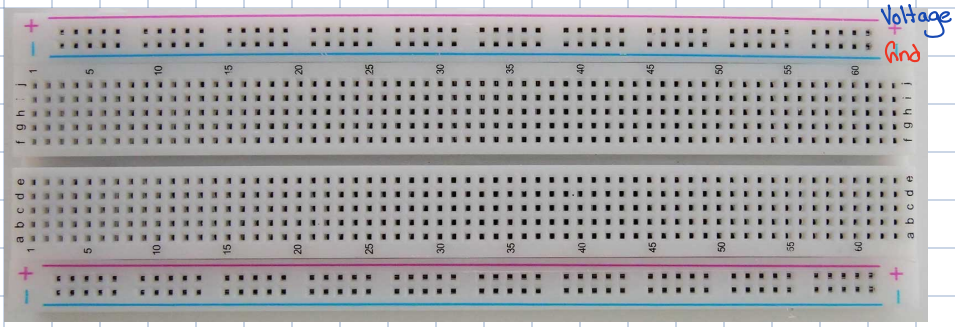
Lab: 01 Introduction to Lab



Lab 2: Logic Gates & truth table

NAND / AND / OR(7432) / XOR

VOLT	in	in	out	in	in	out
14	13	12	11	10	9	8

1	2	3	4	5	6	7
in	in	out	in	in	out	AND

OR(4071) / XNOR

VOLT	in	in	out	out	in	in
14	13	12	11	10	9	8

1	2	3	4	5	6	7
in	in	out	out	in	in	AND

NOT

VOLT	in	out	in	out	in	out
14	13	12	11	10	9	8

1	2	3	4	5	6	7
in	out	in	out	in	out	AND

NOR

VOLT	out	in	in	out	in	in
14	13	12	11	10	9	8

1	2	3	4	5	6	7
out	in	in	out	in	in	AND

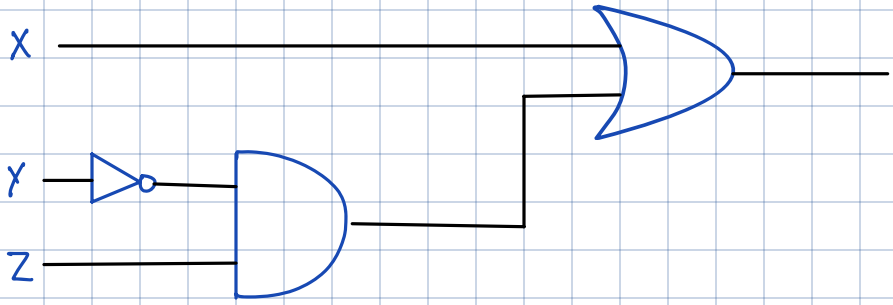
A	B	$A \cdot B$	$A+B$	$\overline{A+B}$	$\overline{A \cdot B}$	$A \oplus B$	$\overline{A \oplus B}$	$\overline{A}$
0	0	0	0	1	1	0	1	1
0	1	0	1	0	1	1	0	1
1	0	0	1	0	1	1	0	0
1	1	1	1	0	0	0	1	0

Lab: 03 Boolean Algebra & De Morgan's Law

Task 01:

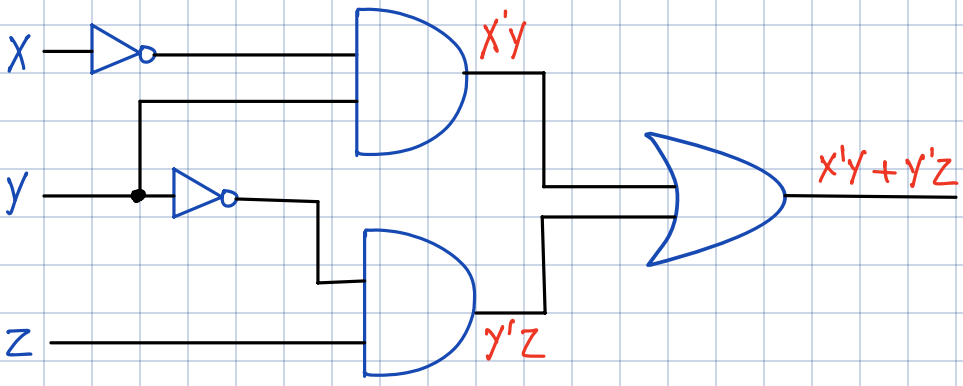
Expression: $X + y'z$

Circuit:



Task 02:

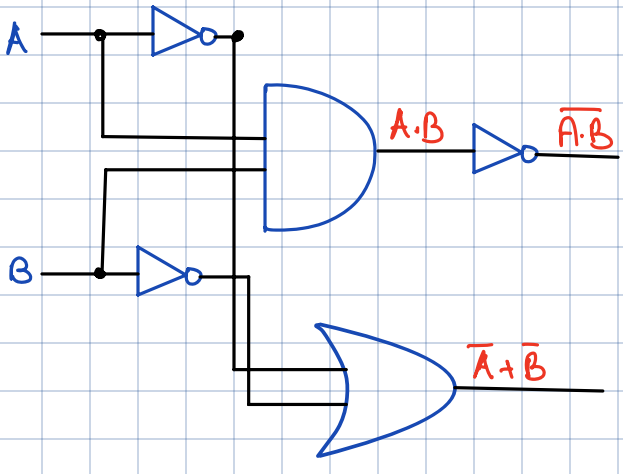
Expression: $x'y + y'z$



Task :03

Expression: $\overline{A \cdot B} = \overline{A} + \overline{B}$

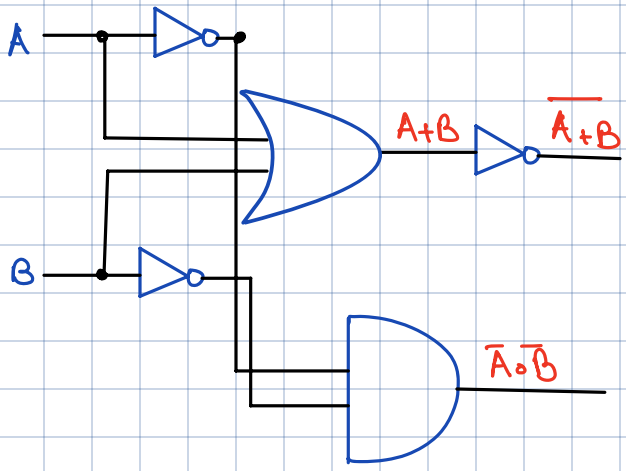
Circuit:



Task: 04

Expression: $\overline{A+B} = \overline{A}.\overline{B}$

Circuit:



Lab: 04 Combination Logic circuit

Task: 01 : Half adder

Expression:

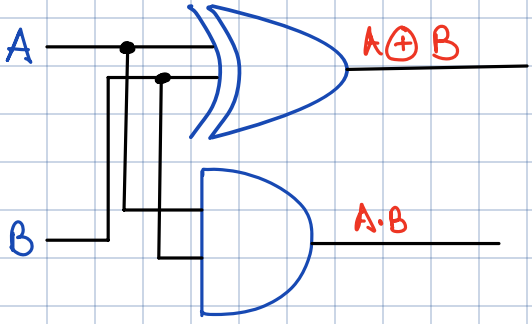
Sum: $A \oplus B$ → addert

Carry: $A.B$ → cygent

Truth table

A	B	Sum $A \oplus B$	carry $A.B$
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Circuit:



Task 02: Full Adder

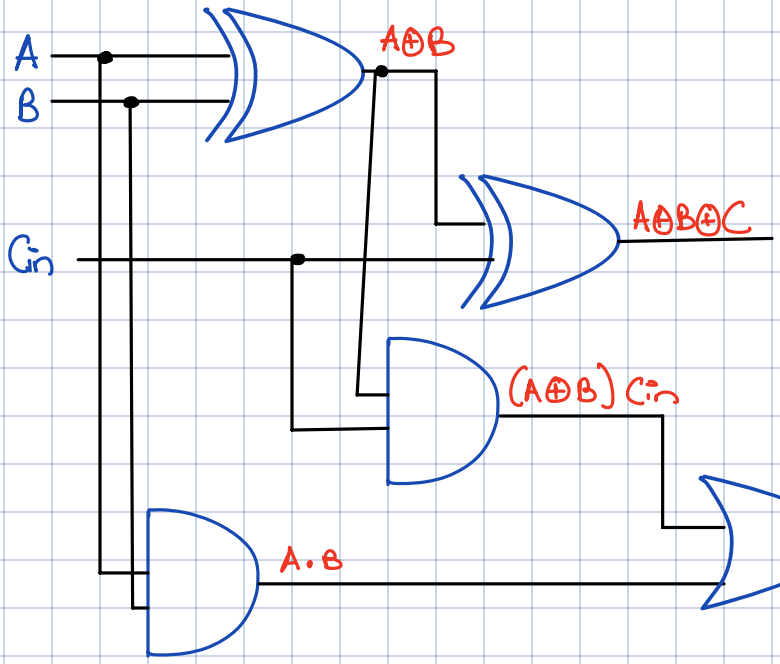
Expression:

Sum: $A \oplus B \oplus C_{in}$

Carry: $A.B + (A \oplus B).C_{in}$

Circuit

Truth table



A	B	Cin	A⊕B⊕Cin	A.B + (A⊕B)Cin
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Task: 03: Half subtractor

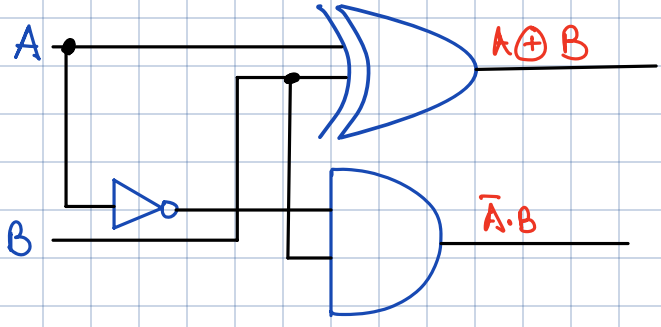
Expression: (minuend, subtrahend)

sum: $A \oplus B$

Borrow: $\bar{A}B$

Truth table

A	B	sub $A \oplus B$	Borrow $\bar{A} \cdot B$
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0



Task: 04: Full subtractor

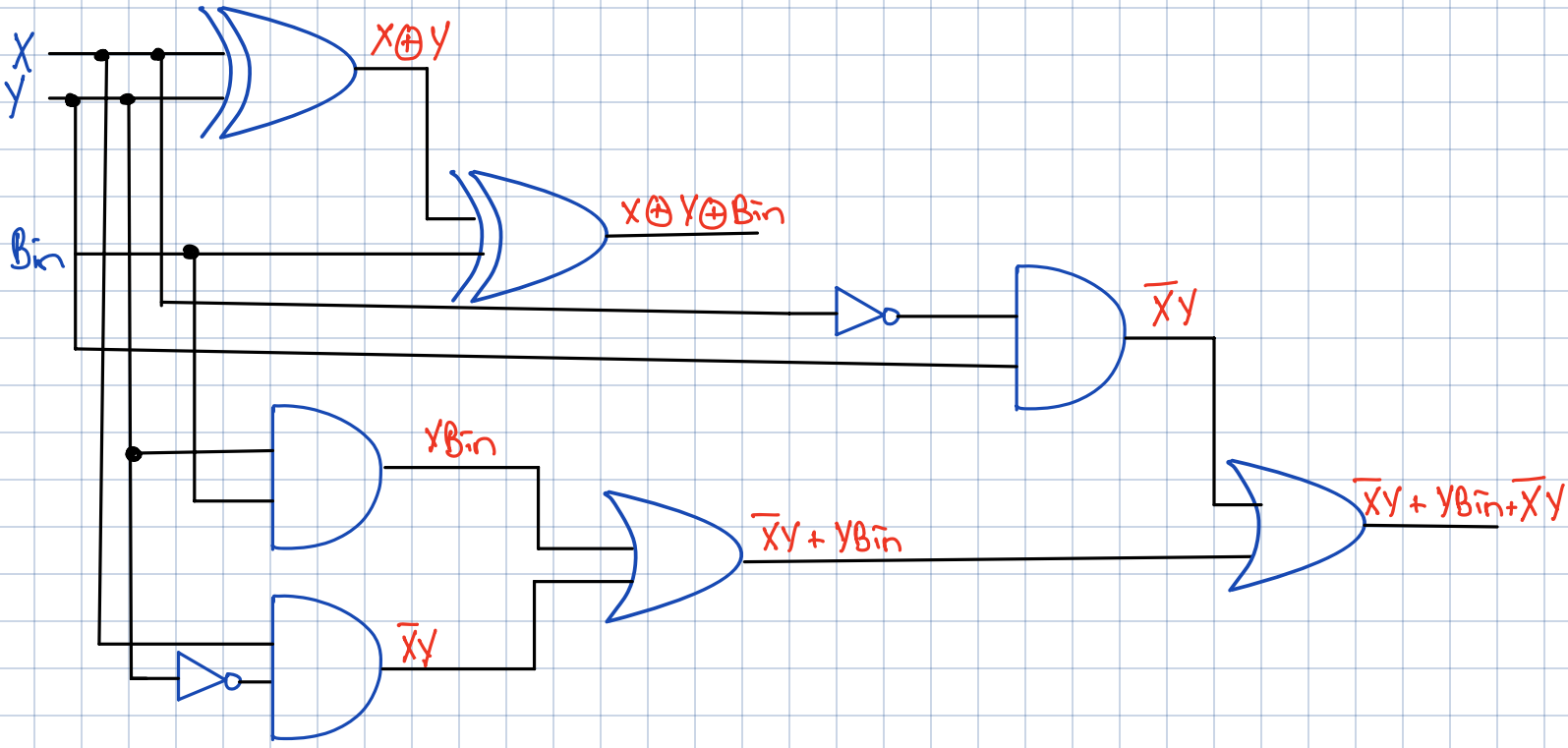
Expression:

Sub: $X \oplus Y \oplus B_{in}$

Borrow: $\bar{X}B_{in} + \bar{X}Y + YB_{in}$

Truth table

X	Y	B_{in}	$X \oplus Y \oplus B_{in}$	$\bar{X}Y + \bar{X}B_{in} + YB_{in}$
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



Task: 04 : Two bit adder

Expression:

$S_0 = A_0 \oplus B_0$

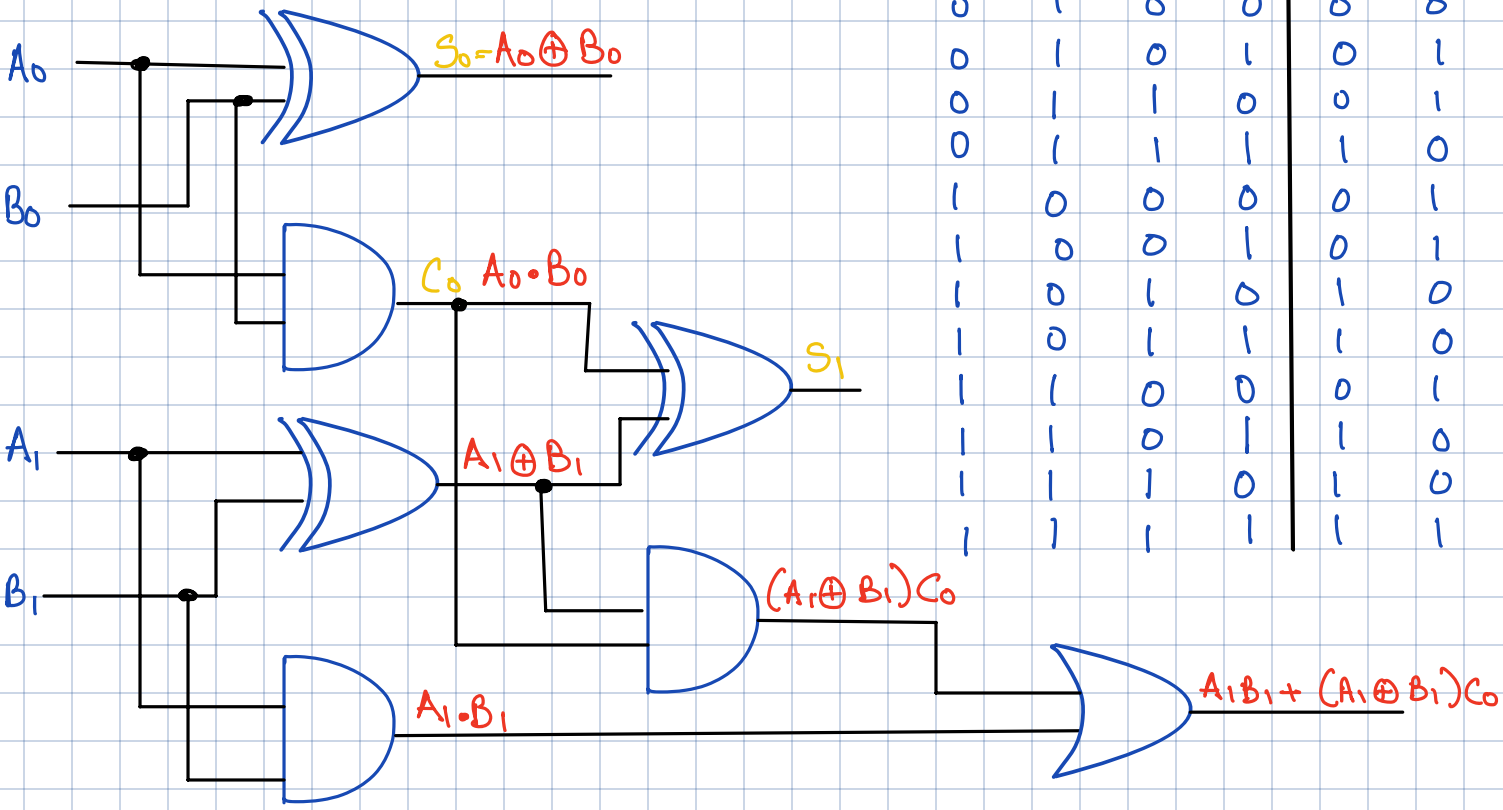
$C_0 = A_0 \cdot B_0$

$S_1 = A_1 \oplus B_1 \oplus C_0$

$C_1 = A_1 B_1 + (A_1 \oplus B_1) C_0$

Truth table

A_1	A_0	B_1	B_0	C_1	S_1	S_0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0



Lab: 05: Encoders & Decoders

Decoder:

Task: 01: 2x4

Truth table

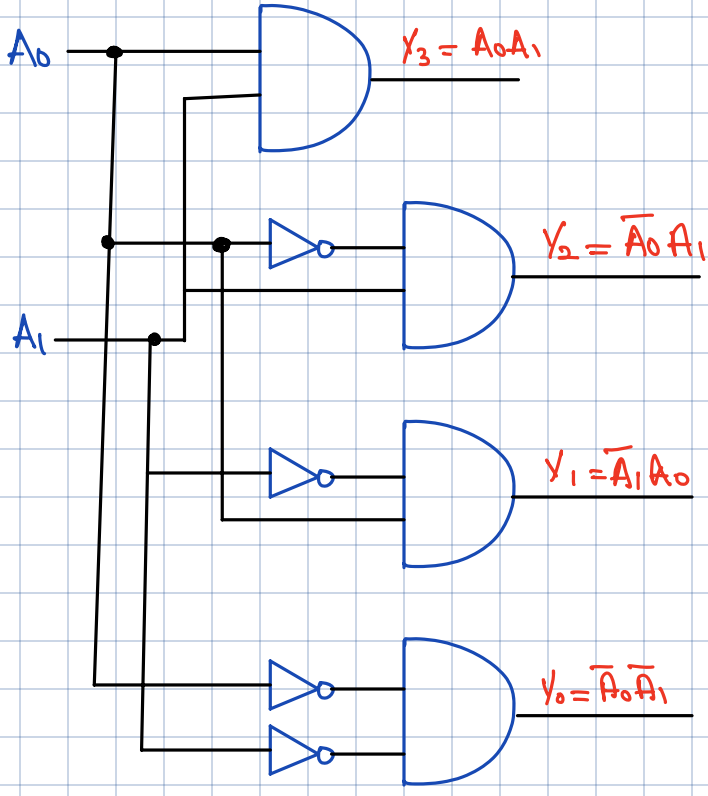
A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Expression:

$Y_0 = \bar{A_1}\bar{A_0}$ $Y_2 = A_1\bar{A_0}$

$Y_1 = \bar{A_1}A_0$ $Y_3 = A_1A_0$

Circuit:



Task: 02: 3x8

Truth table

A_2	A_1	A_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	0								1
0	0	1							1	
0	1	0						1		
0	1	1					1			
1	0	0				1				
1	0	1			1					
1	1	0		1						
1	1	1	1							

Expression:

$Y_0 = \bar{A_0}\bar{A_1}\bar{A_2}$ $Y_1 = A_0\bar{A_1}\bar{A_2}$

$Y_2 = \bar{A_0}A_1\bar{A_2}$ $Y_3 = A_0A_1\bar{A_2}$

$Y_4 = \bar{A_0}\bar{A_1}A_2$ $Y_5 = A_0\bar{A_1}A_2$

$Y_6 = \bar{A_0}A_1A_2$ $Y_7 = A_0A_1A_2$

Encoder:

Task:03

Truth table

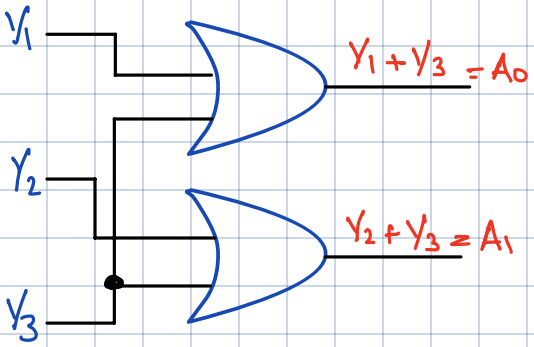
Y_3	Y_2	Y_1	Y_0	A_1	A_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

Expression:

$A_0 = Y_1 + Y_3$

$A_1 = Y_2 + Y_3$

Circuit



Task 04: 8 x 3 (Octal to Binary)

Truth table

Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0	A2	A1	A0
							1	0	0	0
						1		0	0	1
					1			0	1	0
				1				0	1	1
			1					1	0	0
		1						1	0	1
	1							1	1	0
1								1	1	1

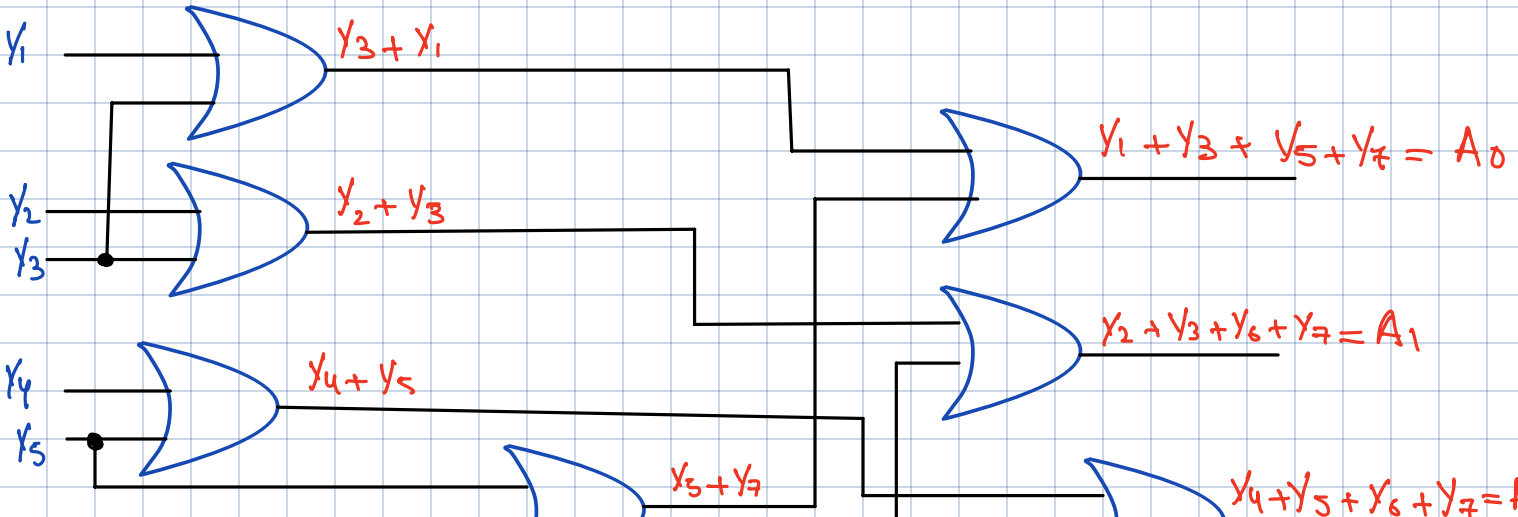
Expression:

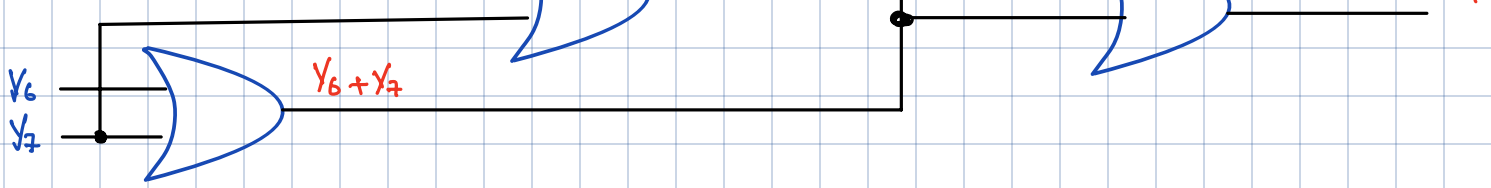
$A2 = Y_4 + Y_5 + Y_6 + Y_7$

$A1 = Y_2 + Y_3 + Y_6 + Y_7$

$A0 = Y_1 + Y_3 + Y_5 + Y_7$

Circuit





Task 05: 10 x 4 (Decimal to BCD)

Expression:

$A3 = I_8 + I_9$

$A2 = I_4 + I_5 + I_6 + I_7$

$A1 = I_2 + I_3 + I_6 + I_7$

$A0 = I_1 + I_3 + I_5 + I_7 + I_9$

Truth table

	A_3	A2	A1	A_0
I_0	0	0	0	0
I_1	0	0	0	1
I_2	0	0	1	0
I_3	0	0	1	1
I_4	0	1	0	0
I_5	0	1	0	1
I_6	0	1	1	0
I_7	0	1	1	1
I_8	1	0	0	0
I_9	1	0	0	1

Lab: 06: De'd Multiplexer

Multiplexer

Task 01: 4 x 1

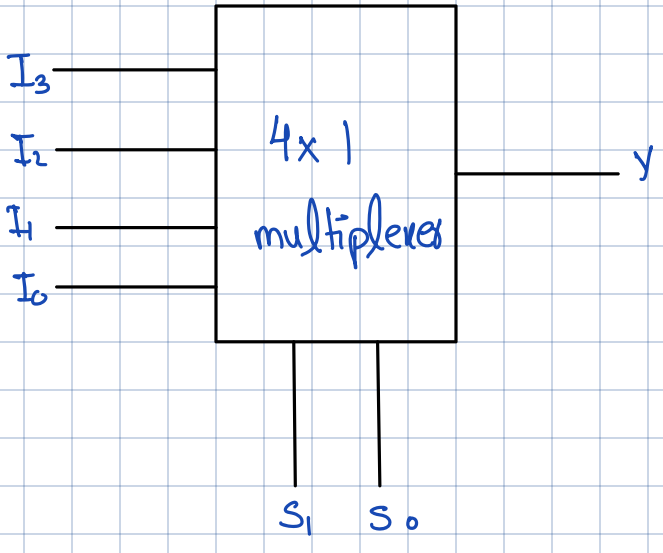
Expression:

$Y = \overline{S_1}\,\overline{S_0} I_0 + \overline{S_1} S_0 I_1 + S_1 \overline{S_0} I_2 + S_1 S_0 I_3$

Truth table

I_3	I_2	I_1	I_0	S_1	S_0	y
			1	0	0	I_0
		1		0	1	I_1
	1			1	0	I_2
1				1	1	I_3

Circuit:



Task 02: 8x1

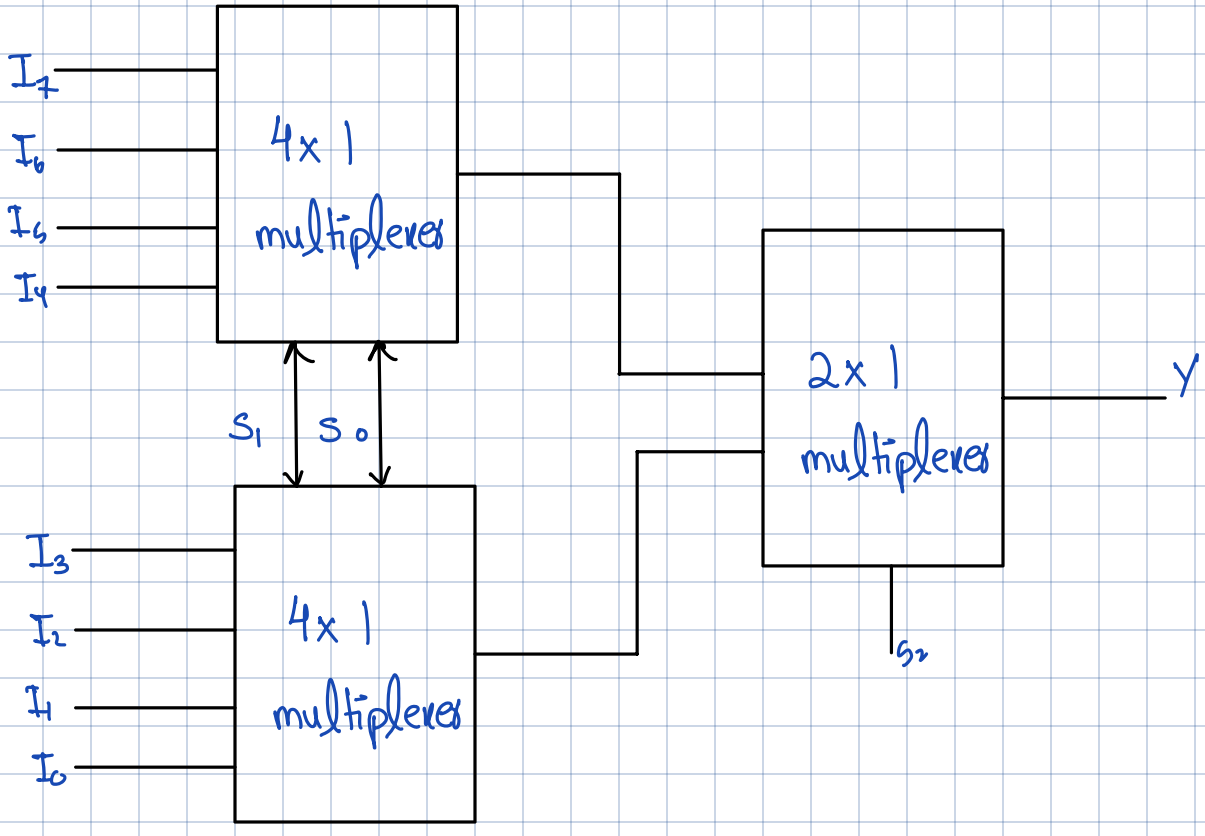
Expression:

$$Y = \bar{S}_2\bar{S}_1\bar{S}_0 I_0 + \bar{S}_2\bar{S}_1 S_0 I_1 + \bar{S}_2 S_1\bar{S}_0 I_2 + \bar{S}_2 S_1 S_0 I_3 + S_2\bar{S}_1\bar{S}_0 I_4 + S_2\bar{S}_1 S_0 I_5 + S_2 S_1\bar{S}_0 I_6 + S_2 S_1 S_0 I_7$$

Truth table

I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	S_2	S_1	S_0	Y
							1	0	0	0	I_0
						1		0	0	1	I_1
					1			0	1	0	I_2
				1				0	1	1	I_3
			1					1	0	0	I_4
		1						1	0	1	I_5
	1							1	1	0	I_6
1								1	1	1	I_7

Circuit.



De-Multiplexer

Task 03: 1x4

Expression

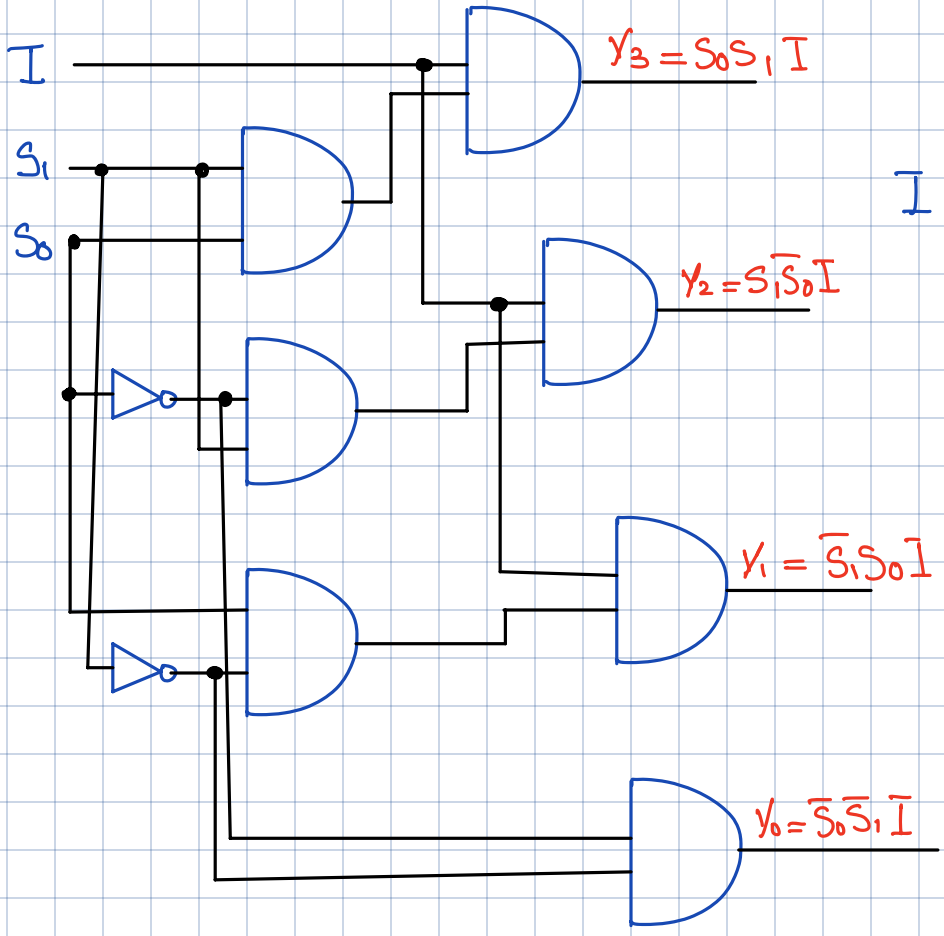
$Y_3 = S_1 S_0 I$ $\quad Y_1 = \bar{S}_1 S_0 I$

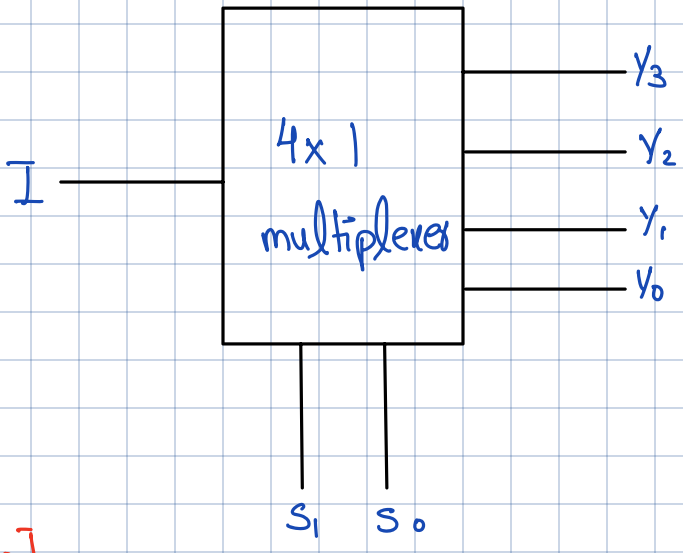
$Y_2 = S_1\bar{S}_0 I$ $\quad Y_0 = \bar{S}_1\bar{S}_0 I$

Truth table

I	S_1	S_0	Y_3	Y_2	Y_1	Y_0
I	0	0				I
I	0	1			I	
I	1	0		I		
I	1	1	I			

Circuit:


I
S_1
S_0
$Y_3 = S_0 S_1 I$
$Y_2 = S_1 \bar{S_0} I$
$Y_1 = \bar{S_1} S_0 I$
$Y_0 = \bar{S_0} \bar{S_1} I$


I
4x 1
multiplexer
Y_3
Y_2
Y_1
Y_0
S_1
S_0