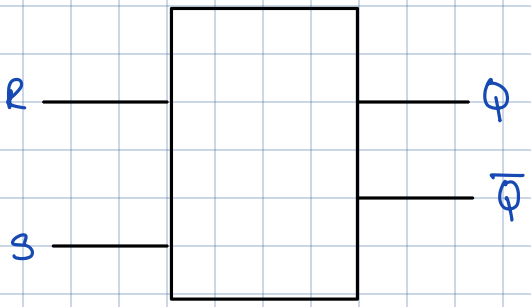
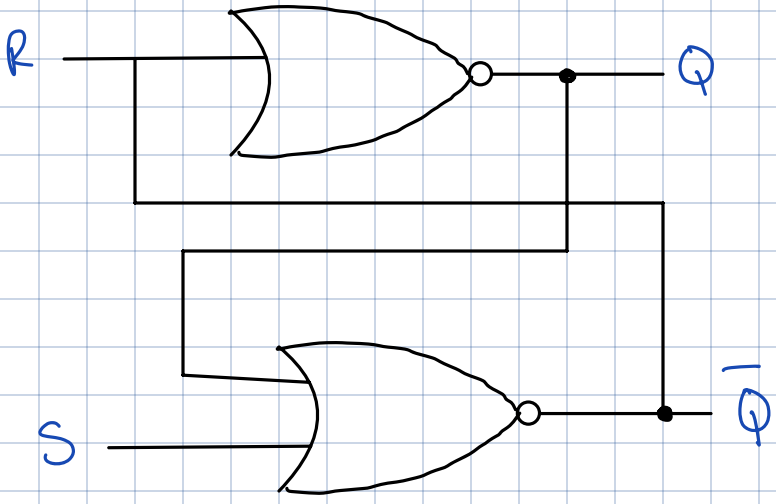
Latches:

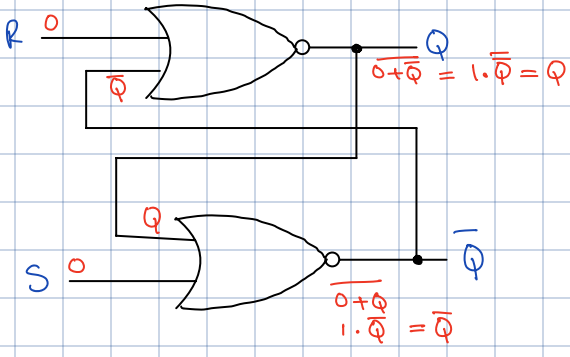
- Temporary storage device
- The basic form is SR Latch
- Created 2 NOR gates



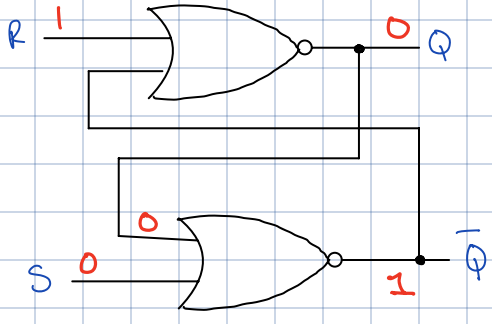


S	R	Q	$\bar{Q}$	
0	0	Q	$\bar{Q}$	Memory state
0	1	0	1	Reset Q
1	0	1	0	Set Q
1	1	Invalid mode		

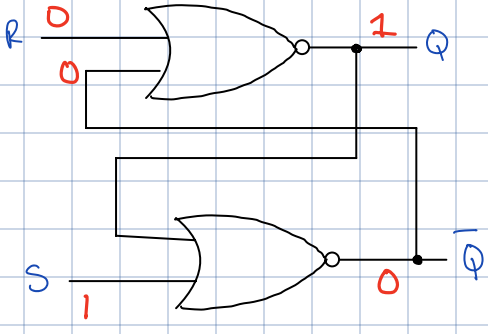
Case 01:



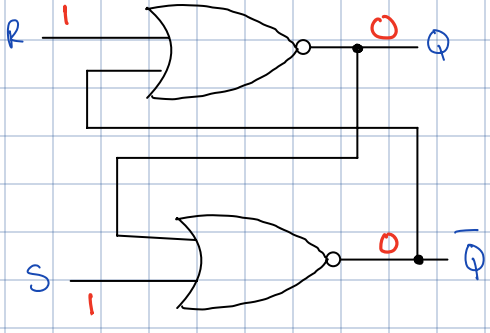
Case 02:



Case 03:



Case 04:



!!

- When there is atleast one 1, then output is 0.

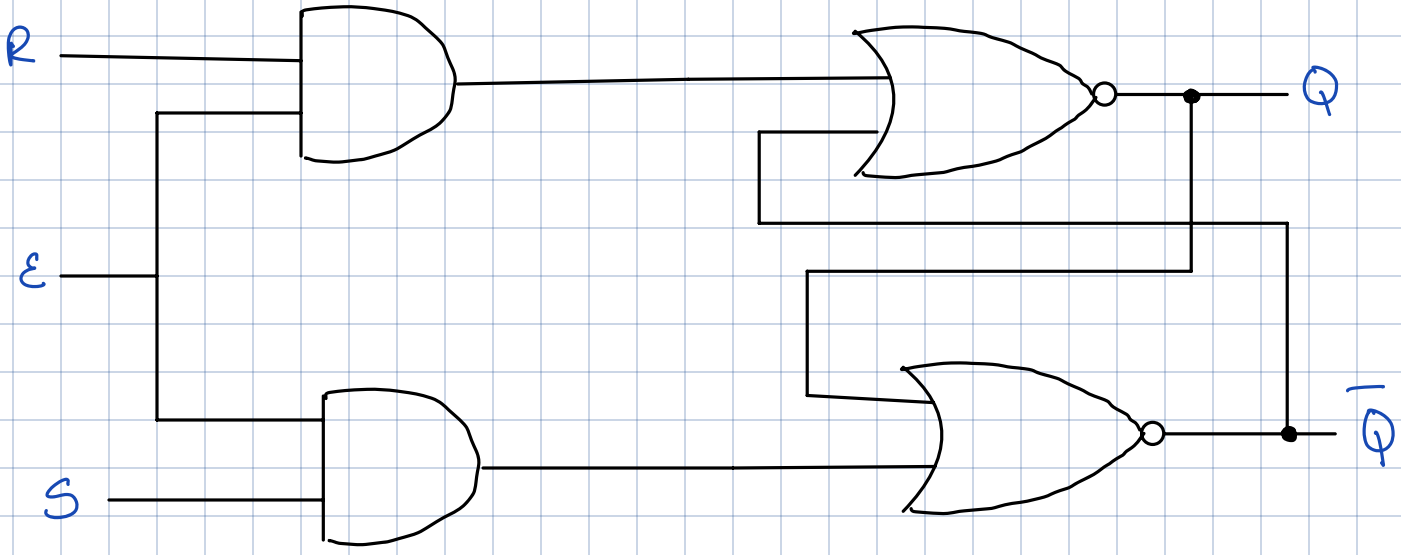
Disadvantages:

↳ It has an invalid mode

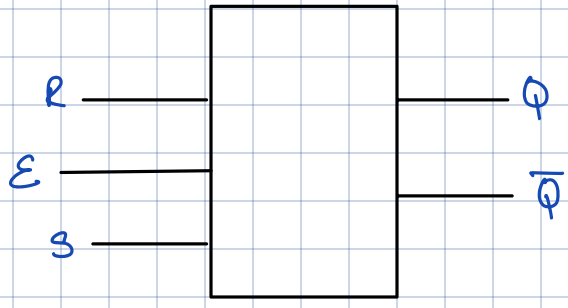
↳ Due to glitches, S & R values can change.

Gated S-R Latch:

↳ Reduces the possibility of glitches occuring.



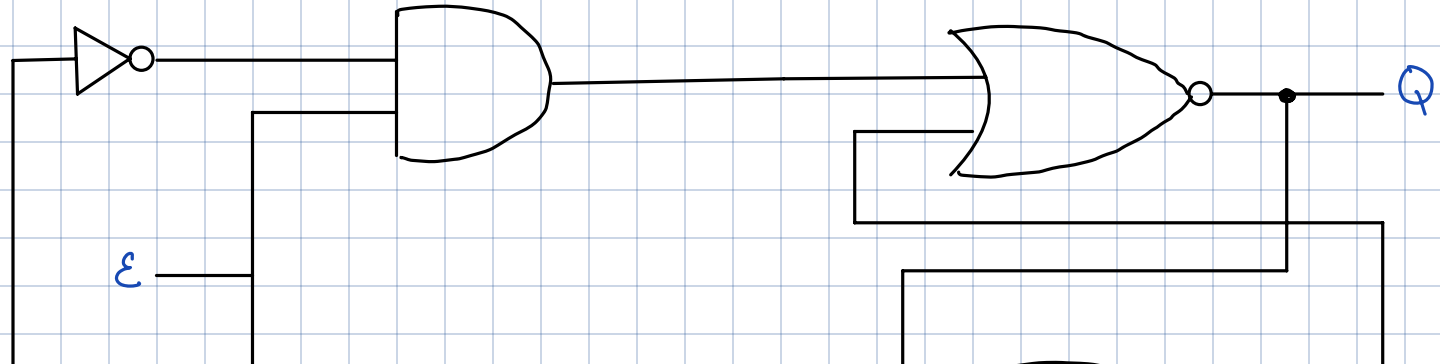
E	S	R	Q	$\overline{Q}$	
0	0	0	Q	$\overline{Q}$	
0	0	1	Q	$\overline{Q}$	
0	1	0	Q	$\overline{Q}$	
0	1	1	Q	$\overline{Q}$	
1	0	0	Q	$\overline{Q}$	
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	Invalid mode		



D- Latch:

↳ Combines S-R into D.

↳ Resolves the invalid mode



E	D	Q	$\bar{Q}$
0	0	Q	$\bar{Q}$
0	1	Q	$\bar{Q}$
1	0	0	1
1	1	1	0

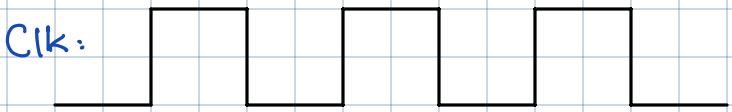
↳ Q follows D when E=1

Flip-flops:

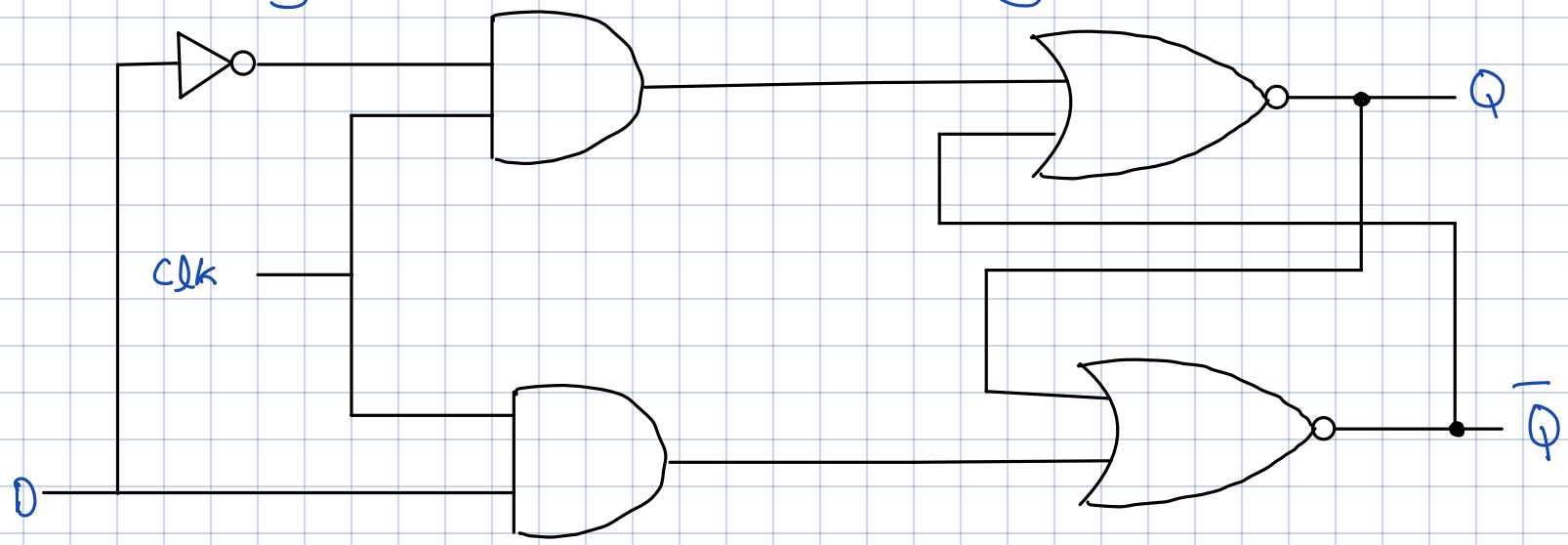
Latch: A latch can store data indefinitely only as long as the power is maintained. However, it is more prone to accidental overwriting because it updates immediately with input changes while enabled.

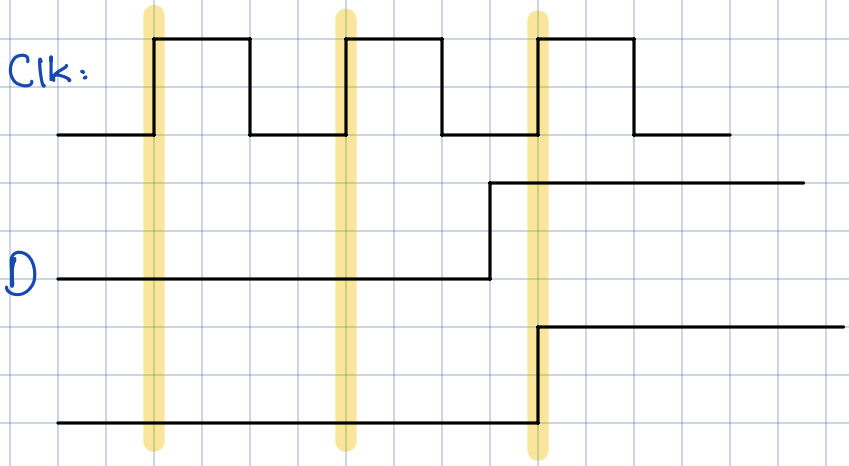
Flip-Flop: A flip-flop also stores data indefinitely (given power is supplied), but it does so in a much more controlled manner. It holds its state securely until the next clock edge triggers a potential update. This precise timing gives the impression that flip-flops "store data for infinite time."

Clk	D	Q	$\bar{Q}$	
0	X	Q	$\bar{Q}$	
↑	0	0	1	RESET
↑	1	1	0	SET



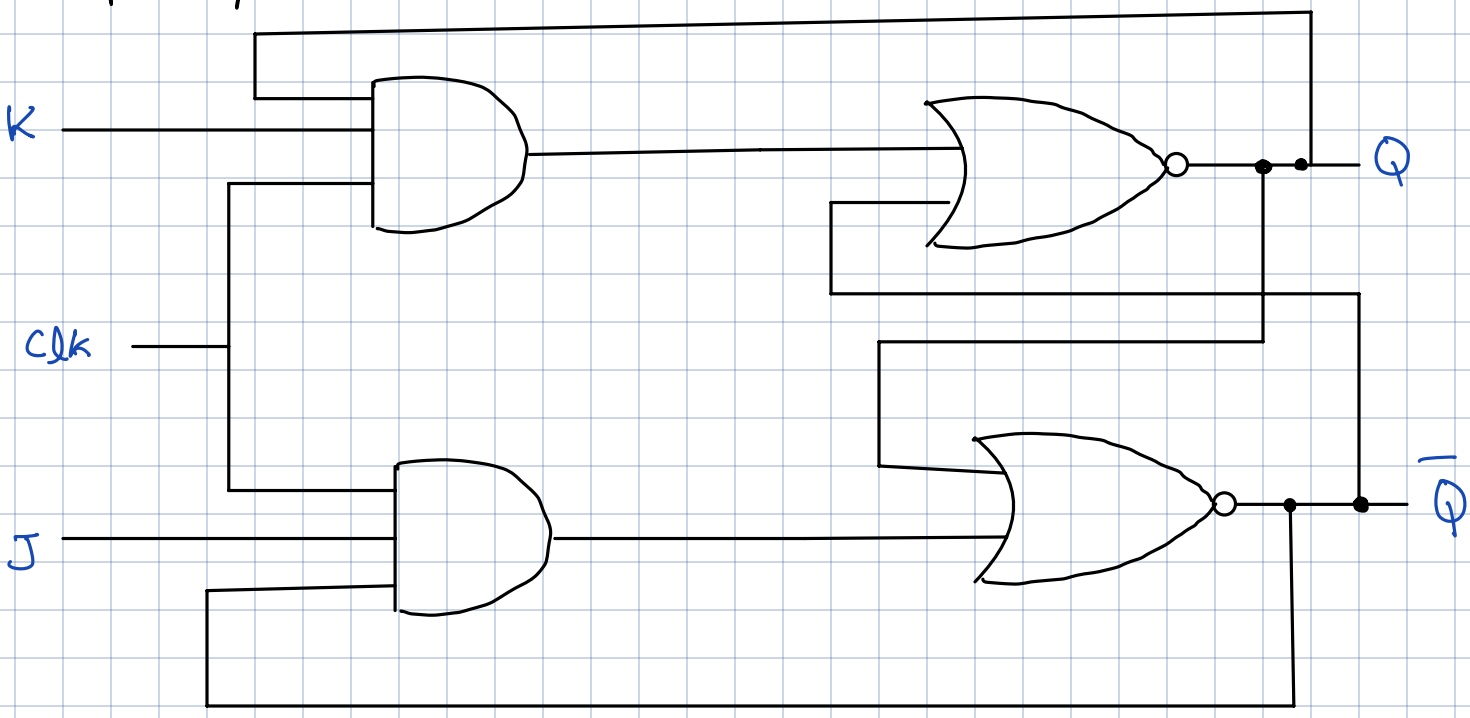
↳ when rising edge occurs, the flip flop changes it's state





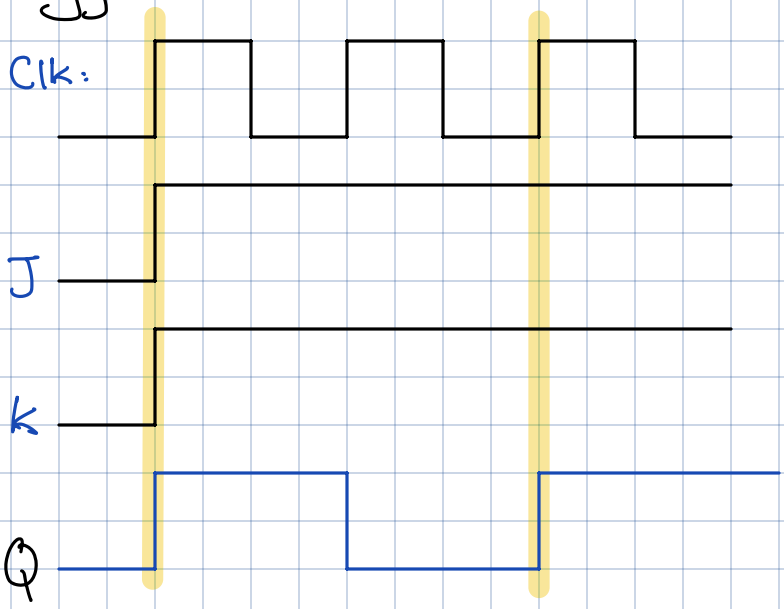
↳Q follows D.

J-K flip flop:

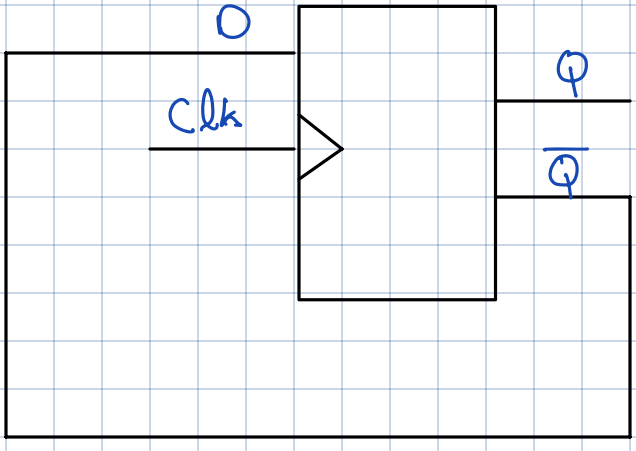


Clk	J	k	Q	$\overline{Q}$	
0	0	0	Q	$\overline{Q}$	
0	0	1	Q	$\overline{Q}$	
0	1	0	Q	$\overline{Q}$	
0	1	1	Q	$\overline{Q}$	
1	0	0	Q	$\overline{Q}$	
1	0	1	0	1	RESET
1	1	0	1	0	SET
1	1	1	Toggle mode		

Toggle mode:



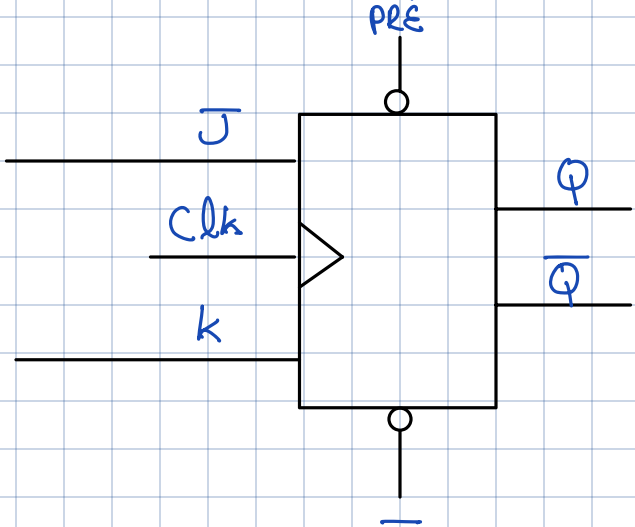
↳ D flip flop can be made to toggle as:



↳ Toggle mode acts as a frequency divider (by 2)

↳ User controlled inputs

Asynchronous flip flop:



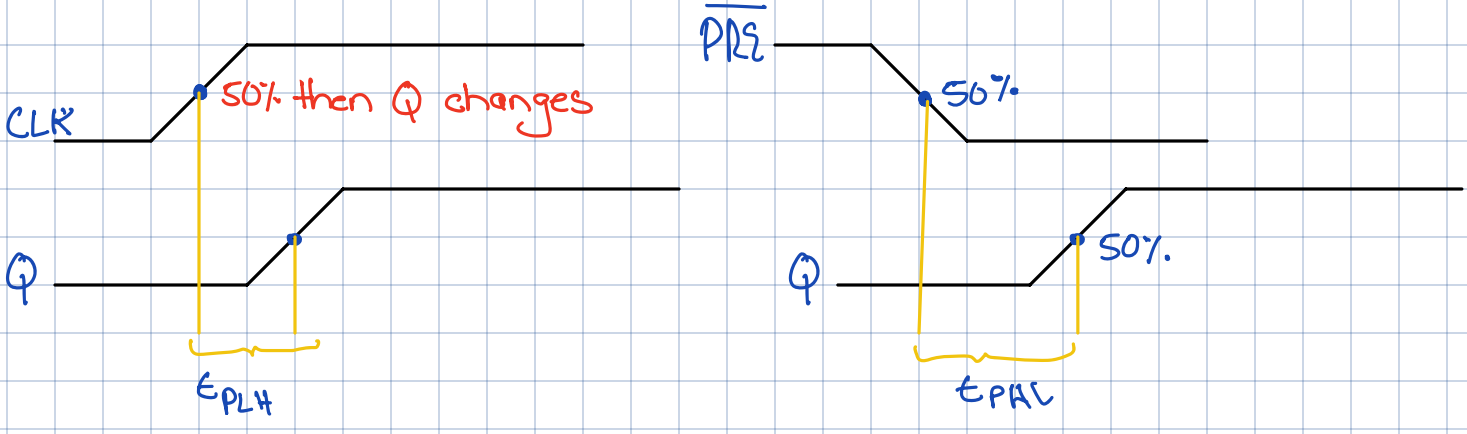
CLR

flip-flop characteristics

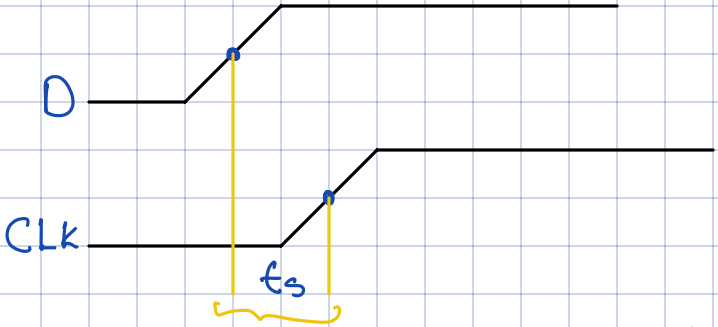
1. Propagation Delay:

↳ Propagation delay time specification is the time required for output to change.

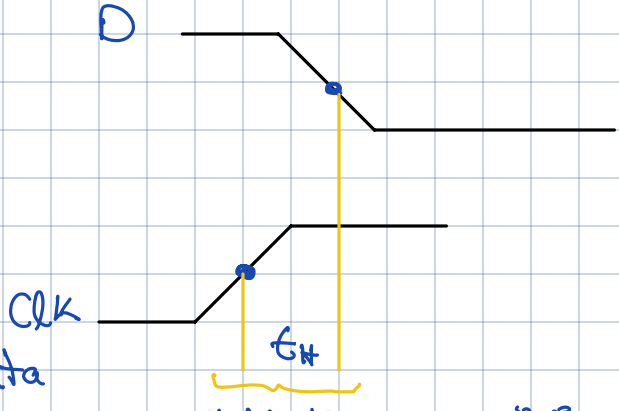
↳ It's measured from their 50% levels



Set & Hold time:



set time is minimum time for data to present before the clock

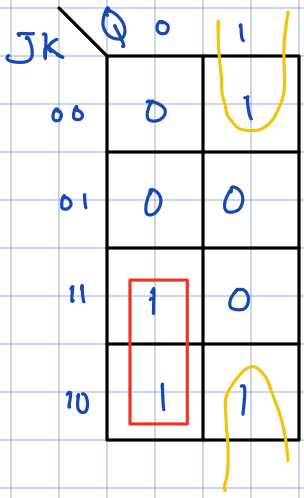


Hold time is minimum time for data to remain after the clock.

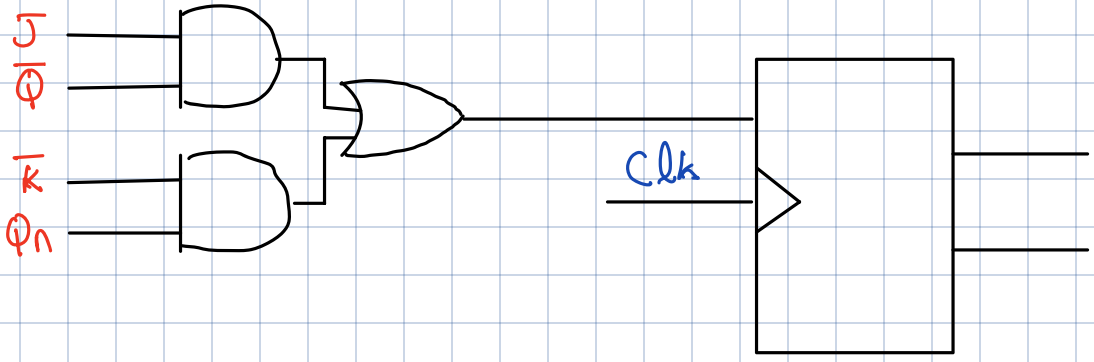
D to J-K flip flop:

Clk	J	k	Q	$\bar{Q}$	
0	X	X	Q	$\bar{Q}$	
↑	0	0	Q	$\bar{Q}$	
↑	0	1	0	1	RESET
↑	1	0	1	0	SET
↑	1	1	Toggle mode		

Clk	D	Q	$\bar{Q}$	
0	X	Q	$\bar{Q}$	
↑	0	0	1	RESET
↑	1	1	0	SET

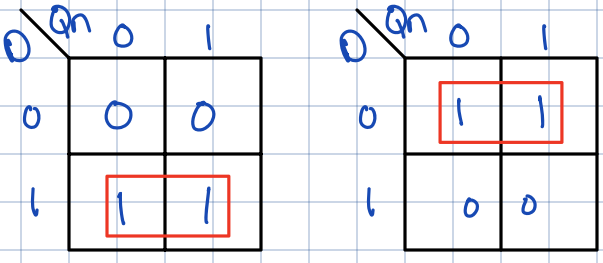


$Q_{n+1} = J\bar{Q}_n + \bar{k}Q_n$



J-K flip-flop to D

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1



$J = D$, $k = \bar{D}$