

Communication algorithms and principles for a prototype of a wireless mesh network

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Outline

1 Introduction

2 Hardware

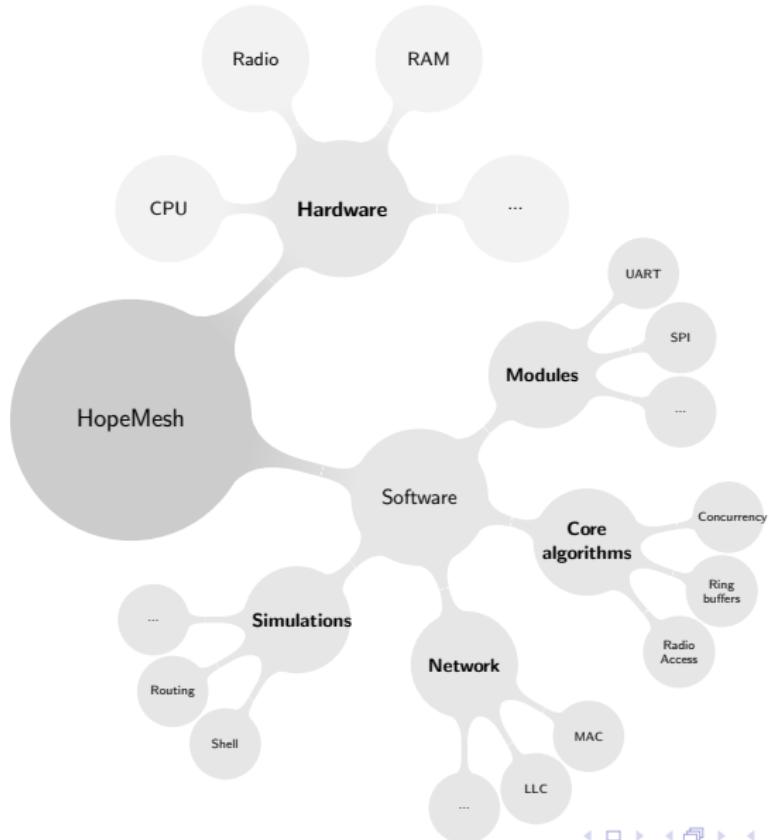
3 Software

Main Goal

Research and implement a fail-safe wireless mesh network prototype using embedded technologies.

- **Hardware:** Research and develop easily reproducible hardware design.
- **Software:** Research, analyze and implement enhanced concurrent algorithms.
- **Network:** Implement a pragmatic network stack and a B.A.T.M.A.N. based routing algorithm.
- **Simulation:** Make it possible to simulate algorithmic behaviour on x86 based PCs.

Project structure

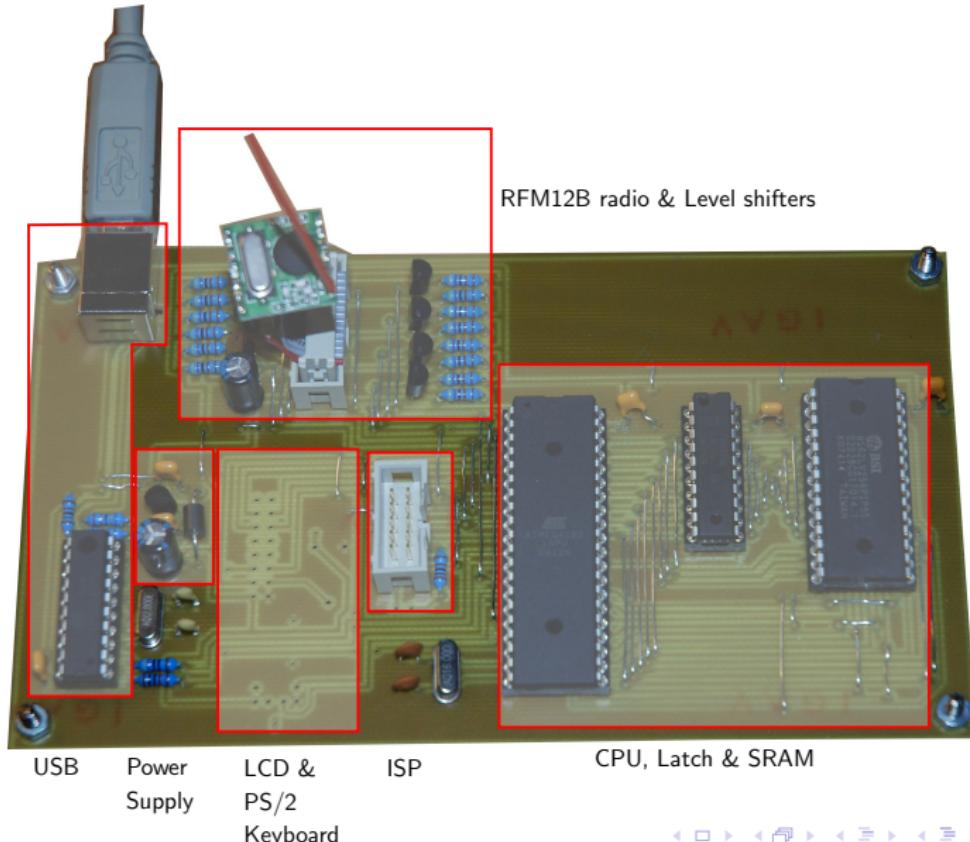


Hardware modules

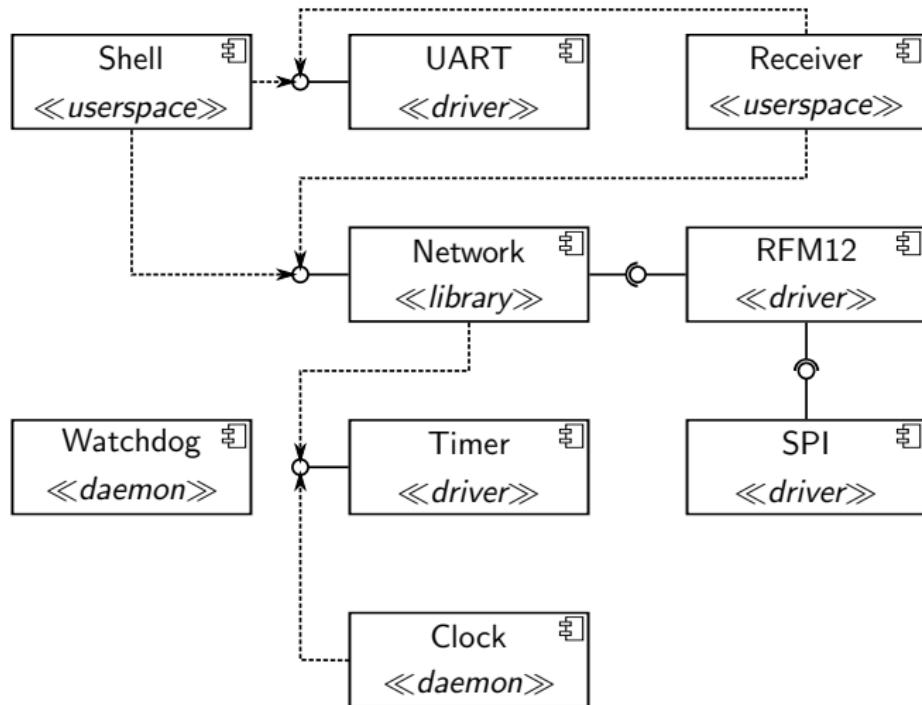
The goal was to use easily accessible embedded hardware parts:

- **CPU:** ATmega162: Includes the XMEM extension allowing to use external RAM natively.
- **RAM:** 62256 32kB SRAM: Connected to the CPU using a Latch.
- **Periphery:** USB connection to PC based terminal emulators, LCD and PS/2 keyboard connection.
- **Wireless connection:** RFM12B radio module from HOPERF.

PCB - Printed Circuit Board



Module Architecture



Concurrency Model

Concurrency models for embedded systems with an operating system:

Sequential Execution

Executes modules inside an infinite main loop starting from the first module until the last one. Once the last module ends the execution starts again from the first module.

Concurrent Execution

The main function only initializes and launches concurrent modules. Modules run in their own stack space and can execute individual main loops.

Petri net driver

