1. Show how to implement a JK flip-flop with a D flip-flop.

2. Show how to implement a D flip-flop with a T flip-flop.

3. Show how to implement a JK flip-flop with a T flip-flop.

4. Design a mod-6 counter, which counts in the following sequence: 0, 1, 2, 3, 4,
   5 and repeat. The counter counts if its enable input, w, is equal to 1, and does
   not count if w is equal to 0. If the counter, by accident, runs into an unused
   state (6 or 7), it should transition to state 0 with the next clock trigger to
   avoid being stuck in an unused state.

   A) Draw the state diagram and next state table.

   B) Implement this counter using D flip-flops.

5. Consider the design of a 4-bit BCD counter that counts in the following way:
   0000, 0001, 0010, 0011,…., 1001 and back to 0000.

   A) Draw the state diagram and next state table.

   B) Implement this counter using D flip-flops.

6. The 4-bit Johnson counter advances through the sequence: 0000, 1000, 1100,
   1110, 1111, 0111, 0011, 0001 and repeat.

   A) Implement this counter using D flip-flops.

   B) Implement this counter using T flip-flops.