Pass Transistors and Transmission Gates

The strength of a signal is measured by how closely it approximates an ideal voltage source.
In general, the stronger a signal, the more current it can source or sink.
An nMOS transistor is an almost perfect switch when passing a 0 and thus we say it passes a strong 0. However, the nMOS transistor is imperfect at passing a 1. The high voltage level is somewhat less than VDD.
A pMOS transistor again has the opposite behavior, passing strong 1s but degraded 0s. When an nMOS or pMOS is used alone as an imperfect switch, we sometimes call it a pass transistor.

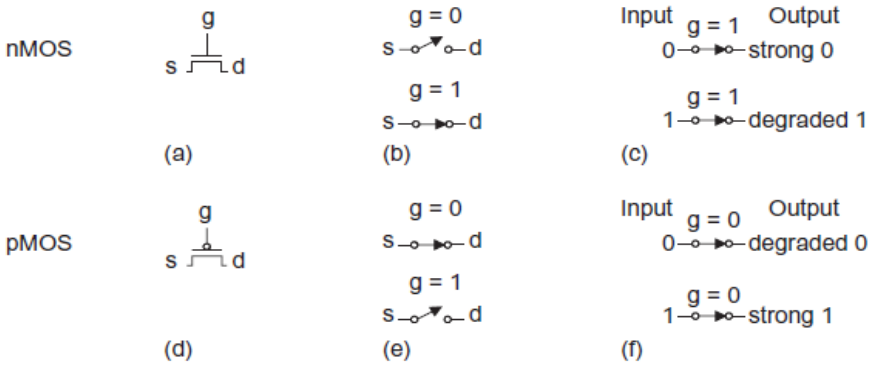


FIGURE 1.20 Pass transistor strong and degraded outputs

By combining an nMOS and a pMOS transistor in parallel (Figure 1.21(a)), we obtain a switch that turns on when a 1 is applied to g (Figure 1.21(b)) in which 0s and 1s are both passed in an acceptable fashion (Figure 1.21(c)). We term this a transmission gate or pass gate.

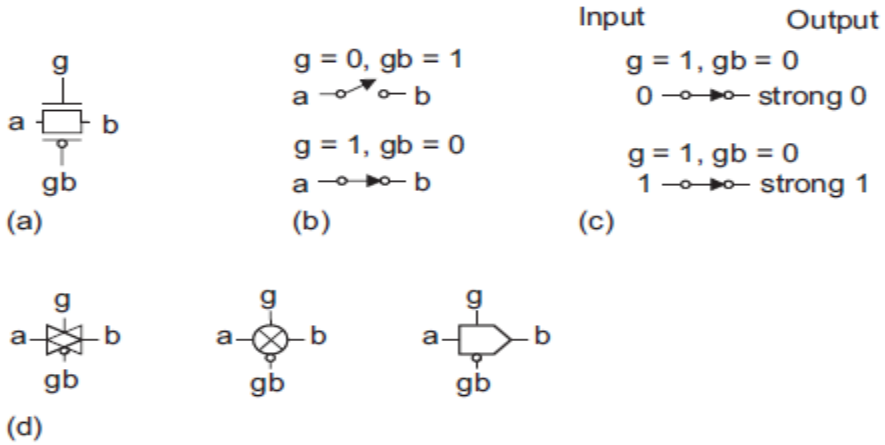
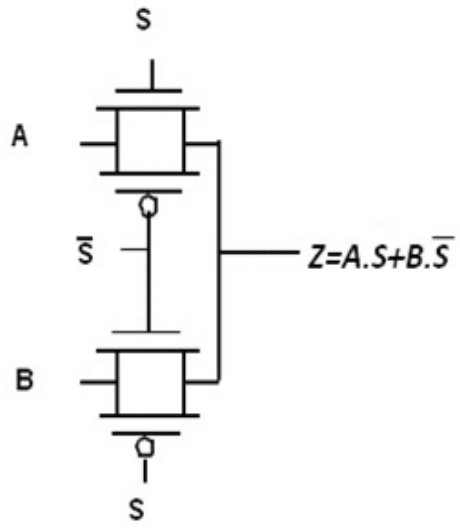


FIGURE 1.21 Transmission gate

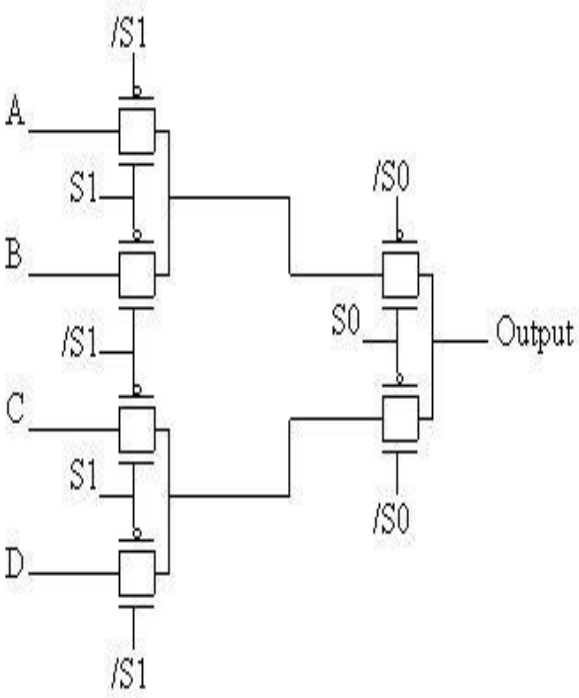
Some logic design using Transmission Gates

- **2:1 Multiplexer**



When S=0, $\overline{S}$ = 1, then, PMOS and NMOS of B will be ON and Z= A.0 + B.1=B

When S=1, $\overline{S}$ = 0, then, PMOS and NMOS of A will be ON and Z= A.1 + B.0=A



When S1=0, /S1=1, B and D turns ON, and, When S0=0, /S0=1, D is selected and appears at the output.

When S1=1, /S1=0, A and C turns ON, and, When S0=0, /S0=1, C is selected and appears at the output.

When S1=0, /S1=1, B and D turns ON, and, When S0=1, /S0=0, B is selected and appears at the output.

When S1=1, /S1=0, A and C turns ON, and, When S0=1, /S0=0, A is selected and appears at the output.

Latches

A D-latch built from a 2-input multiplexer and two inverters is shown in Figure 1.31(a). The multiplexer can be built from a pair of transmission gates, shown in Figure 1.31(b), because the inverters are restoring. This latch also produces a complementary output, Q. When CLK = 1, the latch is transparent and D flows through to Q (Figure 1.31(c)). When CLK falls to 0, the latch becomes opaque. A feedback path around the inverter pair is established (Figure 1.31(d)) to hold the current state of Q indefinitely. The D latch is also known as a level-sensitive latch because the state of the output is dependent on the level of the clock signal, as shown in Figure 1.31(e). The latch shown is a positive-level-sensitive latch, represented by the symbol in Figure 1.31(f). By inverting the control connections to the multiplexer, the latch becomes negative-level-sensitive.

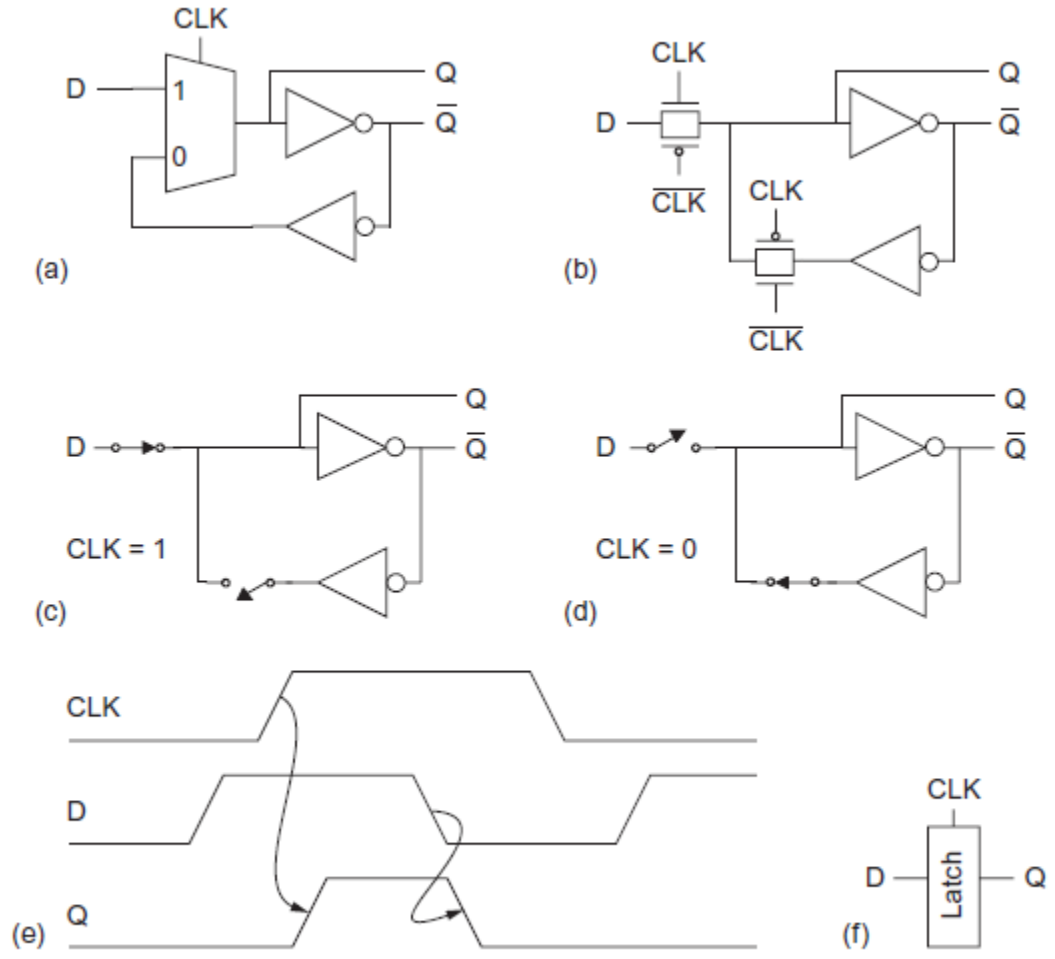


FIGURE 1.31 CMOS positive-level-sensitive *D* latch