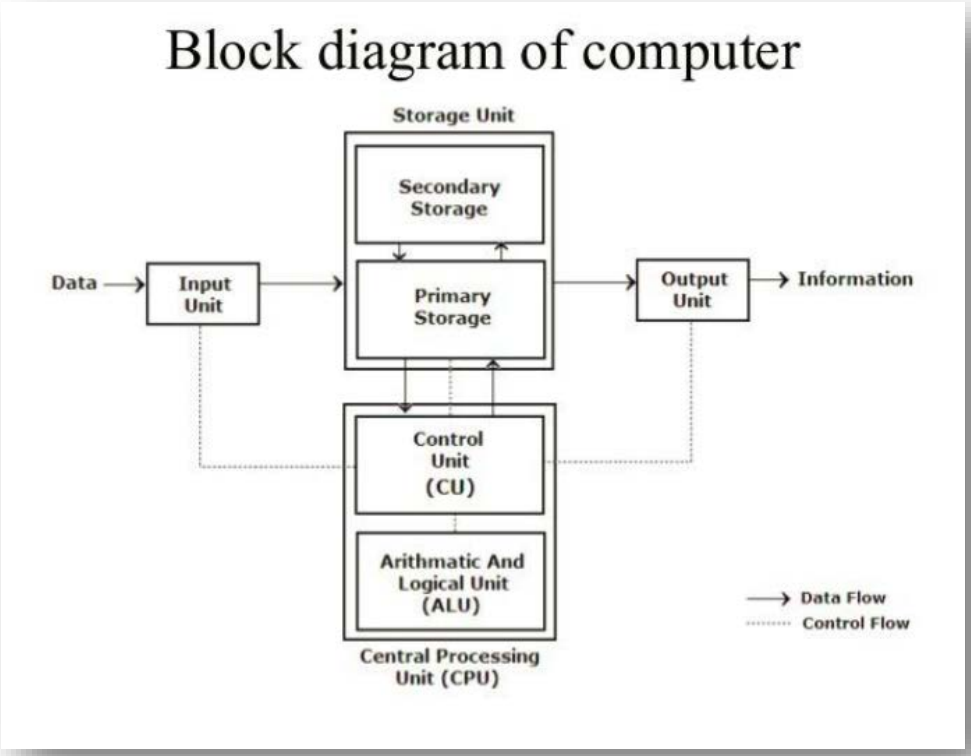
Describe the Digital Computer architecture?

The digital computer is a digital framework that performs different computational assignments. The word digital infers that the data in the computer is addressed by factors that take a set number of discrete qualities. These qualities are prepared inside by parts that can keep a set number of discrete states. The decimal digits 0, 1, 2, ..., 9, for instance, give 10 discrete qualities. The principal electronic digital computer, created in the last part of the 1940s, was utilized essentially for mathematical calculations and the discrete components were the digits. From this application the term digital computer arose. Practically speaking, digital computers work all the more dependably if just two states are utilized. In view of the actual limitation of parts, and on the grounds that human rationale will in general be paired (i.e., valid or bogus, yes or no assertions), digital segments that are obliged to take discrete qualities are additionally compelled to take just two qualities and are supposed to be parallel. Digital computers utilize the double number framework, which has two digits: 0 and 1. A twofold digit is known as a piece. Data is addressed in digital computers in gatherings of pieces. By utilizing different coding methods, gatherings of pieces can be made to address paired numbers as well as other discrete

images, like decimal digits or letters of the letters in order.



Computer Architecture:

Computer Architecture is worried about the design and conduct of the computer as seen by the client. It incorporates the data, arranges, the guidance set, and procedures for tending

to memory. The compositional plan of a computer framework is worried about the details of the different useful modules, like processors and recollections, and organizing them together into a computer framework.

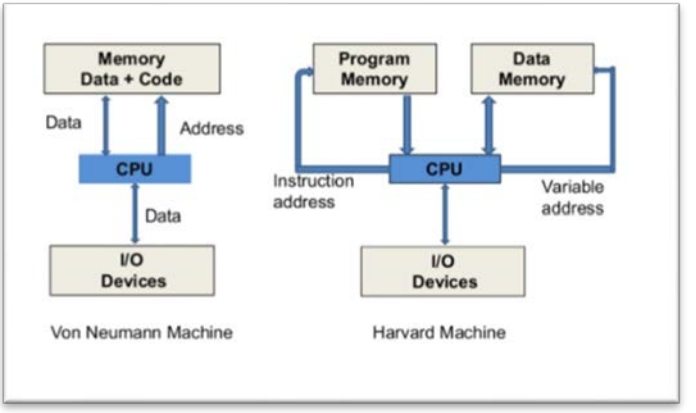
Two types of computer architecture are:

1. ***von Neumann architecture:***

The Von Neumann architecture comprises of three particular segments: a central processing unit (CPU), memory unit, and info/yield (I/O) interfaces. The CPU is the core of the PC framework that comprises of three principal segments: the Arithmetic and Logic Unit (ALU), the control unit (CU), and registers.

2. ***Harvard architecture:***

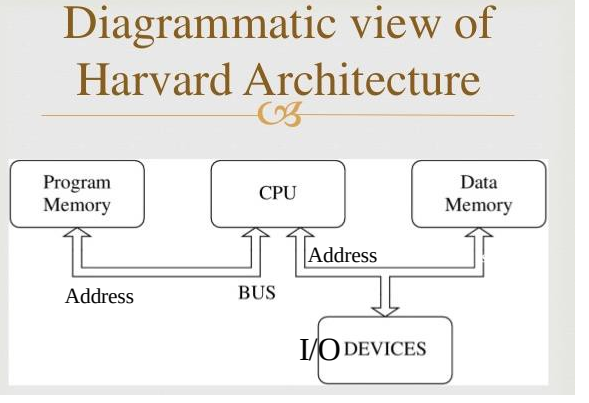
It's anything but a PC architecture with actually separate stockpiling and sign pathways for program information and guidelines. Not at all like Von



Neumann architecture which utilizes a solitary transport to both get directions from memory and move information starting with one piece of a PC then onto the next, Harvard architecture has separate memory space for information and guidance.

Types of Harvard Computer Architecture?

Harvard architecture is a sort of PC architecture that isolates its memory into two sections so information and guidelines are put away independently. The architecture additionally has separate transports for information moves and guidance gets. This permits the CPU to bring information and directions simultaneously.



Today, processors utilizing Harvard architecture utilize an adjusted structure so they can accomplish a more noteworthy exhibition. Some adjusted structures permit

the help of errands like stacking a program from optional capacity (went against to RAM) as information then, at that point executing it. In certain frameworks, guidelines are put away in read-just memory and information in read-compose memory.

This architecture is at times utilized inside the CPU to deal with its stores, yet it is less utilized with fundamental memory in light of intricacy and cost. It is utilized broadly with installed Digital Signal Processing (DSP) frameworks. DSP frameworks incorporate sound and discourse signal handling, sonar and radar signal preparing machines, biomedical sign preparing, seismic information preparing and advanced picture preparing. Implanted frameworks incorporate particular reason gadgets incorporated into gadgets frequently working progressively, like those utilized in route frameworks, traffic signals, airplane control frameworks and test systems.

Harvard architecture can be quicker than Von Neumann architecture since information and directions can be gotten in equal as opposed to contending on a similar bus.

Von Neumann architecture defined by:

A standard plan of PC framework (delivered 1945-51) in which there is a control unit, arithmetic logic unit (ALU), a memory unit (all inside CPU) and input/output

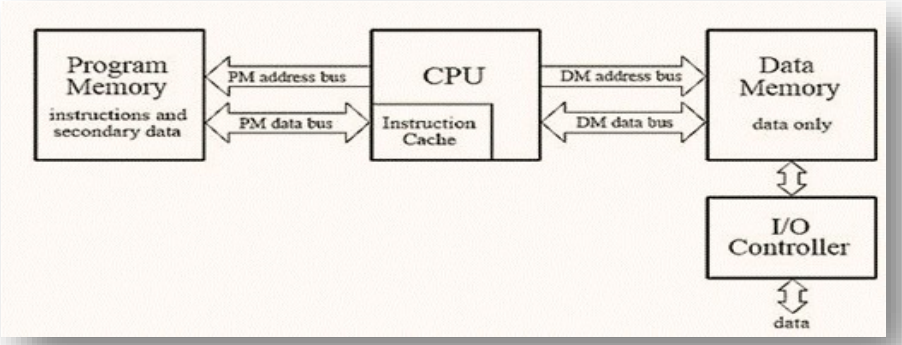
gadgets. These elements are associated over a progression of busses.

- There is just a single information transport which is utilized for both guidance gets and information move from the memory which likewise is utilized for capacity of the two directions and information.
- Data/directions can pass down the middle duplex (planned/each in turn) mode from to and from CPU
- Also called stored program concept.
- The memory is addressed linearly; that is, there is a single sequential numerical address for each memory location.
- Memory is split into small cells of equal sizes each with address numbers (i.e. same word size used for all memory).

  Program guidelines are executed as per the pattern in which where they show up in the memory, the arrangement of directions must be changed by genuine/restrictive leap guidelines.

  All instructions/data is in binary form.

Diagrammatic representation of Harvard Architecture:



Difference between Von Neumann and Harvard Architecture?

The Von Neumann architecture is a hypothetical PC configuration dependent on the idea of put away program where projects and information are put away in a similar memory. The idea was planned by a mathematician John Von Neumann in 1945 and which by and by fills in as the premise of practically all cutting edge PCs. The Harvard architecture depended on the first Harvard Mark I transfer based PC model which utilized separate busses for information and guidelines.

VON NEUMANN ARCHITECTURE	HARVARD ARCHITECTURE
It is old PC architecture dependent on put away program PC idea.	*It is current PC architecture dependent on Harvard Mark I hand-off-based model.*
Same actual memory address is utilized for guidelines and information.	*Separate actual memory address is utilized for directions and information.*
There is normal bus for information and guidance move.	*Separate busses are utilized for moving information and guidance.*
Two clock cycles are needed to execute single guidance.	*A guidance is executed in a solitary cycle.*
It is less expensive in cost.	*It is expensive than van Neumann architecture.*
Central processor can't get to guidelines and read/compose simultaneously.	*Computer processor can get to directions and read/compose simultaneously.*
It is utilized in PCs and little PCs.	*It is utilized in miniature regulators and sign preparing.*