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Assignment # 02 Lectures Summary

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Lecture # 09* Boolean addition:-

Boolean addition is equivalent to the OR logic function, as well as parallel switch contacts - Boolean algebra is the expressing defining Boolean addition is a term which is the sum of literals.

$$A+B, A+B, \overline{A}+\overline{B}+\overline{C}$$

- * A Sum term is 1 when any one literal is 1.
- * A Sum term is 0 when all literals are 0.

* Boolean Multiplication-

Boolean multiplication is performed by our AND gate. In Boolean algebra expression defining Boolean Multiplication is a product term which is the product of literals.

$$A \cdot B, A \cdot \overline{B}, A \cdot \overline{B} \cdot C$$

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- * A Product term 1 when all literals terms are 1 -
- * A Product term 0 when all literals terms are 0 -

* Commutative Law:-

The Commutative law of addition States that if two numbers are added then the result is equal to the addition of the interchange Position -

$$A+B = B+A$$

In this law of multiplication States that 2 numbers stay the same, even if the positions of the numbers are interchanged -

$$A \cdot B = B \cdot A$$

* Associative Law:-

The associative laws State that you add or multiply any three real numbers, the grouping of the numbers does not affect the result -

The Associative law of addition :-

$$(a+b)+c = a+(b+c).$$

The Associative law of Multiplication :-

$$(ab)c = a(bc)$$

Continued to next Pg

* Distributive Law :-

This law is completely different from Commutative and associative law. According to this law, if A, B and C are three real numbers, then ;

$$A(B+C) = A \cdot B + A \cdot C$$

Lecture # 10

* Rules of Boolean Algebra :-

To convert a gate Circuit to a boolean expression, label each gate output with a Boolean Sub-expression corresponding to the gates input signals, until a final expression is reached at the last gate.

Below is an example boolean expression. In fact, it represents the same logic as the example logic Circuit diagram above. This concept will also become clearer when we cover converting from and to the boolean expression below.

$$Y = (\overline{AB}) \overline{BC}$$

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* De Morgan's Theorem :-

These are two de Morgan's rules or theorems.

1) Two Separate terms NOR'ed together is the same as the two terms inverted (complement) and AND'ed for example : $\overline{A+B} = \overline{A} \cdot \overline{B}$

2) Two Separate terms NAND'ed together is the same as the two terms inverted (complement) and OR'ed. for example : $\overline{A \cdot B} = \overline{A} + \overline{B}$

* Boolean Analysis of logic Circuit :-

By writing the expression for each gate and combining the expressions according to the rule for Boolean algebra, Combinational logic Circuits can be analyzed.

Lecture # 11

In Such lecture we have been learn about boolean algebra
in detail.

Introduction:-

George Boole who was the 19th Century English mathematician was develop logical Algebra System. That System are now called "Boolean Algebra".

* Logical Addition:-

The logic of boolean expression given for a logic OR gate is that for logical addition which is denoted by a plus Sign (+).

* Logical Multiplication:-

This expression given for a digital's logic AND gate is that for logical multiplication which is denoted by a Single dot or full Stop symbol (.)

Continued to next Pg.

* OR Gate :-

The OR gate is an electronic circuit that gives a high output 1 if one or more of its inputs are high.

* NOT Gate :-

The NOT gate is an electronic circuit that produces an inverted version of the input at its output. It is also known as an inverter.

* AND Gate :-

The AND gate is an electronic circuit that gives a high output 1 only if all its inputs are high.

* NAND Gate :-

This is NOT-AND gate which is equal to an AND gate followed by a NOT gate. The outputs of all NAND gates are high if any of the inputs are low.

* NOR Gate :-

This is a NOT-OR gate which is equal to an OR gate followed by a NOT gate. The outputs of all NOR gates are low if any of the inputs are high.

Continued to next Pg.

* Sum of Product (Minterm) :-

It means that the product of variables which are separated by "+" sign. e.g ;
 $XY + X\bar{Y} + \bar{X}Y + \bar{X}\bar{Y} + X\bar{Y}\bar{Z} + X\bar{Y}Z + X\bar{Y}Z$

* Product of Sum :-

It means that the variables are separated by the sign of multiplication e.g ;
 $(X+Y)(\bar{X}+Y)(X+\bar{Y})(\bar{X}+\bar{Y})(X+\bar{Y})(X+\bar{Y}+Z)$
 $(X+\bar{Y}+Z)(X+\bar{Y}+Z)$.

* Boolean Expressions :-

It is generally used to describe the logical behaviour of Circuits. By Using truth-table and Boolean expression -

* Redundant Groups:-

After you finish ^{un}Circling group there is one more thing to do before writing Simplified Boolean expressions eliminated one group whose 1's are completely overlapped by another group.

Lecture # 12

* Sum of Products :-

The Sum of Product (SOP) expression comes from the fact that two or more products (AND) are summed (OR) together. That is the outputs from two or more AND gates are connected to the input of an OR gate so that they are effectively OR'ed together to create the final AND-OR logical output.

* Product of Sums :-

The Product of Sum (POS) expressions are Boolean expression made up of sums consisting of one or more variables either in its normal true form or complemented form or combination of both, which are then AND'ed together.

* Standard SOP & POS form :-

Special cases of SOP & POS.

The Canonical forms are

Continued to next Pg.

* Canonical Form :-

Canonical SOP form means Canonical Sum of Product form. In this form, each product term contains all literals. So, these product terms are nothing but the minterms. Hence, Canonical SOP form is also called as Sum of minterms.

form

* Max Term :-

A max term is a boolean expression resulting in a 0 for the output of a single cell expression, and 1's for all other cells in the Karnaugh map, or truth-table. The maxterm is a 0, not a 1 in the Karnaugh map. The maxterm is a sum term, ($A+B+C$) in our example, not a product term.

* Min Term :-

A min term is a Boolean expression resulting in 1 for the output of a single cell, and 0's for all cells in a Karnaugh map, or truth-table. If a minterm has a single 1 and the remaining cells as 0's, it would appear to cover a minimum area of 1's.

Lecture # 13

* Karnaugh Map :-

A Karnaugh map (K-map) is a pictorial method used to minimize Boolean expressions without having to use Boolean algebra theorems and equation manipulations.

A K-map can be thought of as a special version of a truth-table. Using a K-map expressions with two or four variables are easily minimized.

* Karnaugh Map Rules :-

- 1) Groups may not include any cell containing a zero.
- 2) Groups may be horizontal or vertical, but not diagonal.
- 3) Groups must be contain $1, 2, 4, 8$ or in general 2^k cells.
- 4) Each group should be as large as possible.
- 5) Each cell containing a one must be in at least one group.
- 6) Groups may overlap.
- 7) Groups may wrap around the table.

Continued to next Pg

$AB \backslash CD$	00	01	11	10
00	0	4	12	8
01	1	3	13	9
11	3	7	15	11
10	2	6	14	10

$AB \backslash CD$	00	01	11	10
00	1	0	1	1
01	0	0	1	0
11	0	1	1	0
10	1	1	1	1

Lecture # 14

Q No 1: $F(A, B, C, D) = \Sigma(4, 6, 7, 15)$

Solve

$$F(A, B, C, D) = \Sigma(4, 6, 7, 15)$$

$$\text{So, } \therefore (A^5 B^4 C^3 D^2)$$

$$F(A, B, C, D) = \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}B\bar{C}D + ABCD$$

So, Now;

Continued to next Pg

$AB \backslash CD$	$\bar{C}\bar{D}$	$\bar{C}D$	$\bar{C}\bar{D}$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	$\bar{A}\bar{B}\bar{C}\bar{D}$	$\bar{A}\bar{B}\bar{C}D$	$\bar{A}\bar{B}C\bar{D}$	$\bar{A}\bar{B}CD$	$\bar{A}\bar{B}C\bar{D}$
$\bar{A}B$	$\bar{A}B\bar{C}\bar{D}$	$\bar{A}B\bar{C}D$	$\bar{A}BC\bar{D}$	$\bar{A}BCD$	$\bar{A}B\bar{C}\bar{D}$
$A\bar{B}$	$AB\bar{C}\bar{D}$	$AB\bar{C}D$	$ABC\bar{D}$	$ABCD$	$ABC\bar{D}$
$A\bar{B}$	$A\bar{B}\bar{C}\bar{D}$	$A\bar{B}\bar{C}D$	$A\bar{B}C\bar{D}$	$A\bar{B}CD$	$A\bar{B}\bar{C}\bar{D}$

$AB \backslash CD$	$\bar{C}\bar{D}$	$\bar{C}D$	$\bar{C}\bar{D}$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	1	3	2	
$\bar{A}B$	4	5	7	6	
$A\bar{B}$	12	13	15	14	
$A\bar{B}$	8	9	11	10	

$AB \backslash CD$	$\bar{C}\bar{D}$	$\bar{C}D$	$\bar{C}\bar{D}$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0000	0001	0011	0010	
$\bar{A}B$	0100	0101	0111	0110	
$A\bar{B}$	1100	1101	1111	1110	
$A\bar{B}$	1000	1001	1011	1010	

$AB \backslash CD$	$\bar{C}\bar{D}$	$\bar{C}D$	$\bar{C}\bar{D}$	CD	$C\bar{D}$
$\bar{A}\bar{B}$					
$\bar{A}B$	1			1	1
$A\bar{B}$					
$A\bar{B}$				1	

So here;

$$(\bar{A}\bar{B}\bar{C}\bar{D})(\bar{A}B\bar{C}\bar{D})$$

So,

$$\bar{A}\bar{B}\bar{D}$$

1st Pair,

$$\boxed{\bar{A}\bar{B}\bar{D}}$$

2nd Pair,

$$(\bar{A}\bar{B}\bar{C}\bar{D}) \cdot (\bar{A}B\bar{C}\bar{D})$$

$$\boxed{\bar{B}\bar{C}\bar{D}}$$

Ans

$$\therefore \bar{A} \cdot \bar{A} = A$$

$$\therefore B \cdot B = 1$$

$$\therefore C \cdot C = C$$

$$\therefore A \cdot A = A$$

$$\therefore D \cdot D = D$$

$$\therefore D \cdot D = 1$$

$$\therefore D \cdot D = D$$

* Find the minimized SOP expression against the following.

$$1) F(A, B, C) = \Sigma(0, 2, 6, 7)$$

Sol:-

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
\bar{A}	$\bar{A}\bar{B}\bar{C}$	$\bar{A}\bar{B}C$	$\bar{A}BC$	$\bar{A}B\bar{C}$
A	$A\bar{B}\bar{C}$	$A\bar{B}C$	ABC	$A\bar{B}\bar{C}$

	00	01	11	10
0	1	0	0	1
1	0	0	1	1

Continued to next Pg
C

$$\begin{array}{c|c}
 \begin{array}{c} \bar{A} \\ \bar{B} \\ \bar{C} \\ \hline \bar{A} \bar{C} \end{array} & \begin{array}{c} AB\bar{C} \\ AB\bar{C} \\ \hline AB \end{array}
 \end{array}$$

$$\boxed{\bar{A}\bar{C} + AB} \text{ aus}$$

2) $F(A, B, C) = \Sigma(0, 2, 3, 4, 6)$

\bar{A}	$\bar{A}\bar{B}\bar{C}$	$\bar{A}\bar{B}C$	$\bar{A}BC$	$\bar{A}B\bar{C}$
A	$A\bar{B}\bar{C}$	$A\bar{B}C$	ABC	$A\bar{B}\bar{C}$

	00	01	11	10
0	0	0	1	1
1	1	0	0	1

$$\begin{array}{c|c}
 \begin{array}{c} \bar{A}\bar{B}\bar{C} \\ A\bar{B}\bar{C} \\ A\bar{B}C \\ \bar{A}B\bar{C} \\ \hline \bar{C} \end{array} & \begin{array}{c} \bar{A}\bar{B}\bar{C} \\ \bar{A}\bar{B}C \\ \hline \bar{A}B \end{array}
 \end{array}$$

$$\boxed{AB + C} \text{ aus}$$

Lecture # 15

Multiplexer :-

A multiplexer is a circuit used to select and route any one of the several input signals to a signal output. A simple example of an non electronic circuit of a multiplexer is a single pole multi position switch.

Demultiplexer :-

A demultiplexer is a device that takes a single input line and routes it to one of several digital output lines. A demultiplexer of 2^n outputs has n select lines, which are used to select which output line to send the input.

Parity Generator:-

A parity generator is a combinational logic circuit that generates the parity bit in the transmitter. On the other hand, a circuit that checks the parity in the receiver is called parity checker.

Encoder :-

An encoder in digital electronics is a one-to-

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to binary Converter if there are 2^n input lines, and at most only one of them will ever be high, The binary code of this 'hot' line is produced on the n bit output lines. A binary encoder is the dual of a binary decoder -

Decoder :-

Decoder is a Combinational Circuit that has n input lines and maximum of 2^n output lines. One of these output will be active high based on the combination of inputs present, when the decoder is enabled. That means decoder detects a particular code -

Half Adder :-

Half adder is a combinational arithmetic circuit that adds 2 numbers and produces a sum bit (S) and carry bit (C) as the output. If A & B are the inputs bits, then sum bit (S) is the X-or of A and B and the carry bit (C) will be the AND of A and B -

Full Adder :-

A full adder circuit is central to most digital

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Circuits that Perform addition or Subtraction. It is So called it adds together two binary digits, plus a Carry in digits to produce a Sum and Carry-out digit -

Parallel Adder:-

A Parallel adder is a digital circuit capable of finding the arithmetic sum of 2 binary numbers that is greater the one bit in length by operating on corresponding pairs of bits in parallel.

X X X