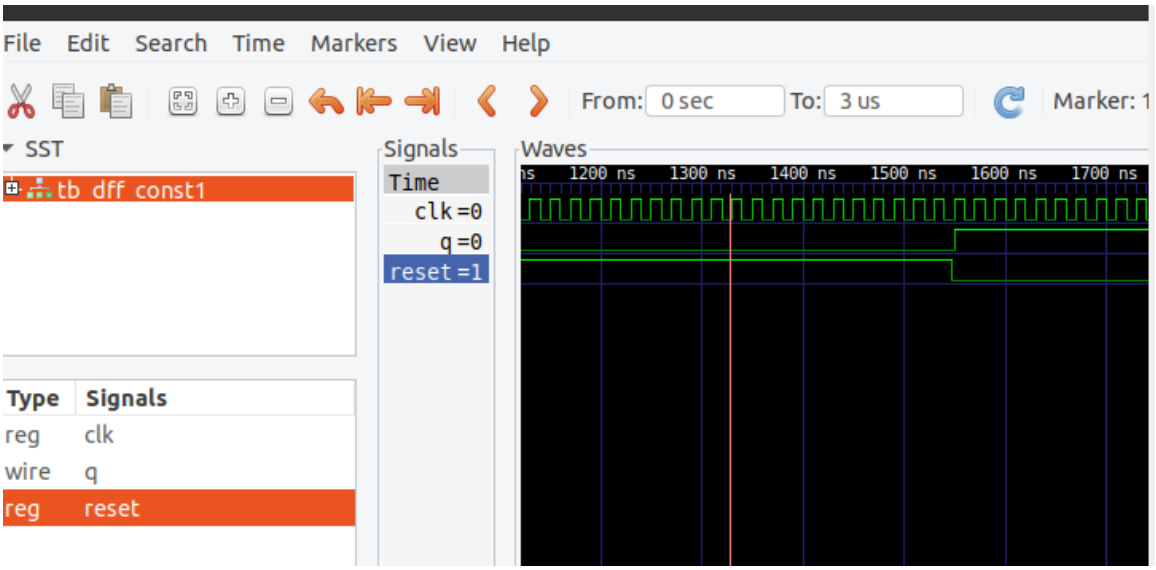
Lab5

```
root@raheem:/home/raheem/week1/sky130RTLDesignAndSynthesisWorkshop-main/verilog
_files# iverilog dff_
dff_ares.net.v          dff_async_set.v         dff_const4.v
dff_asyncres_net.v      dff_const1.v            dff_const5.v
dff_asyncres_syncres.v  dff_const2.v            dff_net.v
dff_asyncres.v          dff_const3.v            dff_syncres.v
root@raheem:/home/raheem/week1/sky130RTLDesignAndSynthesisWorkshop-main/verilog
_files# iverilog dff_const1.v tb_dff_const1.v
root@raheem:/home/raheem/week1/sky130RTLDesignAndSynthesisWorkshop-main/verilog
_files# ./a.out
VCD info: dumpfile tb_dff_const1.vcd opened for output.
root@raheem:/home/raheem/week1/sky130RTLDesignAndSynthesisWorkshop-main/verilog
_files# gtkwave tb_dff_const2.v
```



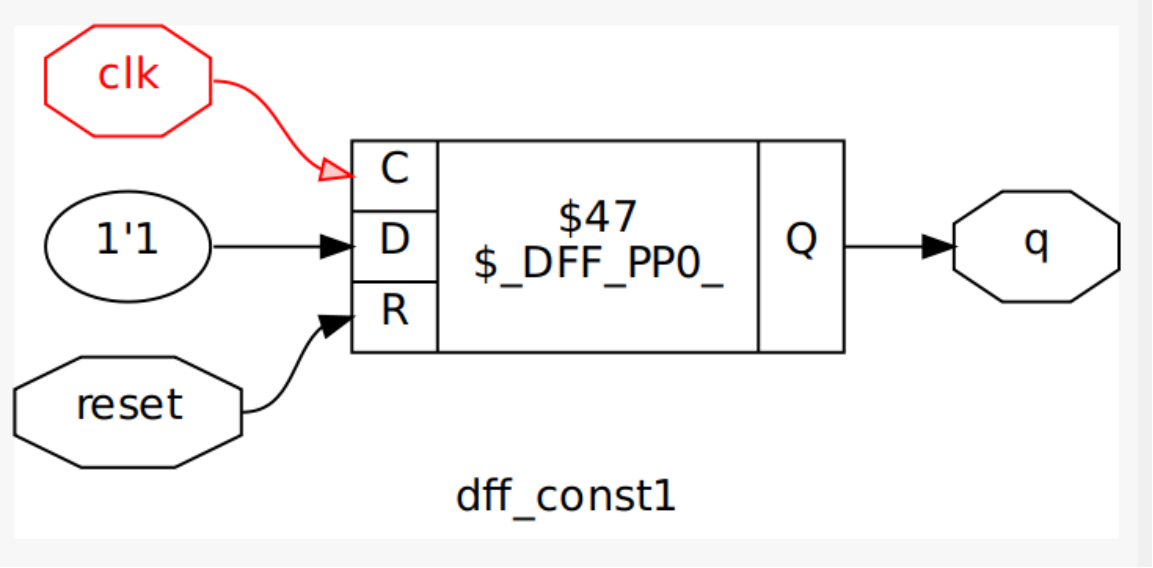
```
3.25.2. Analyzing design hierarchy..
Top module:  \dff_const1
Removed 0 unused modules.

3.26. Printing statistics.

=== dff_const1 ===

   Number of wires:                 3
   Number of wire bits:             3
   Number of public wires:          3
   Number of public wire bits:      3
   Number of memories:              0
   Number of memory bits:           0
   Number of processes:             0
   Number of cells:                 1
     $_DFF_PP0_                     1

3.27. Executing CHECK pass (checking for obvious problems).
checking module dff_const1..
found and reported 0 problems.
```



```
ABC: + &put
ABC: + write_blif <abc-temp-dir>/output.blif

7.1.2. Re-integrating ABC results.
ABC RESULTS:   sky130_fd_sc_hd__clkinv_1 cells:        1
ABC RESULTS:        internal signals:        0
ABC RESULTS:           input signals:        1
ABC RESULTS:          output signals:        1
Removing temp directory.

yosys>
```