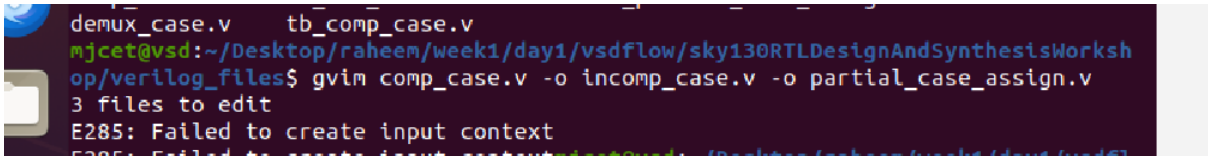
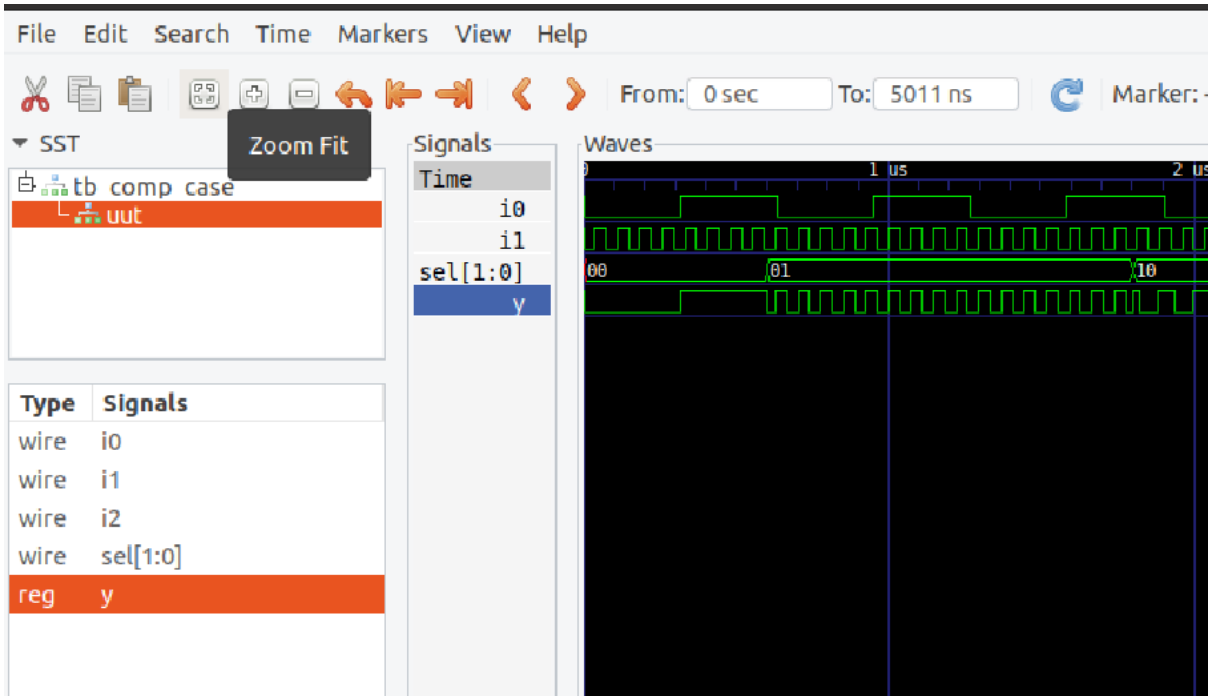
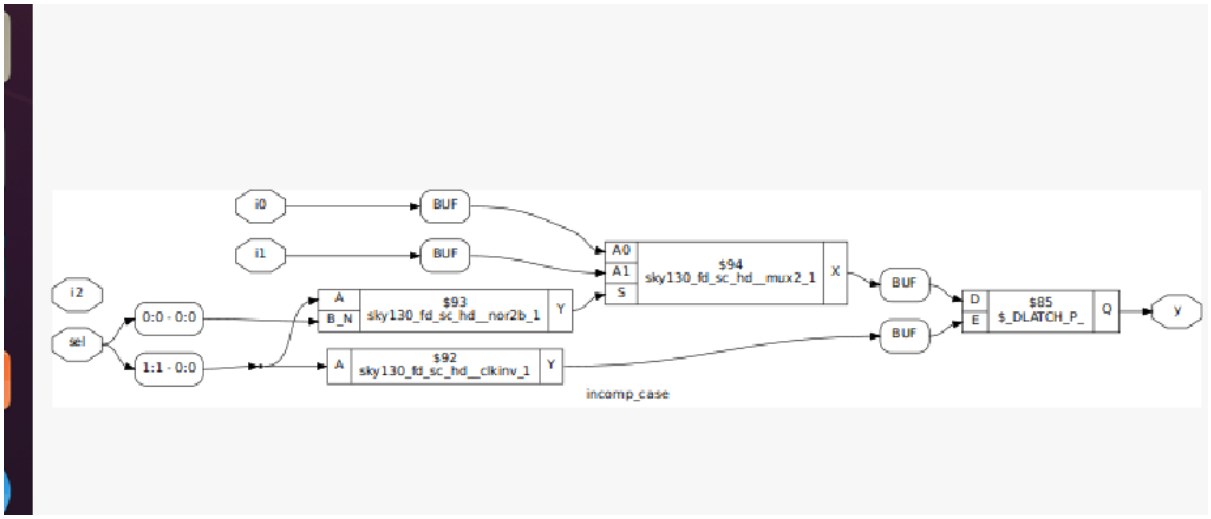
Incomplete Overlapping Case Examples




```
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# iverilog comp_case.v incomp_case.v
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# ./a.out
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# iverilog comp_case.v tb_comp_case.v
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# ./a.out
VCD info: dumpfile tb_comp_case.vcd opened for output.
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# gtkwave tb_comp_case.vcd
Gtk-Message: 19:32:01.711: Failed to load module "canberra-gtk-module"

GTKWave Analyzer v3.3.103 (w)1999-2019 BSI
```



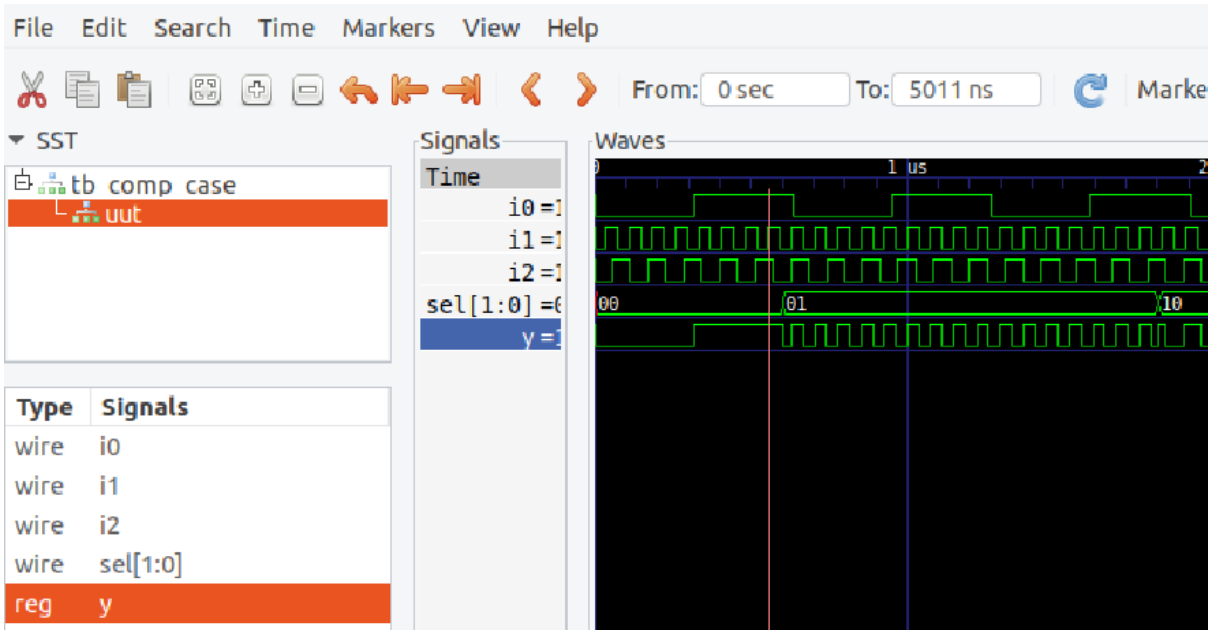

```
 Yosys 0.9 (git sha1 1979e0b)


yosys> read_verilog incomp_case.v
1. Executing Verilog-2005 frontend: incomp_case.v
Parsing Verilog input from `incomp_case.v' to AST representation.
Generating RTLIL representation for module `\incomp_case'.
Successfully finished Verilog frontend.

yosys> read_liberty -lib ../lib/sky130_fd_sc_hd__tt_025C_1v80.lib

2. Executing Liberty frontend.
Imported 418 cell types from liberty file.

yosys> synth -top incomp_case

3. Executing SYNTH pass.
```


i0
i1
i2
sel
0:0 - 0:0
1:1 - 0:0
BUF
BUF
A
B_N
$93
sky130_fd_sc_hd__nor2b_1
Y
A
$92
sky130_fd_sc_hd__clkinv_1
Y
A0
A1
S
$94
sky130_fd_sc_hd__mux2_1
X
BUF
BUF
D
E
$85
$_DLATCH_P_
Q
y
incomp_case

Comp_case.v

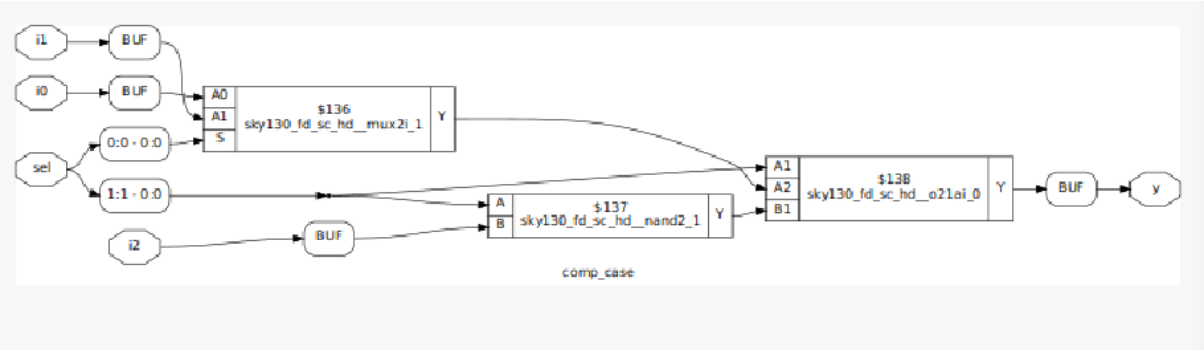
```
2
3 module comp_case (input i0 , input i1 , input i2 , input [1:0] sel, output
  reg y);
4 always @ (*)
5 begin
6         case(sel)
7                 2'b00 : y = i0;
8                 2'b01 : y = i1;
9                 default : y = i2;
10        endcase
11 end
12 endmodule
```

```
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# iverilog comp_case.v tb_comp_case.v
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# ./a.out
VCD info: dumpfile tb_comp_case.vcd opened for output.
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# gtkwave tb_comp_case.v
Gtk-Message: 20:19:50.930: Failed to load module "canberra-gtk-module"

GTKWave Analyzer v3.3.103 (w)1999-2019 BSI


(gtkwave:2695): dconf-WARNING **: 20:19:50.969: failed to commit changes to dco
nf: The connection is closed
Near byte 20, VCD search table NULL..is this a VCD file?
Near byte 20, Unknown VCD identifier: 'ns'
No symbols in VCD file..is it malformed?  Exiting!
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# gtkwave tb_comp_case.vcd
Gtk-Message: 20:20:04.348: Failed to load module "canberra-gtk-module"

GTKWave Analyzer v3.3.103 (w)1999-2019 BSI
```



```
3.26. Printing statistics.

=== incomp_case ===

   Number of wires:                  9
   Number of wire bits:             10
   Number of public wires:           5
   Number of public wire bits:       6
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                  5
     $_ANDNOT_                       1
     $_DLATCH_P_                     1
     $_MUX_                          1
     $_NOR_                          1
     $_OR_                           1

3.27. Executing CHECK pass (checking for obvious problems).
checking module incomp_case..
found and reported 0 problems.
```

```
ABC: + &put
ABC: + write_blif <abc-temp-dir>/output.blif

6.1.2. Re-integrating ABC results.
ABC RESULTS:   sky130_fd_sc_hd__mux2i_1 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__nand2_1 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__o21ai_0 cells:        1
ABC RESULTS:        internal signals:        6
ABC RESULTS:           input signals:        5
ABC RESULTS:          output signals:        1
Removing temp directory.
```

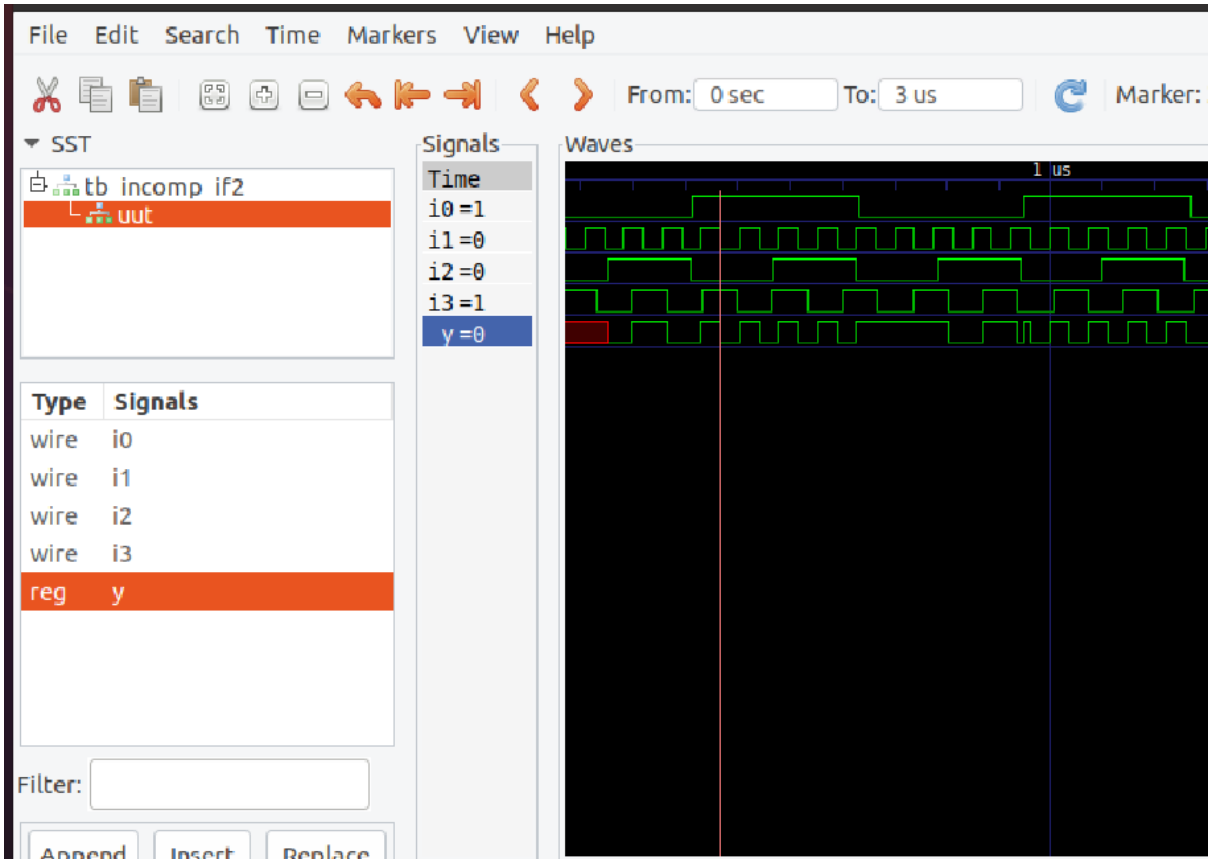


Compilation and Simulation

Incomp_if2.v tb_incomp_if2.v

```
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# ./a.out
VCD info: dumpfile tb_incomp_if2.vcd opened for output.
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# gtkwave tb_incomp_
tb_incomp_case.v   tb_incomp_if2.v    tb_incomp_if2.vcd  tb_incomp_if.v
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# gtkwave tb_incomp_
tb_incomp_case.v   tb_incomp_if2.v    tb_incomp_if2.vcd  tb_incomp_if.v
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# gtkwave tb_incomp_if2.vcd
Gtk-Message: 09:30:58.169: Failed to load module "canberra-gtk-module"

GTKWave Analyzer v3.3.103 (w)1999-2019 BSI
```

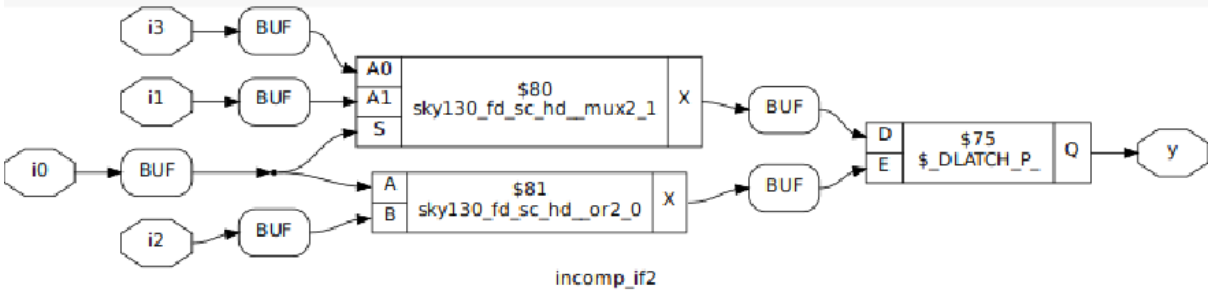
Incomp_if2.vcd Simualtion



Synthesis income_if2

```
yosys> read_verilog incomp_if2.v
1. Executing Verilog-2005 frontend: incomp_if2.v
Parsing Verilog input from `incomp_if2.v' to AST representation.
Generating RTLIL representation for module `\incomp_if2'.
Successfully finished Verilog frontend.

yosys> read_liberty -lib ../lib/sky130_fd_sc_hd__tt_025C_1v80.lib

2. Executing Liberty frontend.
Imported 418 cell types from liberty file.

yosys> synth -top incomp_if2
```

```
ABC: + write_blif <abc-temp-dir>/output.blif

4.1.2. Re-integrating ABC results.
ABC RESULTS:   sky130_fd_sc_hd__mux2_1 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__or2_0 cells:         1
ABC RESULTS:        internal signals:        0
ABC RESULTS:           input signals:        4
ABC RESULTS:          output signals:        2
Removing temp directory.

yosys> show
```

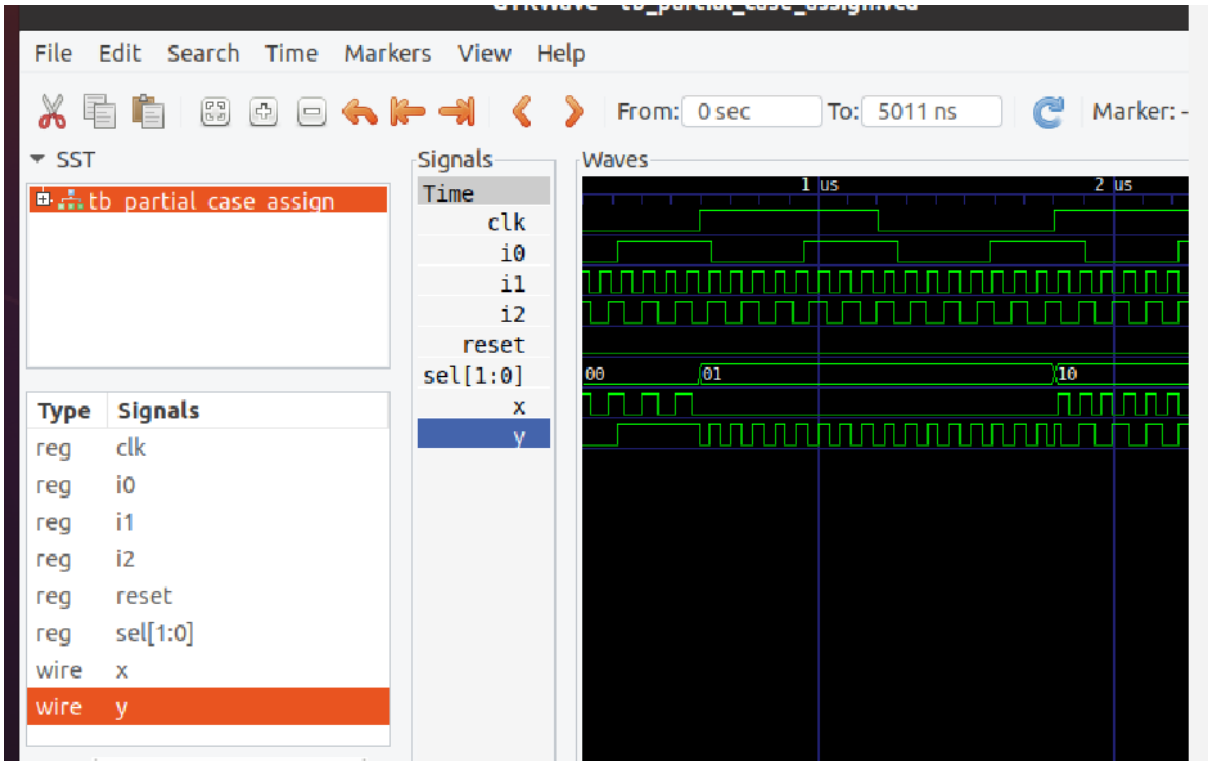


Partial_comp_case.v

```
a word index?
4 error(s) during elaboration.
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# vi tb_partial_case_assign.v
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# vim partial_case_assign.v
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# vi tb_partial_case_assign.v
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# iverilog partial_case_assign.v tb_partial_case_assig
n.v
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# ./a.out
VCD info: dumpfile tb_partial_case_assign.vcd opened for output.
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# gtkwave tb_partial_case_assign.v
Gtk-Message: 10:48:58.300: Failed to load module "canberra-gtk-module"

GTKWave Analyzer v3.3.103 (w)1999-2019 BSI


(gtkwave:3505): dconf-WARNING **: 10:48:58.337: failed to commit changes to dco
nf: The connection is closed
Near byte 20, VCD search table NULL..is this a VCD file?
Near byte 20, Unknown VCD identifier: 'ns'
No symbols in VCD file..is it malformed?  Exiting!
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# gtkwave tb_partial_case_assign.vcd
```

Error are corrected in testbench of tb_partial_comp_case.v

```
`timescale 1ns / 1ps
module tb_partial_case_assign;
        //input
        reg i0,i1,i2;
        reg [1:0] sel;
        // Output
        wire x,y;
        //TB_SIGNALS
        reg clk,reset;

        // Instantiate the Unit Under Test (UUT)
        partial_case_assign uut (
                .sel(sel),
                .i0(i0),
                .i1(i1),
                .i2(i2),

                .x(x),
                .y(y)
        );

        initial begin
        $dumpfile("tb_partial_case_assign.vcd");
        $dumpvars(0,tb_partial_case_assign);
```



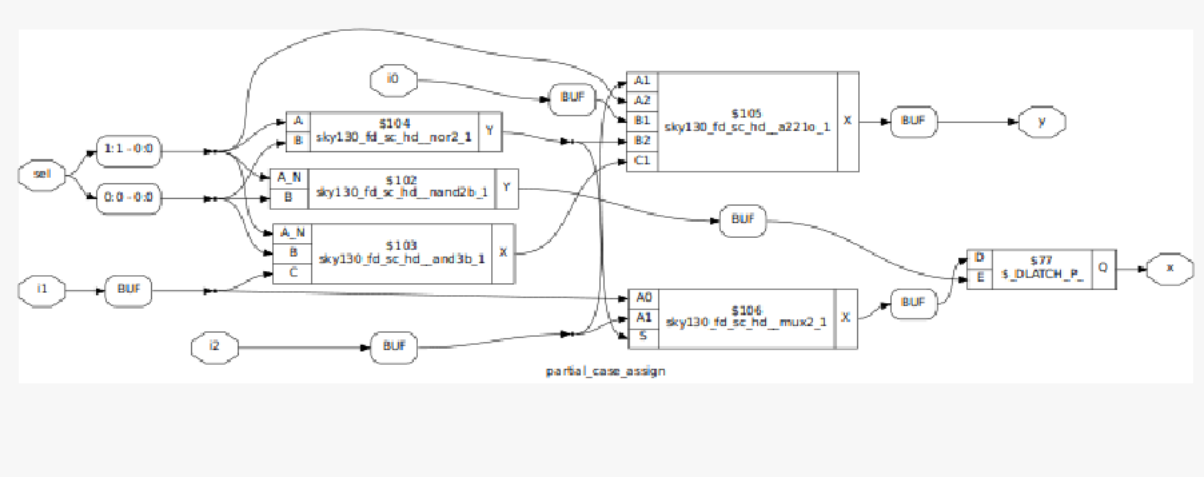
Synthesis top partial_comp_case

```
Top module:  \partial_case_assign
Removed 0 unused modules.

3.26. Printing statistics.

=== partial_case_assign ===

   Number of wires:                 14
   Number of wire bits:             15
   Number of public wires:           6
   Number of public wire bits:       7
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                 10
     $_ANDNOT_                       1
     $_DLATCH_P_                     1
     $_MUX_                          2
     $_NOR_                          1
     $_NOT_                          2
     $_OAI4_                         1
     $_ORNOT_                        1
     $_OR_                           1

3.27. Executing CHECK pass (checking for obvious problems).
checking module partial_case_assign..
found and reported 0 problems.
```

Abc -liberty ../lib/sky

```
ABC: + strash
ABC: + ifraig
ABC: + scorr
ABC: Warning: The network is combinational (run "fraig" or "fraig_sweep").
ABC: + dc2
ABC: + dretime
ABC: + retime
ABC: + strash
ABC: + &get -n
ABC: + &dch -f
ABC: + &nf
ABC: + &put
ABC: + write_blif <abc-temp-dir>/output.blif

4.1.2. Re-integrating ABC results.
ABC RESULTS:   sky130_fd_sc_hd__a221o_1 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__and3b_1 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__mux2_1 cells:         1
ABC RESULTS:   sky130_fd_sc_hd__nand2b_1 cells:       1
ABC RESULTS:   sky130_fd_sc_hd__nor2_1 cells:         1
ABC RESULTS:        internal signals:        6
ABC RESULTS:           input signals:        5
ABC RESULTS:          output signals:        3
Removing temp directory.
```

Show synthesis diagram,

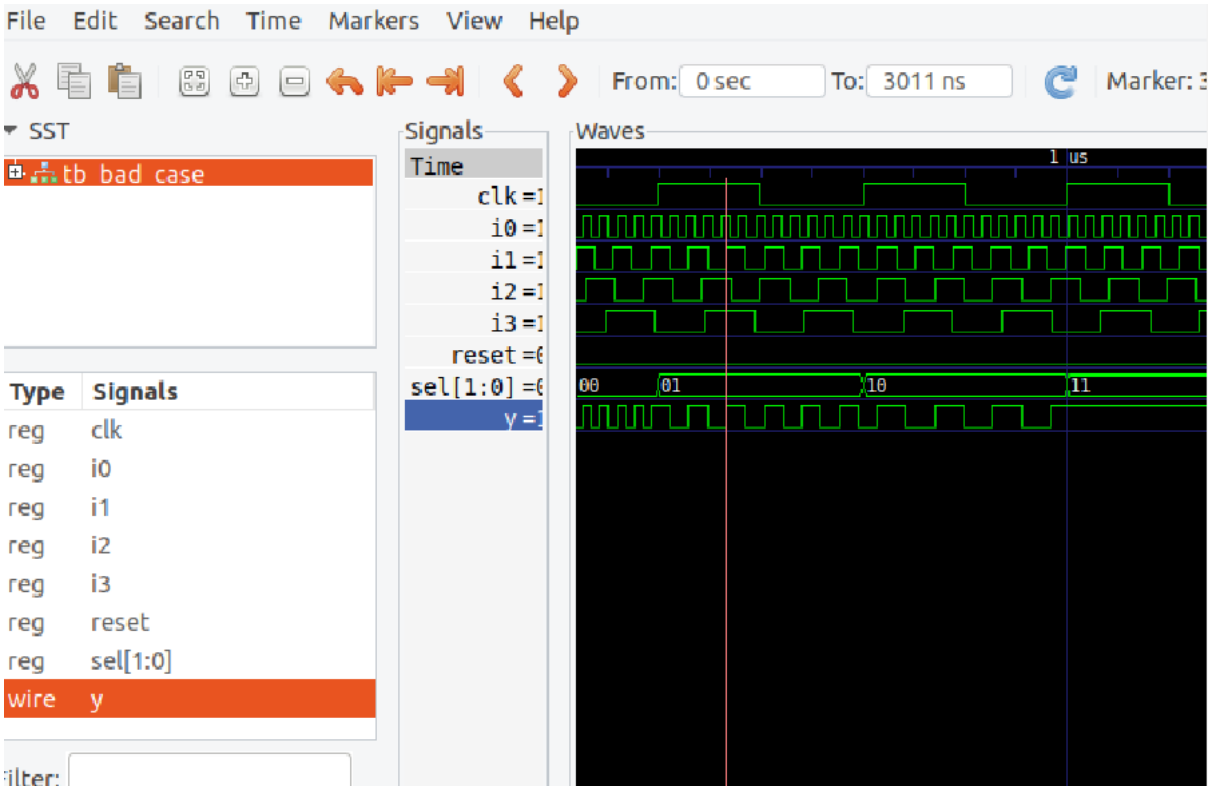


Bad_case.v

Compilation and simulation

```
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# iverilog bad_case.v tb_bad_case.v
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# ./a.out tb_bad_case.v
VCD info: dumpfile tb_bad_case.vcd opened for output.
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# gtkwave tb_bad_case.vcd
Gtk-Message: 11:55:38.789: Failed to load module "canberra-gtk-module"

GTKWave Analyzer v3.3.103 (w)1999-2019 BSI
```

bad_case.v simulation using gtkwave

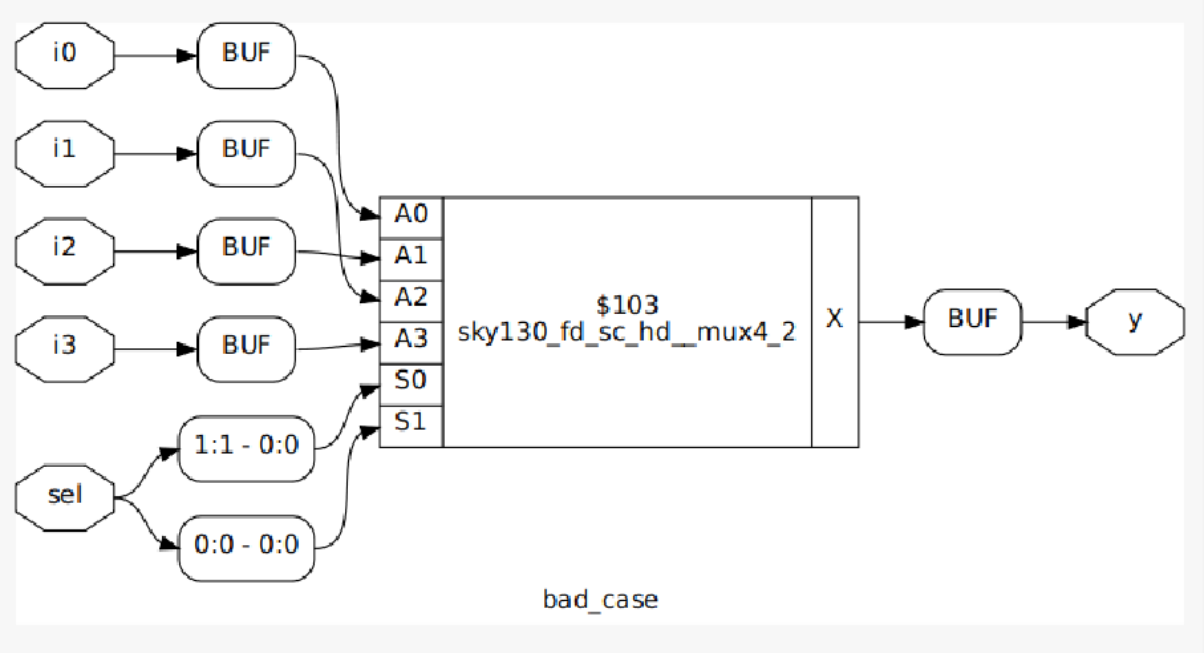


Bad_case.v Synthesis

```
=== bad_case ===

   Number of wires:                 13
   Number of wire bits:             14
   Number of public wires:           6
   Number of public wire bits:       7
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                  8
     $_ANDNOT_                       3
     $_AND_                          1
     $_AOI4_                         1
     $_MUX_                          1
     $_ORNOT_                        1
     $_OR_                           1

3.27. Executing CHECK pass (checking for obvious problems).
checking module bad_case..
found and reported 0 problems.

yosys>
```

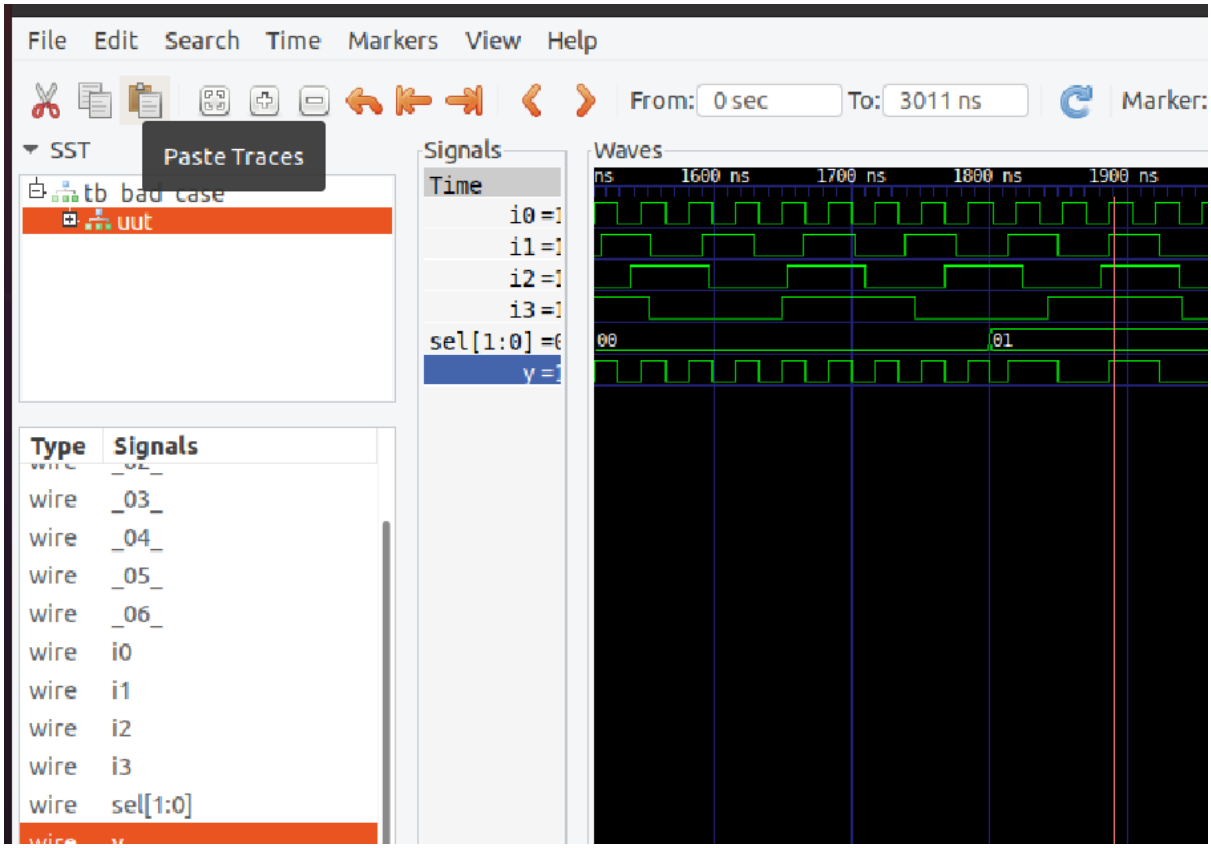
abc -liberty

```
4.1.2. Re-integrating ABC results.
ABC RESULTS:   sky130_fd_sc_hd__mux4_2 cells:        1
ABC RESULTS:        internal signals:        7
ABC RESULTS:           input signals:        6
ABC RESULTS:          output signals:        1
Removing temp directory.
```



Non Overlapping

```
sisWorkshop/verilog_files# iverilog ../my_lib/verilog_model/primitives.v ../my_
lib/verilog_model/
primitives.v       sky130_fd_sc_hd.v
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# iverilog ../my_lib/verilog_model/primitives.v ../my_
lib/verilog_model/sky130_fd_sc_hd.v bad_case_net.v tb_bad_case.v
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# ./a.out
VCD info: dumpfile tb_bad_case.vcd opened for output.
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# gtkwave tb_bad_case.vcd
Gtk-Message: 12:12:44.390: Failed to load module "canberra-gtk-module"
```


File
Edit
Search
Time
Markers
View
Help
From:
0 sec
To:
3011 ns
Marker:
Paste Traces
SST
tb_bad_case
uut
Signals
Time
i0 =
i1 =
i2 =
i3 =
sel[1:0] =
y =
Waves
ns
1600 ns
1700 ns
1800 ns
1900 ns
00
01
Type
Signals
wire _03_
wire _04_
wire _05_
wire _06_
wire i0
wire i1
wire i2
wire i3
wire sel[1:0]