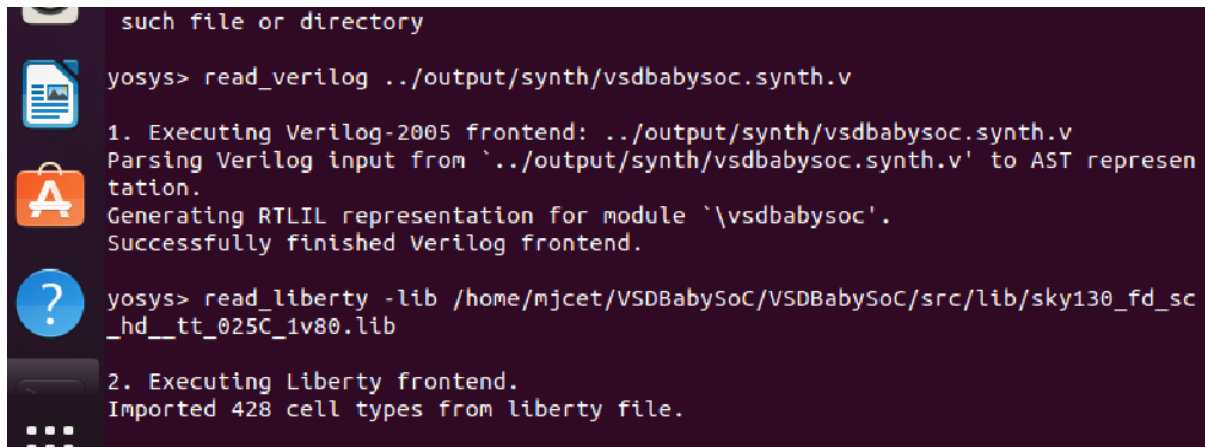


Unable to do STA

A terminal window with a dark purple background. The prompt is 'yosys>'. The first command is 'read_verilog ../output/synth/vsdbabysoc.synth.v'. The output shows '1. Executing Verilog-2005 frontend...' followed by parsing and RTLIL generation messages. The second command is 'read_liberty -lib /home/mjcet/VSDBabySoC/VSDBabySoC/src/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'. The output shows '2. Executing Liberty frontend...' and 'Imported 428 cell types from liberty file.'

```
such file or directory

yosys> read_verilog ../output/synth/vsdbabysoc.synth.v

1. Executing Verilog-2005 frontend: ../output/synth/vsdbabysoc.synth.v
Parsing Verilog input from '../output/synth/vsdbabysoc.synth.v' to AST representation.
Generating RTLIL representation for module '\vsdbabysoc'.
Successfully finished Verilog frontend.

yosys> read_liberty -lib /home/mjcet/VSDBabySoC/VSDBabySoC/src/lib/sky130_fd_sc_hd__tt_025C_1v80.lib

2. Executing Liberty frontend.
Imported 428 cell types from liberty file.
```

The STA checks are performed across all the corners to confirm the design meets the target timing requirements.

- The worst max path (Setup-critical) corners in the sub-40nm process nodes are usually: ss_LowTemp_LowVolt, ss_HighTemp_LowVolt (Slowest corners)
- The worst min path (Hold-critical) corners being: ff_LowTemp_HighVolt, ff_HighTemp_HighVolt (Fastest corners)
- The below tcl script [sta_across_pvt.tcl](#) can be run to performt the STA across the PVT corners for which the sky130 lib files are available:
- set list_of_lib_files(1) "sky130_fd_sc_hd__tt_025C_1v80.lib"
- set list_of_lib_files(2) "sky130_fd_sc_hd__ff_100C_1v65.lib"
- set list_of_lib_files(3) "sky130_fd_sc_hd__ff_100C_1v95.lib"
- set list_of_lib_files(4) "sky130_fd_sc_hd__ff_n40C_1v56.lib"
- set list_of_lib_files(5) "sky130_fd_sc_hd__ff_n40C_1v65.lib"
- set list_of_lib_files(6) "sky130_fd_sc_hd__ff_n40C_1v76.lib"
- set list_of_lib_files(7) "sky130_fd_sc_hd__ss_100C_1v40.lib"
- set list_of_lib_files(8) "sky130_fd_sc_hd__ss_100C_1v60.lib"
- set list_of_lib_files(9) "sky130_fd_sc_hd__ss_n40C_1v28.lib"

- set list_of_lib_files(10) "sky130_fd_sc_hd__ss_n40C_1v35.lib"
- set list_of_lib_files(11) "sky130_fd_sc_hd__ss_n40C_1v40.lib"
- set list_of_lib_files(12) "sky130_fd_sc_hd__ss_n40C_1v44.lib"
- set list_of_lib_files(13) "sky130_fd_sc_hd__ss_n40C_1v76.lib"
-
- for {set i 1} {\$i <= [array size list_of_lib_files]} {incr i} {
- read_liberty ./timing_libs/\$list_of_lib_files(\$i)
- read_verilog ./riscv_pipelined_Final_netlist.v
- link_design riscv_core
- current_design
- read_sdc riscv_core_synthesis.sdc
- check_setup -verbose
- report_checks -path_delay min_max -fields {nets cap slew input_pins fanout} -digits {4} > ./sta_output/min_max_\$list_of_lib_files(\$i).txt
-
- exec echo "\$list_of_lib_files(\$i)" >> ./sta_output/sta_worst_max_slack.txt
- report_worst_slack -max -digits {4} >> ./sta_output/sta_worst_max_slack.txt
-
- exec echo "\$list_of_lib_files(\$i)" >> ./sta_output/sta_worst_min_slack.txt
- report_worst_slack -min -digits {4} >> ./sta_output/sta_worst_min_slack.txt
-
- exec echo "\$list_of_lib_files(\$i)" >> ./sta_output/sta_tns.txt
- report_tns -digits {4} >> ./sta_output/sta_tns.txt
-
- exec echo "\$list_of_lib_files(\$i)" >> ./sta_output/sta_wns.txt
- report_wns -digits {4} >> ./sta_output/sta_wns.txt
- }

PVT Corner	Worst Setup Slack	Worst Hold Slack	WNS	TNS
tt_025C_1v80	-7.4403	-2.8904	-7.4403	-7477.7690
ff_100C_1v65	-6.4158	-2.9509	-6.4158	-6048.2212
ff_100C_1v95	-4.7488	-3.0040	-4.7488	-4155.6294
ff_n40C_1v56	-6.2602	-2.9085	-6.2602	-6312.1372
ff_n40C_1v65	-5.1682	-2.9449	-5.1682	-5053.1143
ff_n40C_1v76	-4.2362	-2.9757	-4.2362	-4004.4890
ss_100C_1v40	-27.9272	-2.2947	-27.9272	-32115.2148
ss_100C_1v60	-18.2358	-2.5580	-18.2358	-20115.0840
ss_n40C_1v28	-51.4456	-1.8463	-51.4456	-72154.9375
ss_n40C_1v35	-37.8016	-1.9116	-37.8016	-51688.5156
ss_n40C_1v40	-31.4799	-2.0751	-31.4799	-42060.9805
ss_n40C_1v44	-27.4636	-2.2091	-27.4636	-36005.7109
ss_n40C_1v76	-12.3806	-2.6962	-12.3806	-14293.3408

