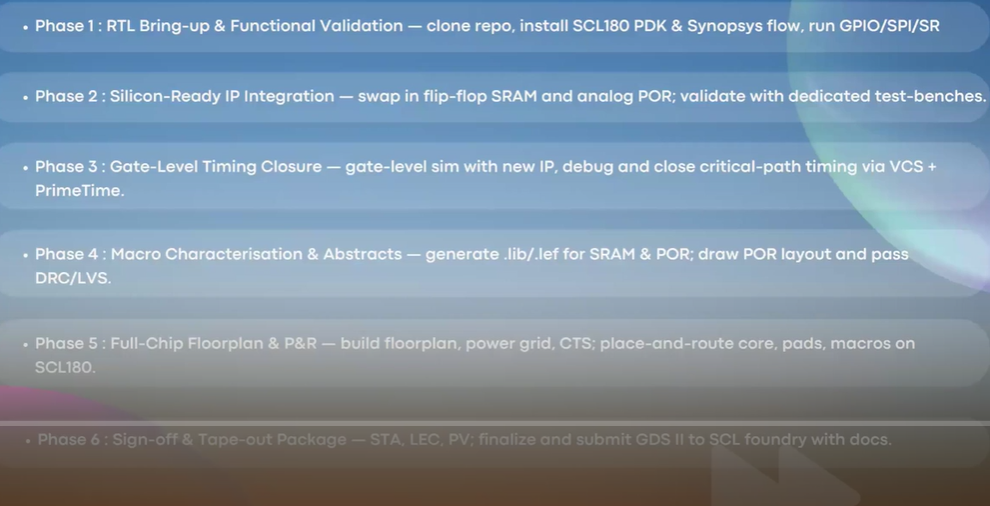
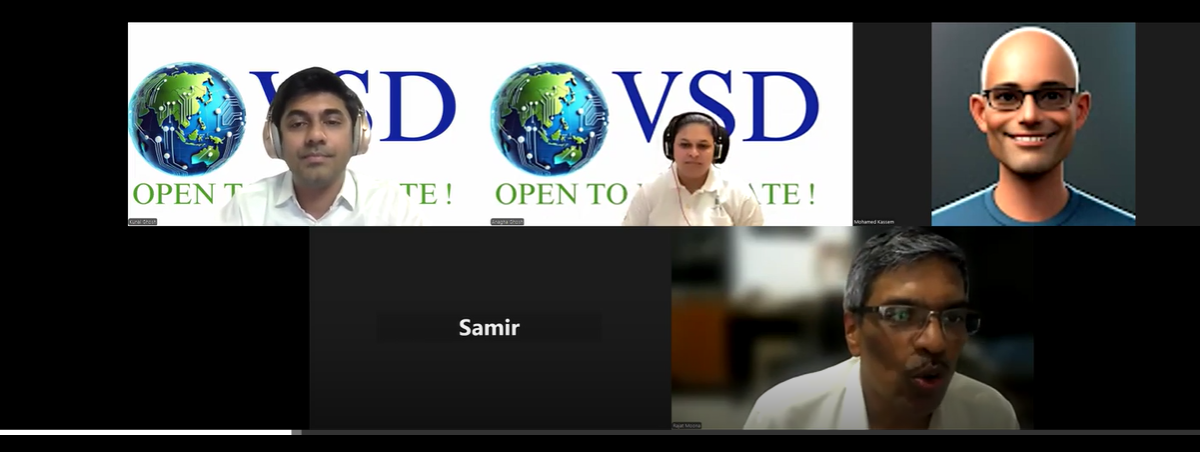
**Introduction Done by Kunal Ghosh Founder and CEO of VSD**

Road Map of the Program in Phase 1 to Phase 6 and Phase 7 is to fabricate the RISC V SoC Design

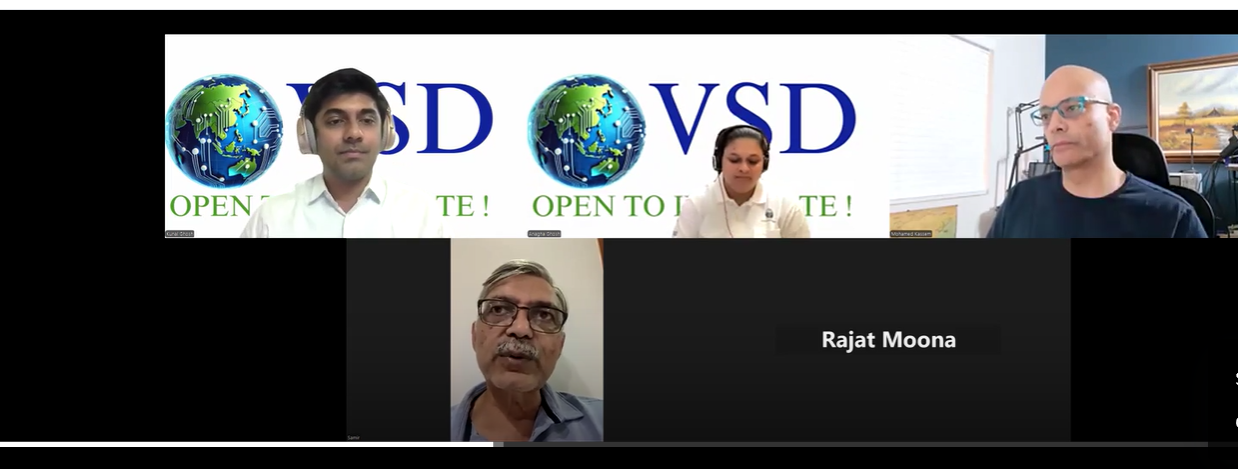
3579 Participants scaled to 50 Participants will be invited in the IIT Ghandinagar work Synopsys signoff tools to fabricate final 20 Participants will scale down to fabricate the chip

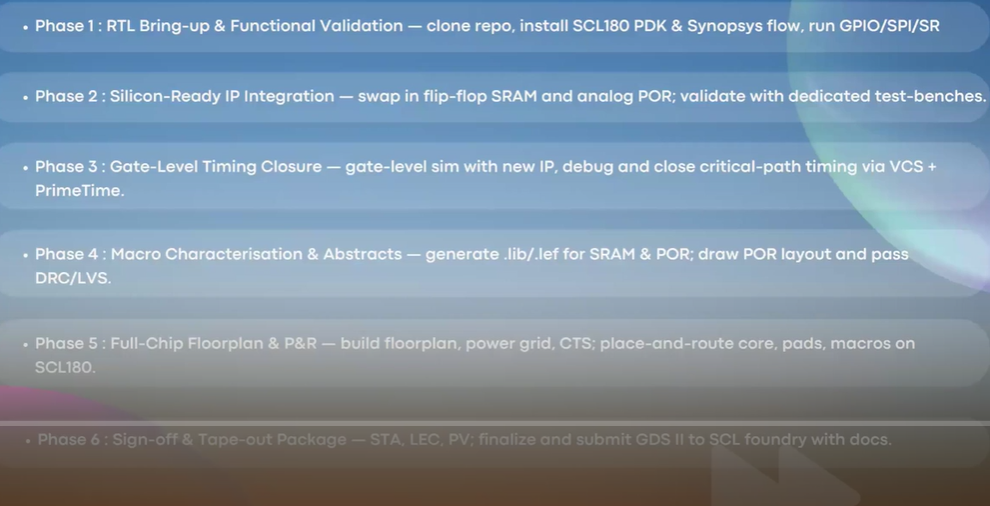
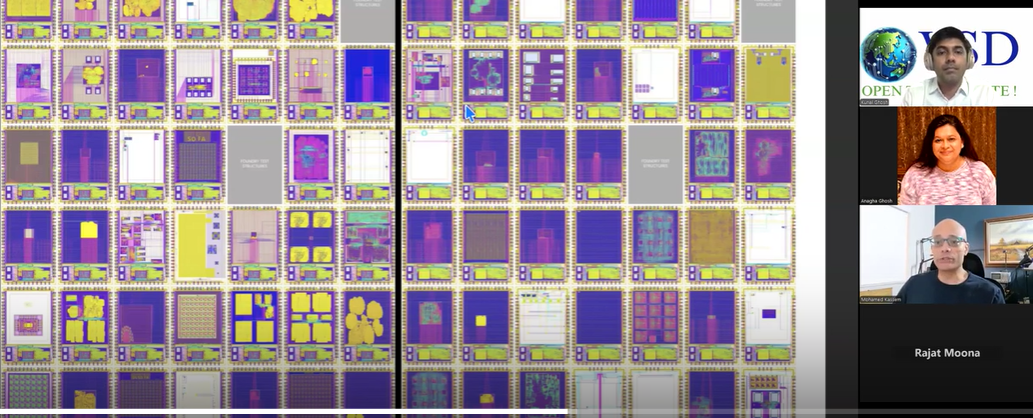
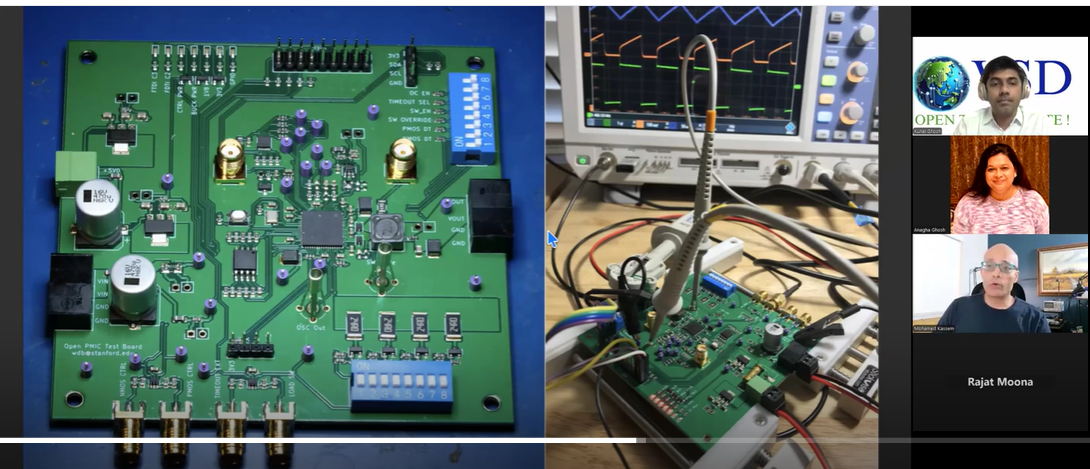
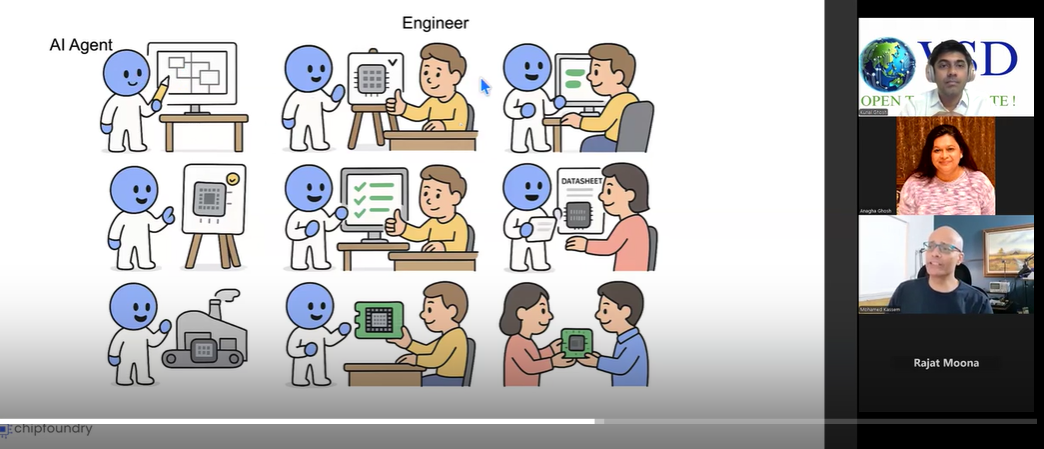
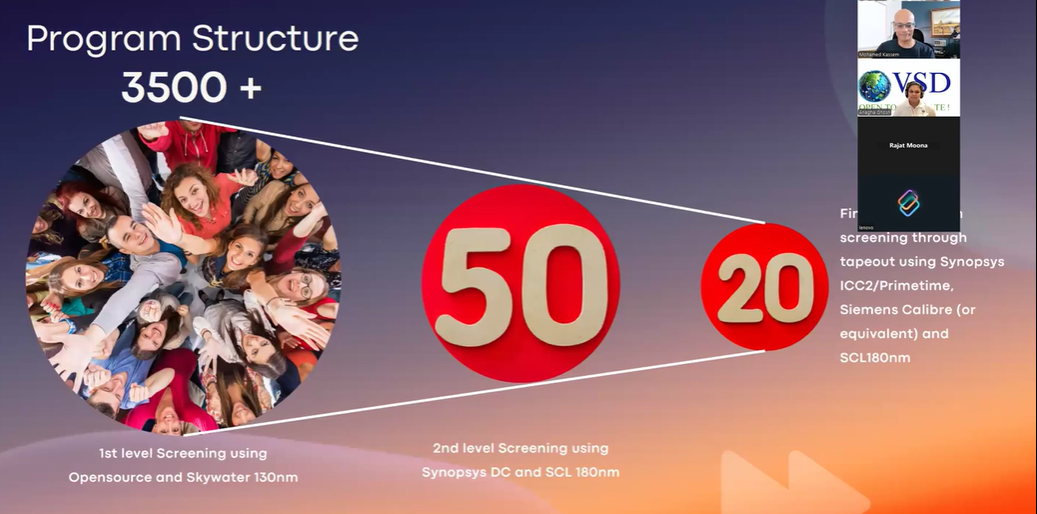


**Key Note Speaker Director IIT Ghandhinagar**



**Speaker Faculty IIT Ghandinagar Mr Sameer**





A **VLSI (Very Large Scale Integration) System Design Program** generally involves multiple phases aimed at designing complex integrated circuits (ICs) or chips. The process includes a variety of tasks such as requirement analysis, specification, design, verification, fabrication, and testing. Here’s a summary of the typical phases involved in a VLSI system design program, from Phase 1 to Phase 7:

**Phase 1: Requirement Analysis & System Specification**

* **Objective**: Define the functional and non-functional requirements of the VLSI system.
* **Activities**:
  + **Requirement Gathering**: Collect input from stakeholders to understand what the system should do, including performance, power, area, and speed specifications.
  + **Feasibility Study**: Conduct a feasibility analysis for the design, considering constraints such as technology, cost, and time.
  + **High-Level Specifications**: Write detailed system specifications, including system architecture, features, interfaces, and expected outcomes.
* **Deliverables**:
  + System Requirements Document (SRD)
  + Preliminary Design Outline

**Phase 2: Architectural Design & High-Level Design**

* **Objective**: Develop the overall architecture of the system and define the components of the VLSI design.
* **Activities**:
  + **System Architecture**: Choose between various architectural options (e.g., data path design, control path design) based on specifications.
  + **Block-Level Design**: Define key blocks and modules, such as ALU (Arithmetic Logic Unit), memory units, and I/O modules.
  + **Technology Selection**: Decide on the fabrication process (e.g., CMOS, BiCMOS) and technology node (e.g., 7nm, 14nm).
  + **Interface Design**: Define communication protocols and interface standards (e.g., I2C, SPI).
* **Deliverables**:
  + Architectural Design Document
  + Block Diagram

**Phase 3: RTL Design (Register Transfer Level Design)**

* **Objective**: Convert the high-level architectural design into a register-transfer-level (RTL) representation, which is the primary description of the system.
* **Activities**:
  + **HDL Coding**: Use hardware description languages (HDL), such as VHDL or Verilog, to describe the behavior and structure of each block in the system.
  + **RTL Simulation**: Perform functional simulation to ensure the design behaves as expected.
  + **Synthesis Constraints**: Define constraints such as clock frequency, power limits, and area requirements.
* **Deliverables**:
  + RTL Code (VHDL/Verilog)
  + Simulation Results

**Phase 4: Functional Verification**

* **Objective**: Verify that the RTL design meets the functional requirements and specifications.
* **Activities**:
  + **Testbench Development**: Create a test environment to simulate different test cases for the design.
  + **Verification Tools**: Use simulation tools such as ModelSim, Synopsys VCS, or Cadence Incisive to run simulations and check functional correctness.
  + **Formal Verification**: Use formal methods to prove that the design satisfies its specification under all conditions.
* **Deliverables**:
  + Verification Reports
  + Functional Coverage Analysis
  + Debugged RTL Code

**Phase 5: Synthesis & Logic Optimization**

* **Objective**: Convert the RTL design into a gate-level netlist, optimizing the design for area, speed, and power.
* **Activities**:
  + **Synthesis**: Use tools like Synopsys Design Compiler or Cadence Genus to convert RTL into gate-level representation.
  + **Logic Optimization**: Optimize the design for speed, area, and power consumption.
  + **Constraints Application**: Apply design constraints for timing, power, and area during synthesis.
  + **Clock Tree Synthesis (CTS)**: Ensure proper clock distribution across the chip.
* **Deliverables**:
  + Gate-Level Netlist
  + Timing and Power Analysis Reports

**Phase 6: Physical Design (Layout Design)**

* **Objective**: Convert the gate-level netlist into a physical layout, which can be fabricated as a chip.
* **Activities**:
  + **Floorplanning**: Decide on the placement of functional blocks on the chip.
  + **Placement & Routing**: Place the logic gates and route the connections between them.
  + **Design Rule Checking (DRC)**: Ensure that the design meets the manufacturing process's design rules.
  + **Layout Verification**: Perform layout-versus-schematic (LVS) checks to ensure that the physical design matches the logical design.
  + **Power and Signal Integrity**: Analyze the chip for issues like crosstalk, voltage drops, and power distribution.
* **Deliverables**:
  + Physical Layout (GDSII/LEF/DEF files)
  + DRC and LVS Reports
  + Power Grid Analysis

**Phase 7: Fabrication & Testing**

* **Objective**: Fabricate the physical chip and test its performance in real-world conditions.
* **Activities**:
  + **Tape-out**: Finalize the design and send it for fabrication.
  + **Fabrication**: The actual chip is fabricated in a semiconductor foundry.
  + **Testing**: Perform various tests to ensure the chip functions as intended. This could involve functional testing, performance testing, and yield analysis.
  + **Post-Silicon Debug**: If issues are found during testing, debug the chip and refine the design.
  + **Package and Deploy**: Once the chip passes testing, it is packaged and sent to customers or integrated into larger systems.
* **Deliverables**:
  + Silicon Chip
  + Test Reports (e.g., Functional Test, Timing Test)
  + Yield Analysis Report

**Summary of Phases:**

| **Phase** | **Description** |
| --- | --- |
| **Phase 1** | Requirement Analysis & System Specification |
| **Phase 2** | Architectural Design & High-Level Design |
| **Phase 3** | RTL Design (VHDL/Verilog) |
| **Phase 4** | Functional Verification |
| **Phase 5** | Synthesis & Logic Optimization |
| **Phase 6** | Physical Design (Layout Design) |
| **Phase 7** | Fabrication & Testing |

**Conclusion:**

A **VLSI System Design Program** is a highly iterative and complex process that spans from conceptualizing the system requirements to the final chip fabrication and testing. Each phase requires attention to detail, from functional verification to physical design and post-silicon validation. Success in VLSI design hinges on ensuring each phase is meticulously executed and thoroughly tested.