

Lab4 Opt-check4

```
root@raheem: /home/raheem/week1/sky130RTLDesignAnd...
opt_checks.v tb_opt_check2.v tb_opt_checks.vcd
opt_check4.v tb_opt_check2.vcd tb_opt_check.v
root@raheem: /home/raheem/week1/sky130RTLDesignAndSynthesisWorkshop-main/verilog
_files# yosys

/-----/
|
| yosys -- Yosys Open SYnthesis Suite
|
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|
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Yosys 0.9 (git sha1 1979e0b)

yosys> read_verilog opt_check4
```

3.26. Printing statistics.

```
=== opt_check4 ===
```

Number of wires:	7
Number of wire bits:	7
Number of public wires:	4
Number of public wire bits:	4
Number of memories:	0
Number of memory bits:	0
Number of processes:	0
Number of cells:	4
\$_AOI3_	1
\$_MUX_	1
\$_NOT_	2

3.27. Executing CHECK pass (checking for obvious problems).

```
checking module opt_check4..  
found and reported 0 problems.
```

```
yosys>
```

```
ABC: + &put  
ABC: + write_blif <abc-temp-dir>/output.blif
```

4.1.2. Re-integrating ABC results.

```
ABC RESULTS: sky130_fd_sc_hd__xnor2_1 cells:      1  
ABC RESULTS:      internal signals:      3  
ABC RESULTS:      input signals:      3  
ABC RESULTS:      output signals:      1  
Removing temp directory.
```

```
yosys> █
```

