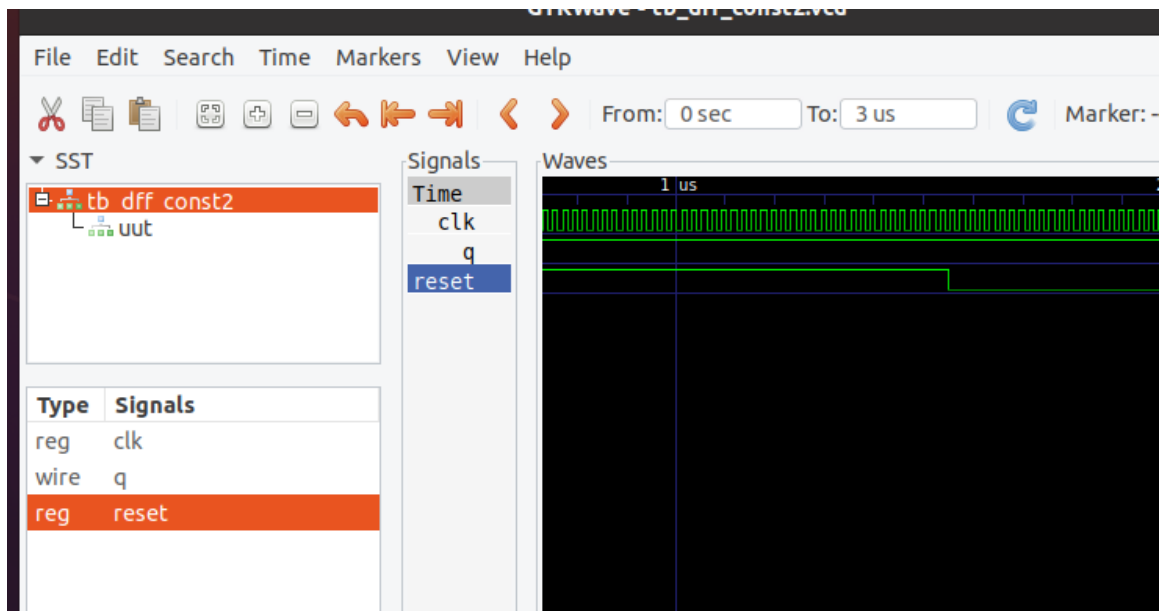Lab 6 dff_const2

```
...
root@raheem:/home/raheem/week1/sky130RTLDesignAndSynthesisWorkshop-main/verilog
_files# iverilog dff_const2.v tb_dff_const2.v
root@raheem:/home/raheem/week1/sky130RTLDesignAndSynthesisWorkshop-main/verilog
_files# ./a.out
VCD info: dumpfile tb_dff_const2.vcd opened for output.
root@raheem:/home/raheem/week1/sky130RTLDesignAndSynthesisWorkshop-main/verilog
_files# gtkwave tb_dff_const2.vcd
Gtk-Message: 10:59:37.171: Failed to load module "canberra-gtk-module"

GTKWave Analyzer v3.3.103 (w)1999-2019 BSI
```

```
    sky130_fd_sc_hd__dfrtp_1 _DFF_PN0_ (.CLK( C), .D( D), .Q( Q), .RESET_B( R))
;
    sky130_fd_sc_hd__dfstp_2 _DFF_PN1_ (.CLK( C), .D( D), .Q( Q), .SET_B( R));
    sky130_fd_sc_hd__dfrtp_1 _DFF_PP0_ (.CLK( C), .D( D), .Q( Q), .RESET_B(~R))
;
    sky130_fd_sc_hd__dfstp_2 _DFF_PP1_ (.CLK( C), .D( D), .Q( Q), .SET_B(~R));
    sky130_fd_sc_hd__dfbbn_1 _DFFSR_NNN_ (.CLK_N( C), .D( D), .Q( Q), .Q_N(~Q),
 .RESET_B( R), .SET_B( S));
    sky130_fd_sc_hd__dfbbn_1 _DFFSR_NNP_ (.CLK_N( C), .D( D), .Q( Q), .Q_N(~Q),
 .RESET_B(~R), .SET_B( S));
    sky130_fd_sc_hd__dfbbn_1 _DFFSR_NPN_ (.CLK_N( C), .D( D), .Q( Q), .Q_N(~Q),
 .RESET_B( R), .SET_B(~S));
    sky130_fd_sc_hd__dfbbn_1 _DFFSR_NPP_ (.CLK_N( C), .D( D), .Q( Q), .Q_N(~Q),
 .RESET_B(~R), .SET_B(~S));
    sky130_fd_sc_hd__dfbbp_1 _DFFSR_PNN_ (.CLK( C), .D( D), .Q( Q), .Q_N(~Q), .
RESET_B( R), .SET_B( S));
    sky130_fd_sc_hd__dfbbp_1 _DFFSR_PNP_ (.CLK( C), .D( D), .Q( Q), .Q_N(~Q), .
RESET_B(~R), .SET_B( S));
    sky130_fd_sc_hd__dfbbp_1 _DFFSR_PPN_ (.CLK( C), .D( D), .Q( Q), .Q_N(~Q), .
RESET_B( R), .SET_B(~S));
    sky130_fd_sc_hd__dfbbp_1 _DFFSR_PPP_ (.CLK( C), .D( D), .Q( Q), .Q_N(~Q), .
RESET_B(~R), .SET_B(~S));
Mapping DFF cells in module `\dff_const2':
```

File   Edit   Search   Time   Markers   View   Help

From: 0 sec   To: 3 us   Marker: –

SST

▼ SST

tb_dff_const2
    uut

Type	Signals
reg	clk
wire	q
reg	reset

Signals

Time
    clk
      q
reset

Waves

1 us

```
=== dff_const2 ===

   Number of wires:                3
   Number of wire bits:            3
   Number of public wires:         3
   Number of public wire bits:     3
   Number of memories:             0
   Number of memory bits:          0
   Number of processes:            0
   Number of cells:                0


3.27. Executing CHECK pass (checking for obvious problems).
checking module dff_const2..
found and reported 0 problems.
```

reset

1'1 → BUF → q

clk

dff_const2