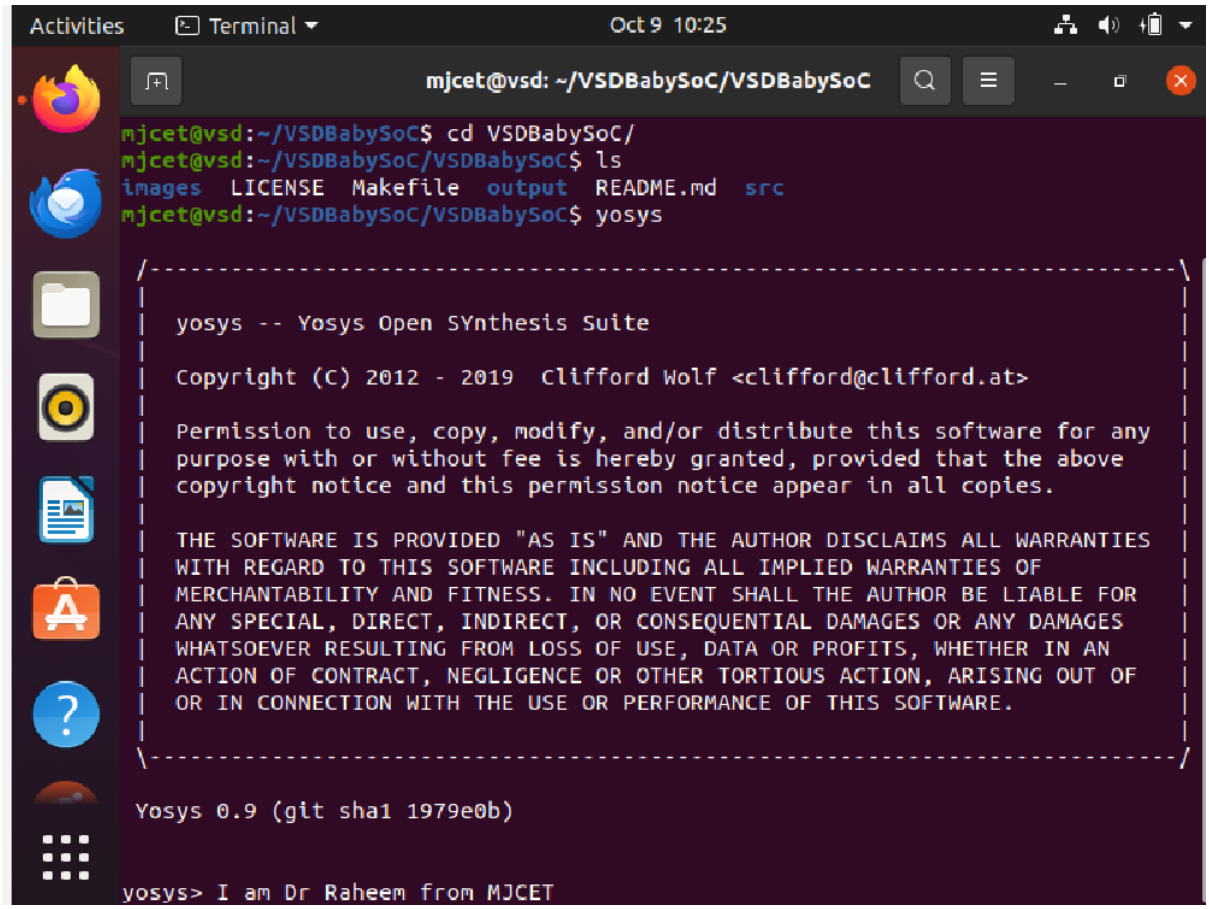
Steps for the Week 3 Assignment of Gate-Level-Synthesis and Funcutional Simualtion

Level I

Step1 Open the synthesis tool Yosys



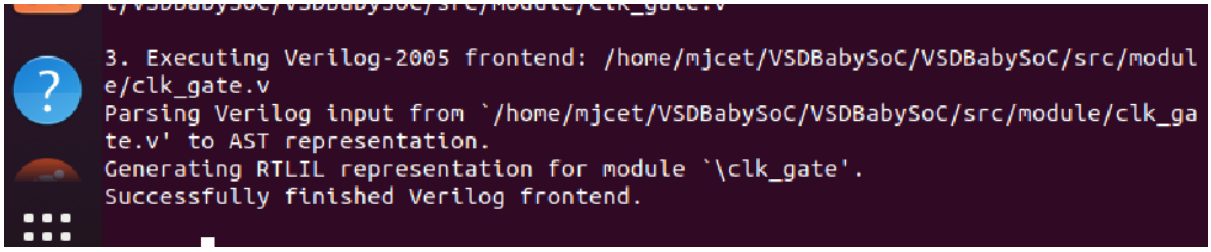
Load the Top-Level and other Verilog files

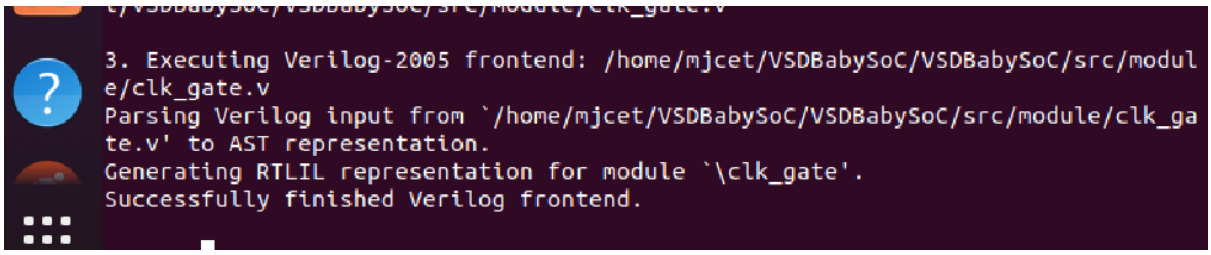
Step 2 : Read_verilog
/home/mjcet/VSDBabySoC/VSDBabySoC/src/module/vsdbabysoc.v

Step 3. Read_verilog -I path ...../Include rvmyth.v

```
yosys> read_verilog -I /home/mjcet/VSDBabySoC/VSDBabySoC/src/include /home/mjce
t/VSDBabySoC/VSDBabySoC/src/module/rvmyth.v

2. Executing Verilog-2005 frontend: /home/mjcet/VSDBabySoC/VSDBabySoC/src/modul
e/rvmyth.v
Parsing Verilog input from `/home/mjcet/VSDBabySoC/VSDBabySoC/src/module/rvmyth
.v' to AST representation.
Generating RTLIL representation for module `\rvmyth'.
Warning: Replacing memory \CPU_Xreg_value_a5 with list of registers. See rvmyth
_gen.v:696
Warning: Replacing memory \CPU_Xreg_value_a4 with list of registers. See rvmyth
_gen.v:695
Warning: Replacing memory \CPU_Dmem_value_a5 with list of registers. See rvmyth
_gen.v:686
Successfully finished Verilog frontend.
```

Step 4. read_verilog -I path ..../clk_gen.v



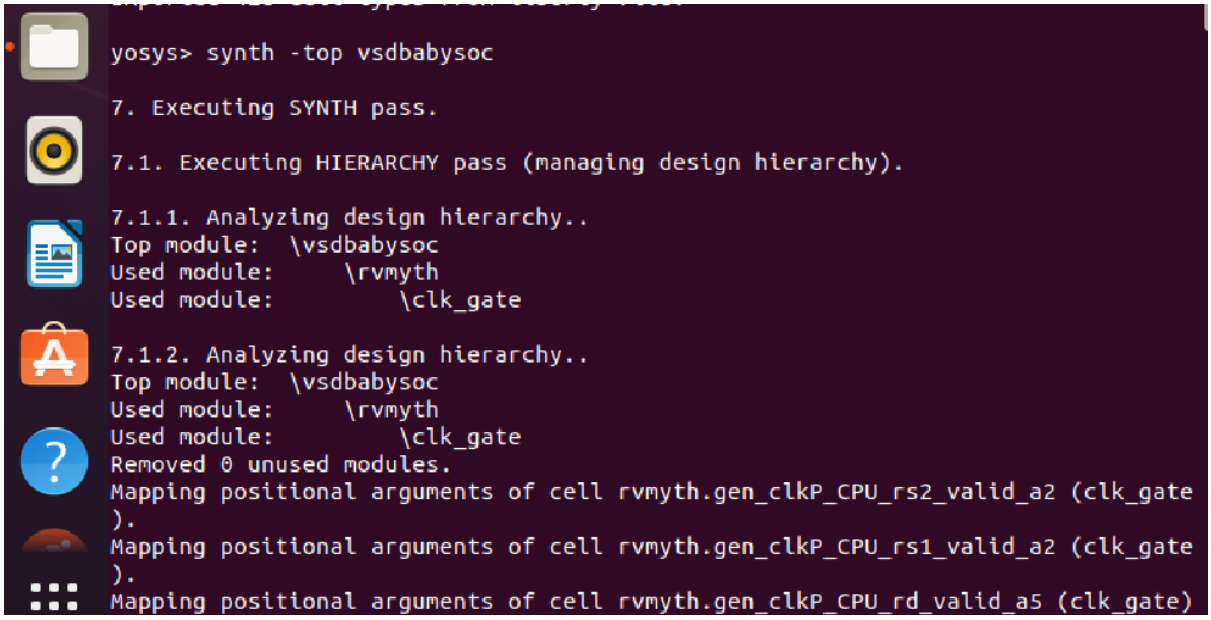


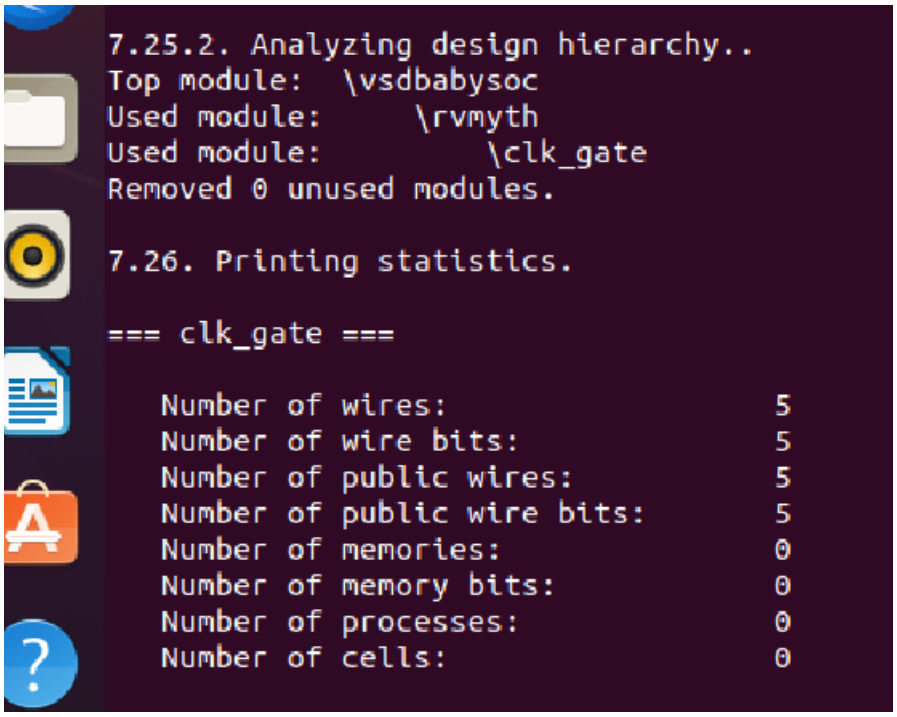
Level II

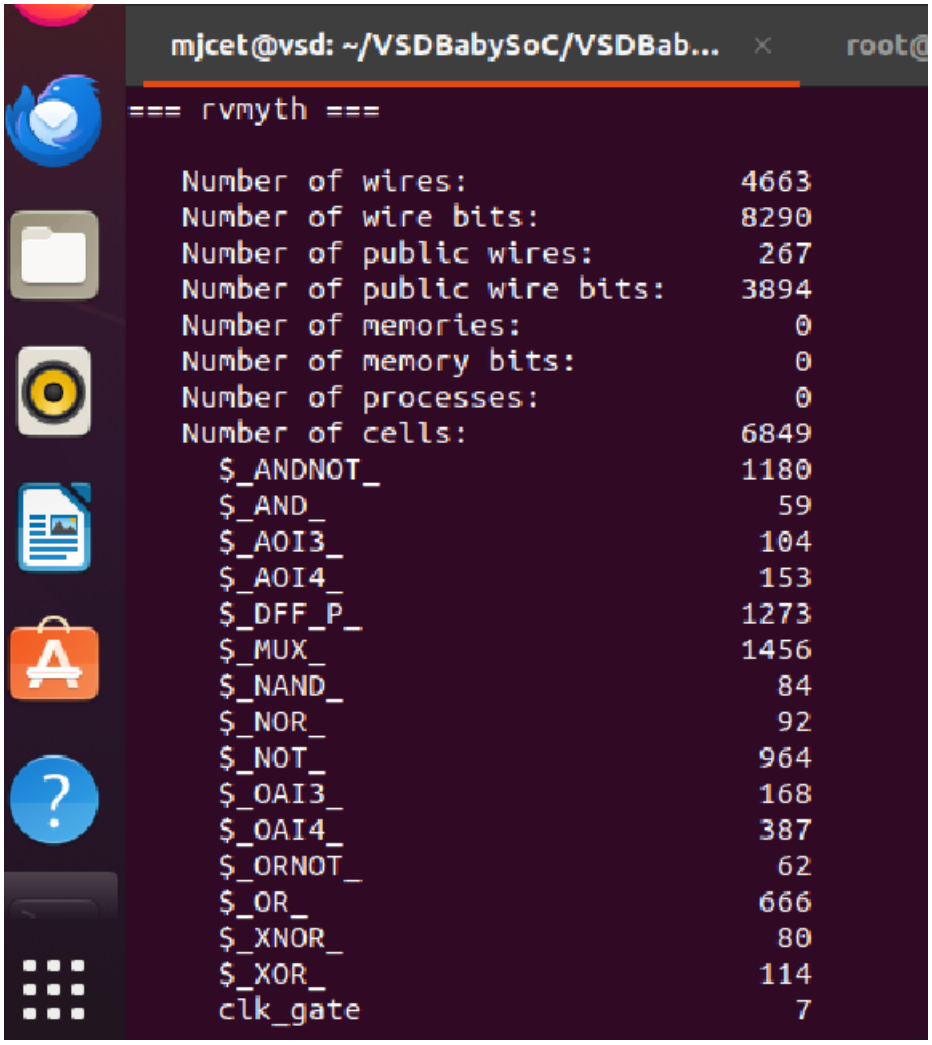
Load the library files

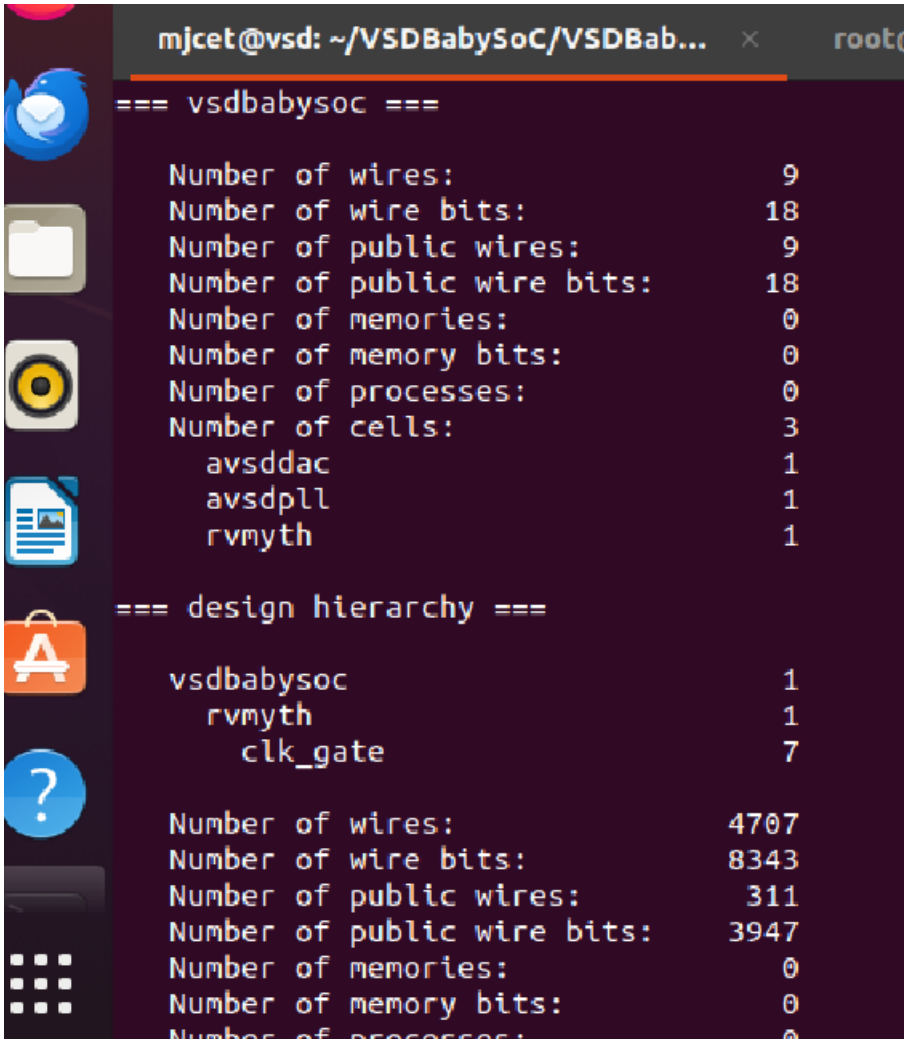
Level III

Synth -top vsdbabysoc.v






mjcet@vsd: ~/VSDBabySoC/VSDBab...
root@
=== rvmyth ===
Number of wires: 4663
Number of wire bits: 8290
Number of public wires: 267
Number of public wire bits: 3894
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 6849
$_ANDNOT_ 1180
$_AND_ 59
$_AOI3_ 104
$_AOI4_ 153
$_DFF_P_ 1273
$_MUX_ 1456
$_NAND_ 84
$_NOR_ 92
$_NOT_ 964
$_OAI3_ 168
$_OAI4_ 387
$_ORNOT_ 62
$_OR_ 666
$_XNOR_ 80
$_XOR_ 114
clk_gate 7

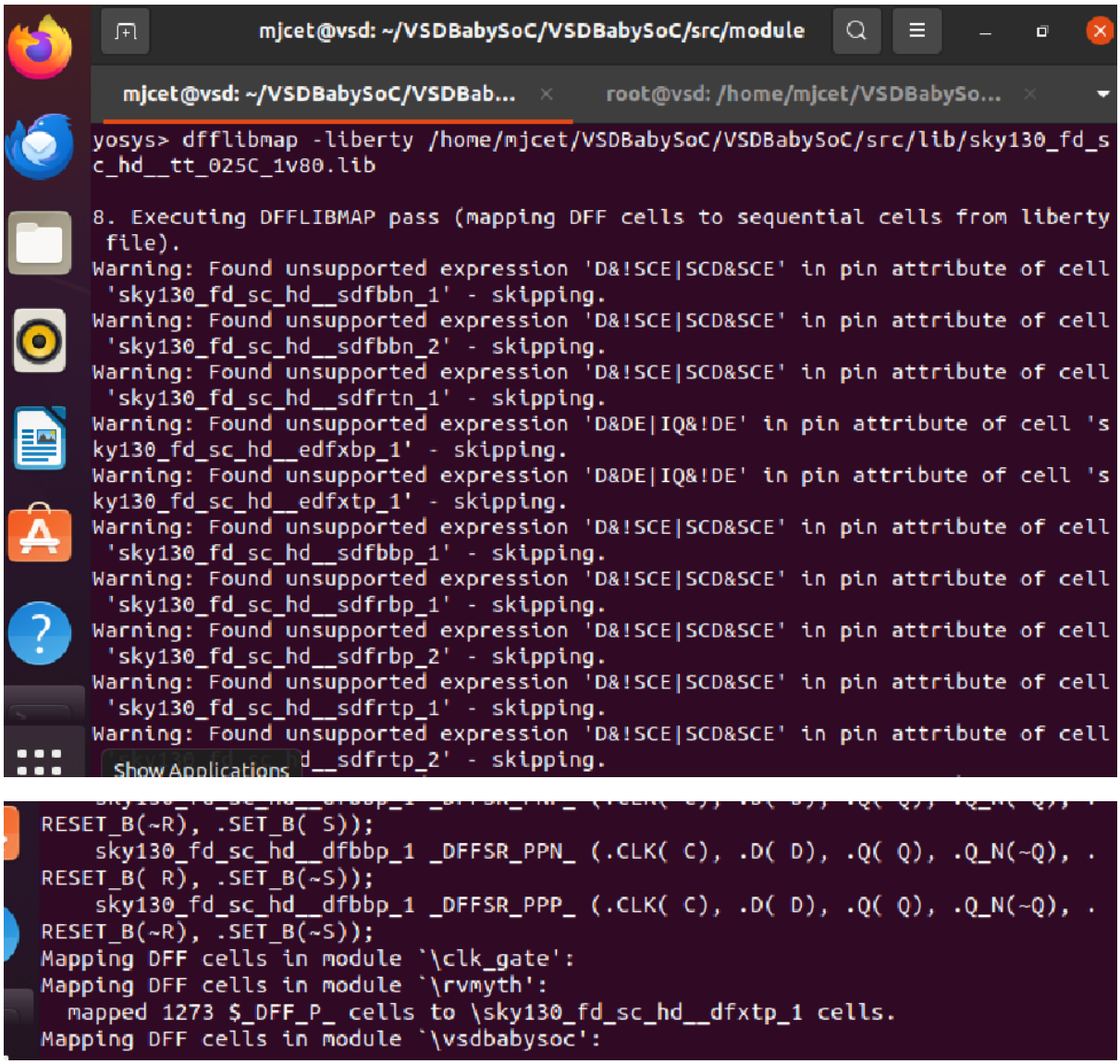



```
7.27. Executing CHECK pass (checking for obvious problems).
checking module clk_gate..
checking module rvmyth..
checking module vsdbabysoc..
found and reported 0 problems.

yosys> i am Dr Raheem
```

Level IV

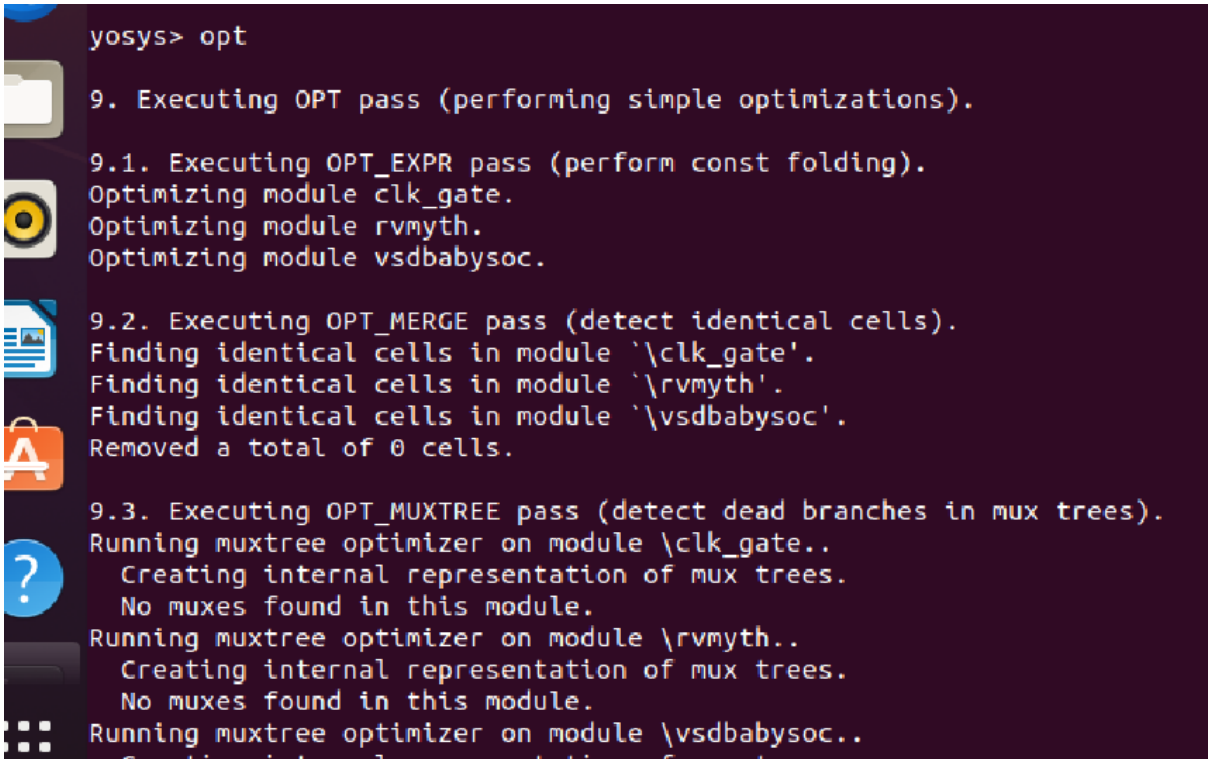
D Flip-Flop to Standard Cells

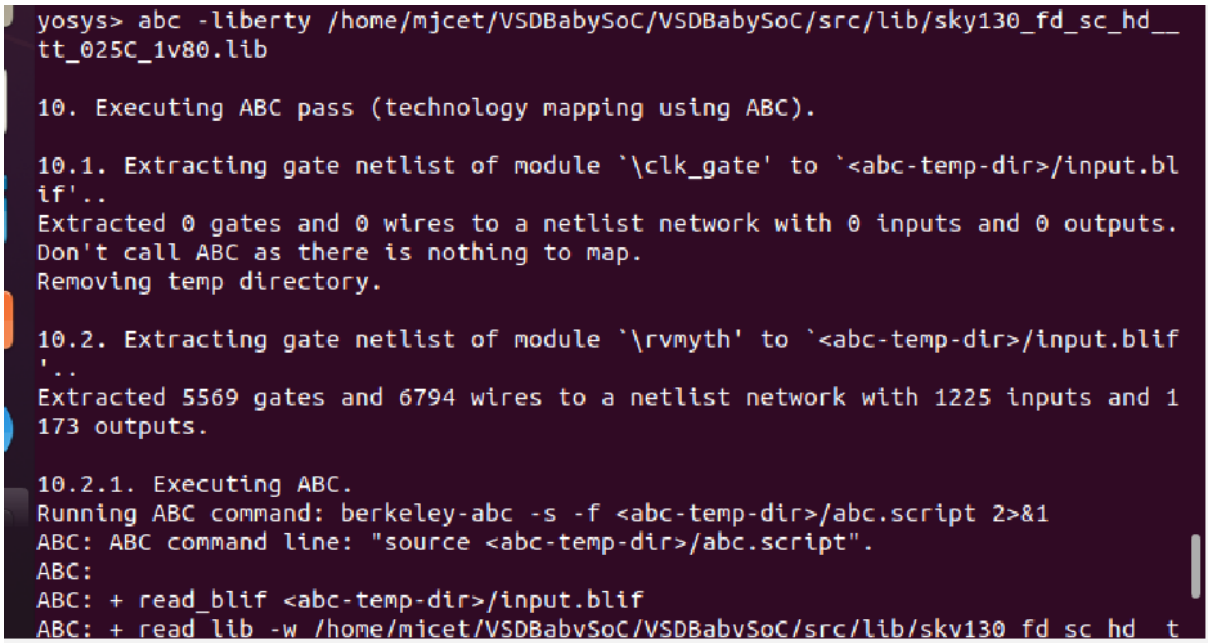
Dfflibmap -liberty

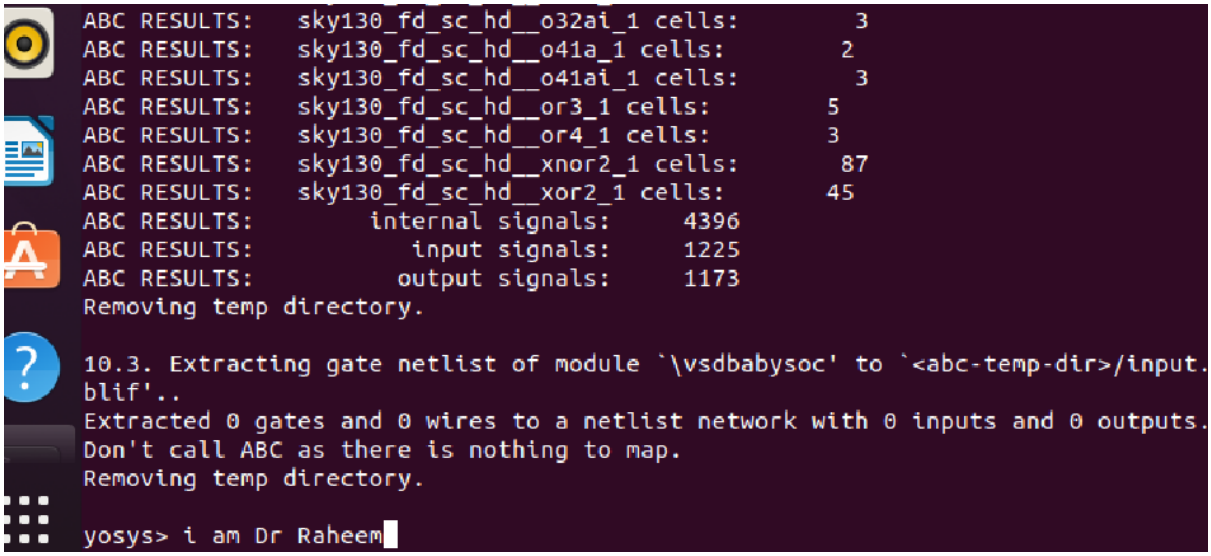


Level VI

Optimization and Technology Mapping

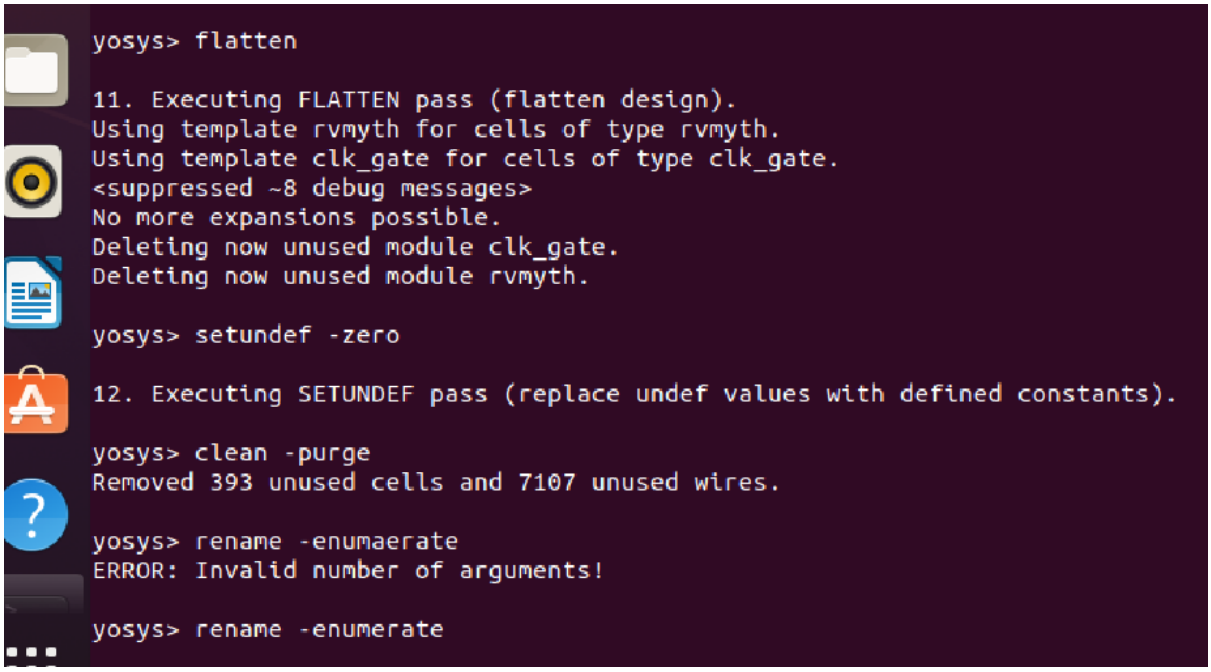

yosys> opt
9. Executing OPT pass (performing simple optimizations).
9.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module clk_gate.
Optimizing module rvmyth.
Optimizing module vsdbabysoc.
9.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\clk_gate'.
Finding identical cells in module `\rvmyth'.
Finding identical cells in module `\vsdbabysoc'.
Removed a total of 0 cells.
9.3. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \clk_gate..
Creating internal representation of mux trees.
No muxes found in this module.
Running muxtree optimizer on module \rvmyth..
Creating internal representation of mux trees.
No muxes found in this module.
Running muxtree optimizer on module \vsdbabysoc..


yosys> abc -liberty /home/mjcet/VSDBabySoC/VSDBabySoC/src/lib/sky130_fd_sc_hd__
tt_025C_1v80.lib
10. Executing ABC pass (technology mapping using ABC).
10.1. Extracting gate netlist of module `\clk_gate' to `<abc-temp-dir>/input.bl
if'..
Extracted 0 gates and 0 wires to a netlist network with 0 inputs and 0 outputs.
Don't call ABC as there is nothing to map.
Removing temp directory.
10.2. Extracting gate netlist of module `\rvmyth' to `<abc-temp-dir>/input.blif
'..
Extracted 5569 gates and 6794 wires to a netlist network with 1225 inputs and 1
173 outputs.
10.2.1. Executing ABC.
Running ABC command: berkeley-abc -s -f <abc-temp-dir>/abc.script 2>&1
ABC: ABC command line: "source <abc-temp-dir>/abc.script".
ABC:
ABC: + read_blif <abc-temp-dir>/input.blif
ABC: + read_lib -w /home/mjcet/VSDBabySoC/VSDBabySoC/src/lib/sky130_fd_sc_hd__t

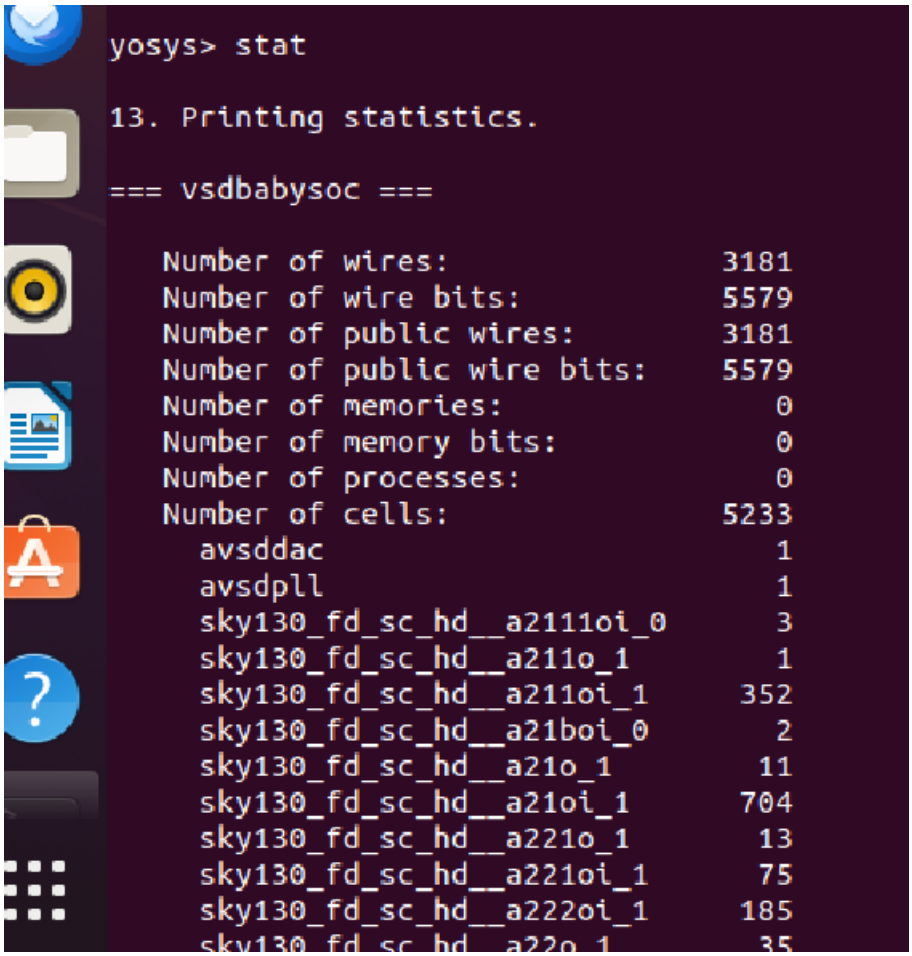


Level VII

Perform Final clean-up and renaming



Statistics



Level IX

Synthesis Netlist

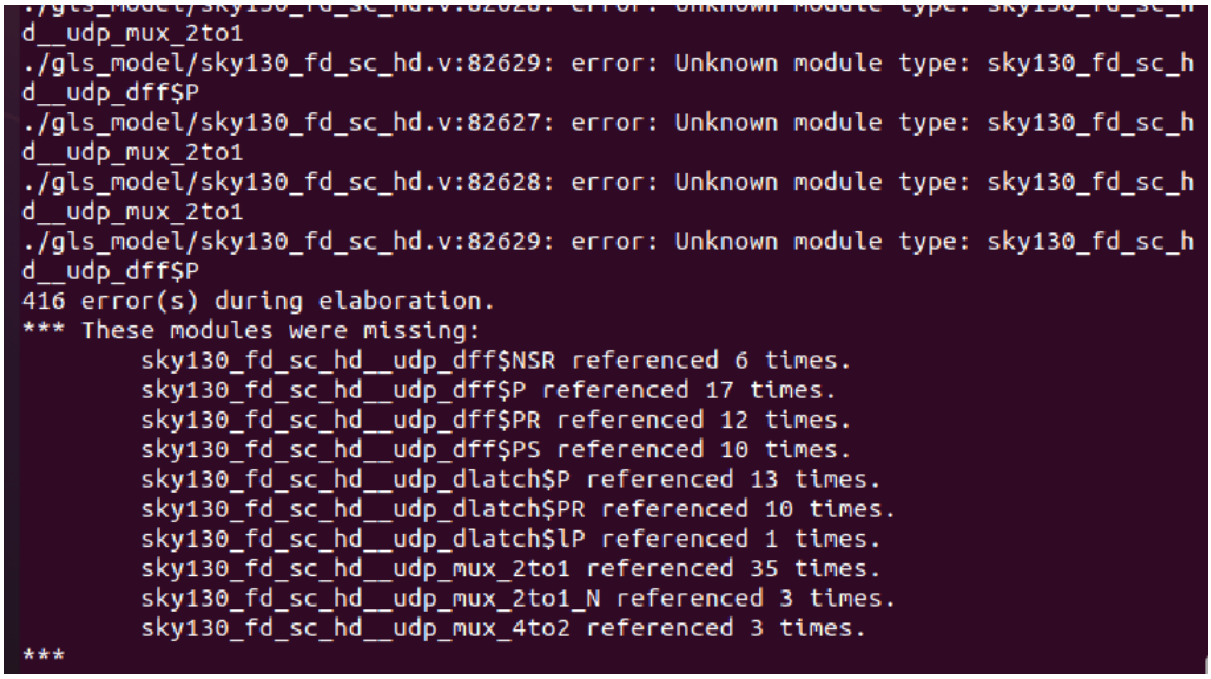
```
yosys> write_verilog -noattr /home/mjcet/VSDBabySoC/VSDBabySoC/output/post_synt
h_sim/vsdbabysoc.synth.v

17. Executing Verilog backend.
Dumping module `\vsdbabysoc'.
```

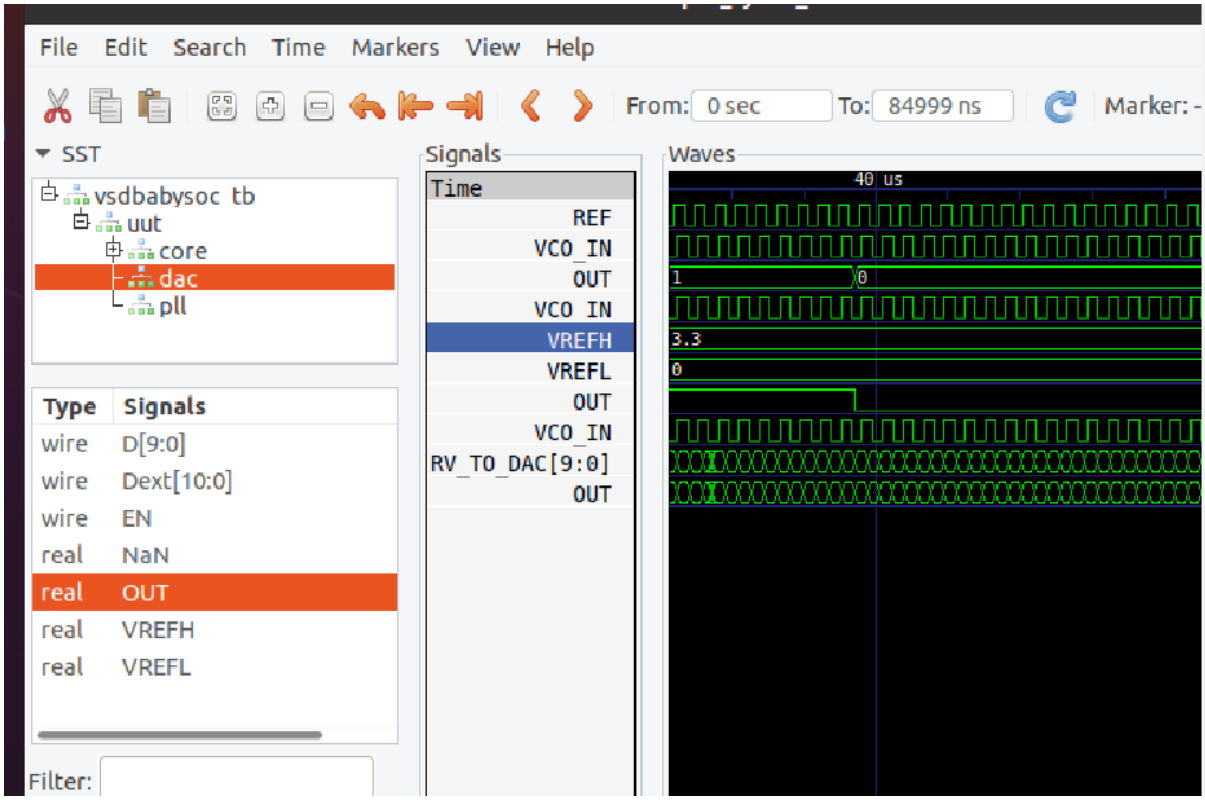
POST Synthesis and Simulation Waveforms of vsdbabysoc.v

Note: Unbale to generate the post_synth_sim.out file

iverilog ../output/synth/vsdbabysoc.synth1.v -DPOST_SYNTH_SIM -DFUNCTIONAL -DUNIT_DELAY=#1 -I ./module/avsddac.v ./module/avsdpll.v -I ./gls_model/primitives.v ./gls_model/sky130_fd_sc_hd.v ./module/testbench.v

Errors in synthesis elaborations




File
Edit
Search
Time
Markers
View
Help
From:
0 sec
To:
84999 ns
Marker: -
SST
vsdbabysoc tb
uut
core
dac
pll
Type
Signals
wire
D[9:0]
wire
Dext[10:0]
wire
EN
real
NaN
real
OUT
real
VREFH
real
VREFL
Filter:
Signals
Time
REF
VCO_IN
OUT
VCO_IN
VREFH
VREFL
OUT
VCO_IN
RV_TO_DAC[9:0]
OUT
Waves
40 us
1
0
3.3
0