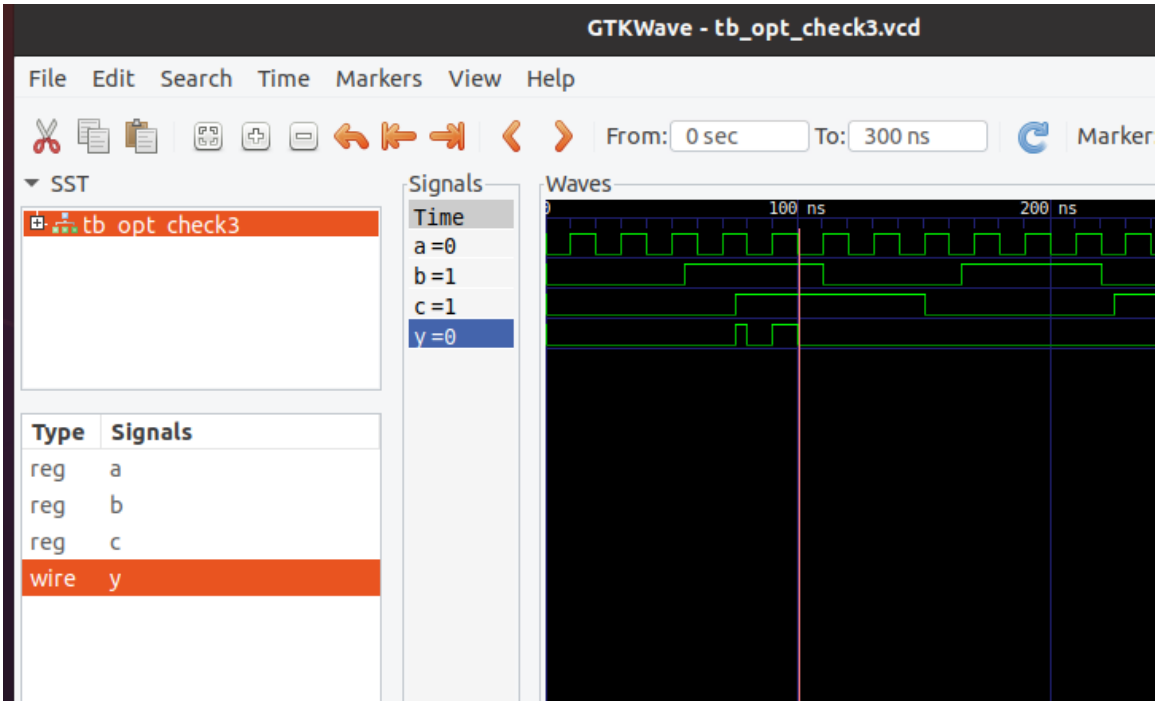
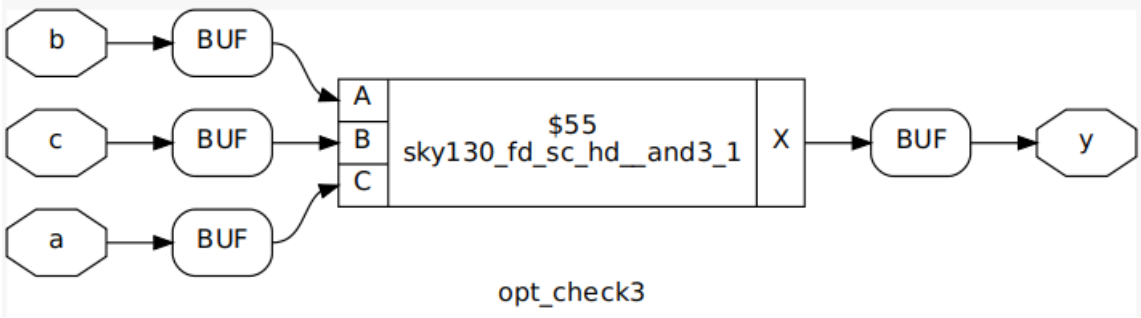
Lab3 opt_check3

```
Time spent: 66% 1x share (0 sec), 17% 2x read_liberty (0 sec), ...
root@raheem:/home/raheem/week1/sky130RTLDesignAndSynthesisWorkshop-main/verilog
_files# iverilog opt_check3.v tb_opt_check3.v
root@raheem:/home/raheem/week1/sky130RTLDesignAndSynthesisWorkshop-main/verilog
_files# ./a.out
VCD info: dumpfile tb_opt_check3.vcd opened for output.
root@raheem:/home/raheem/week1/sky130RTLDesignAndSynthesisWorkshop-main/verilog
_files# gtkwave tb_opt_check3.vcd
Gtk-Message: 15:47:54.850: Failed to load module "canberra-gtk-module"

GTKWave Analyzer v3.3.103 (w)1999-2019 BSI
```



```
3.25.2. Analyzing design hierarchy..
Top module:  \opt_check3
Removed 0 unused modules.

3.26. Printing statistics.

=== opt_check3 ===

   Number of wires:                 5
   Number of wire bits:             5
   Number of public wires:          4
   Number of public wire bits:      4
   Number of memories:              0
   Number of memory bits:           0
   Number of processes:             0
   Number of cells:                 2
     $_ANDNOT_                      1
     $_NAND_                        1

3.27. Executing CHECK pass (checking for obvious problems).
checking module opt_check3..
found and reported 0 problems.
```

```
ABC: + &put
ABC: + write_blif <abc-temp-dir>/output.blif

4.1.2. Re-integrating ABC results.
ABC RESULTS:   sky130_fd_sc_hd__and3_1 cells:        1
ABC RESULTS:        internal signals:        1
ABC RESULTS:           input signals:        3
ABC RESULTS:          output signals:        1
Removing temp directory.

yosys>
```



opt_check3