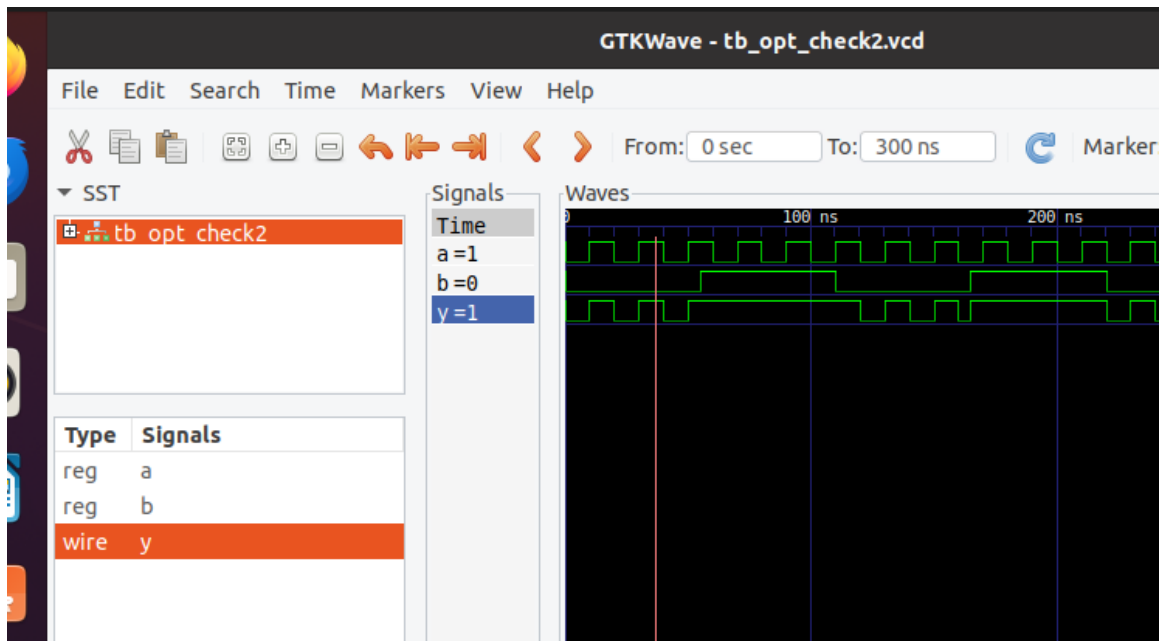


Lab2 Opt_check2.v

```
_files#  
root@raheem:/home/raheem/week1/sky130RTLDesignAndSynthesisWorkshop-main/verilog  
_files# iverilog opt_check2.v tb_opt_check2.v  
root@raheem:/home/raheem/week1/sky130RTLDesignAndSynthesisWorkshop-main/verilog  
_files# ./a.out  
VCD info: dumpfile tb_opt_check2.vcd opened for output.  
root@raheem:/home/raheem/week1/sky130RTLDesignAndSynthesisWorkshop-main/verilog  
_files# gtkwave tb_opt_check2.v  
Gtk-Message: 15:44:13.333: Failed to load module "canberra-gtk-module"  
  
GTKWave Analyzer v3.3.103 (w)1999-2019 BSI
```



3.25.2. Analyzing design hierarchy..

Top module: \opt_check2

Removed 0 unused modules.

3.26. Printing statistics.

=== opt_check2 ===

Number of wires:	3
Number of wire bits:	3
Number of public wires:	3
Number of public wire bits:	3
Number of memories:	0
Number of memory bits:	0
Number of processes:	0
Number of cells:	1
\$_OR_	1

3.27. Executing CHECK pass (checking for obvious problems).

checking module opt_check2..

found and reported 0 problems.

ABC: + apbc

ABC: + write_blif <abc-temp-dir>/output.blif

4.1.2. Re-integrating ABC results.

ABC RESULTS: sky130_fd_sc_hd__or2_0 cells: 1

ABC RESULTS: internal signals: 0

ABC RESULTS: input signals: 2

ABC RESULTS: output signals: 1

Removing temp directory.

vosys>

