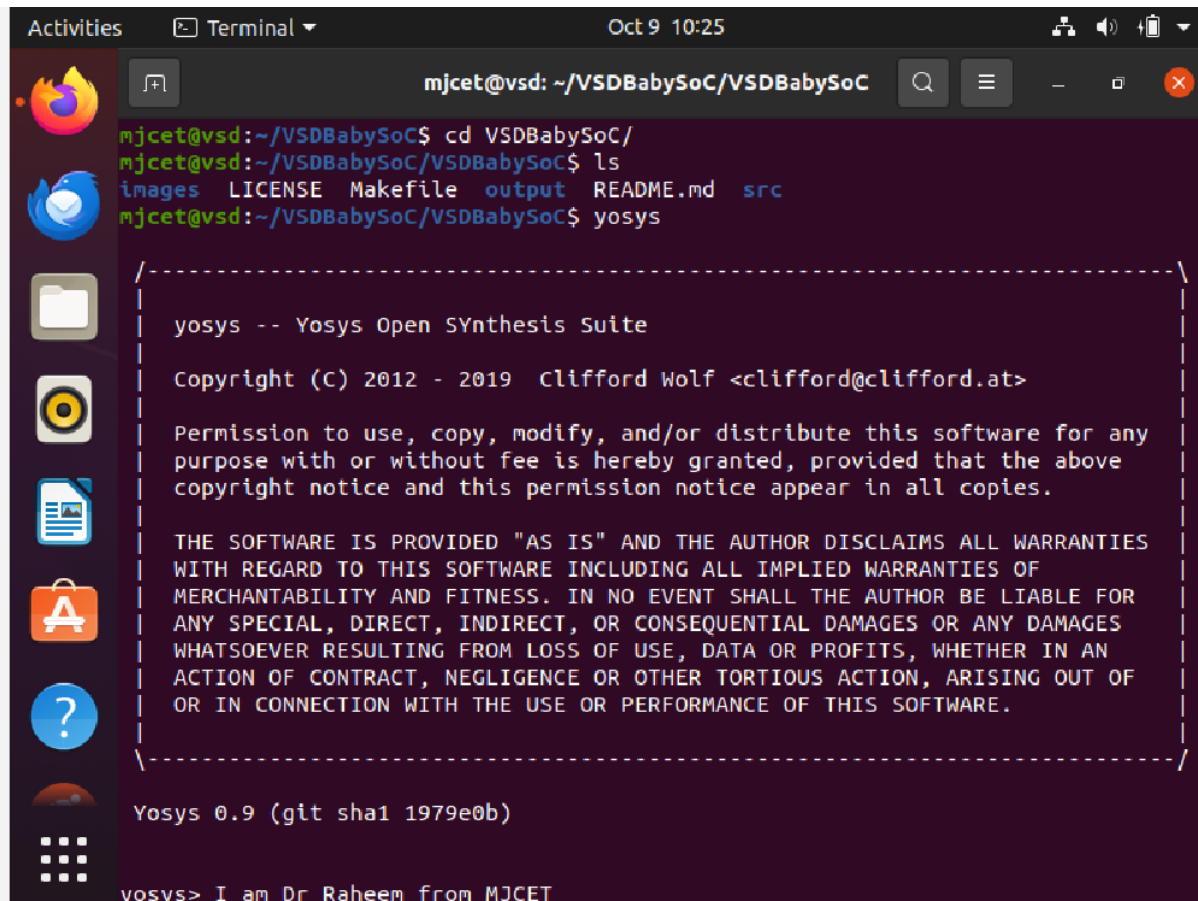


Steps for the Week 3 Assignment of Gate-Level-Synthesis and Functional Simulation

Level I

Step1 Open the synthesis tool Yosys



```
mjcet@vsd: ~/VSDBabySoC/VSDBabySoC
mjcet@vsd:~/VSDBabySoC$ cd VSDBabySoC/
mjcet@vsd:~/VSDBabySoC/VSDBabySoC$ ls
images LICENSE Makefile output README.md src
mjcet@vsd:~/VSDBabySoC/VSDBabySoC$ yosys

-----
yosys -- Yosys Open SYnthesis Suite

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WHATSOEVER RESULTING FROM LOSS OF USE, DATA OR PROFITS, WHETHER IN AN
ACTION OF CONTRACT, NEGLIGENCE OR OTHER TORTIOUS ACTION, ARISING OUT OF
OR IN CONNECTION WITH THE USE OR PERFORMANCE OF THIS SOFTWARE.
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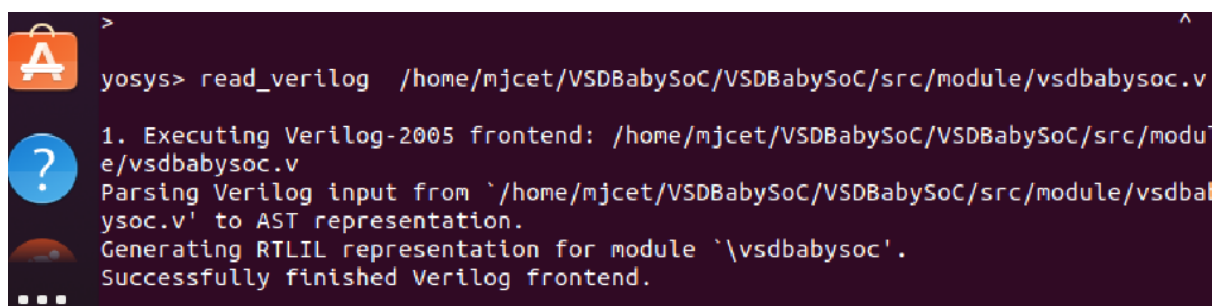
Yosys 0.9 (git sha1 1979e0b)

yosys> I am Dr Raheem from MJCET
```

Load the Top-Level and other Verilog files

Step 2 : Read_verilog

/home/mjcet/VSDBabySoC/VSDBabySoC/src/module/vsdbabysoc.v



```
yosys> read_verilog /home/mjcet/VSDBabySoC/VSDBabySoC/src/module/vsdbabysoc.v

1. Executing Verilog-2005 frontend: /home/mjcet/VSDBabySoC/VSDBabySoC/src/module/vsdbabysoc.v
Parsing Verilog input from `/home/mjcet/VSDBabySoC/VSDBabySoC/src/module/vsdbabysoc.v' to AST representation.
Generating RTLIL representation for module `vsdbabysoc'.
Successfully finished Verilog frontend.
```

Step 3. Read_verilog -I path/Include rvmyth.v

```
yosys> read_verilog -I /home/mjcet/VSDBabySoC/VSDBabySoC/src/include /home/mjcet/VSDBabySoC/VSDBabySoC/src/module/rvmyth.v

2. Executing Verilog-2005 frontend: /home/mjcet/VSDBabySoC/VSDBabySoC/src/module/rvmyth.v
Parsing Verilog input from `/home/mjcet/VSDBabySoC/VSDBabySoC/src/module/rvmyth.v' to AST representation.
Generating RTLIL representation for module `rvmyth'.
Warning: Replacing memory \CPU_Xreg_value_a5 with list of registers. See rvmyth_gen.v:696
Warning: Replacing memory \CPU_Xreg_value_a4 with list of registers. See rvmyth_gen.v:695
Warning: Replacing memory \CPU_Dmem_value_a5 with list of registers. See rvmyth_gen.v:686
Successfully finished Verilog frontend.
```

Step 4. read_verilog -I pathclk_gen.v

```
3. Executing Verilog-2005 frontend: /home/mjcet/VSDBabySoC/VSDBabySoC/src/module/clk_gate.v
Parsing Verilog input from `/home/mjcet/VSDBabySoC/VSDBabySoC/src/module/clk_gate.v' to AST representation.
Generating RTLIL representation for module `clk_gate'.
Successfully finished Verilog frontend.
```

```
3. Executing Verilog-2005 frontend: /home/mjcet/VSDBabySoC/VSDBabySoC/src/module/clk_gate.v
Parsing Verilog input from `/home/mjcet/VSDBabySoC/VSDBabySoC/src/module/clk_gate.v' to AST representation.
Generating RTLIL representation for module `clk_gate'.
Successfully finished Verilog frontend.
```

Level II

Load the library files

```
yosys> read_liberty -lib /home/mjcet/VSDBabySoC/VSDBabySoC/src/lib/avsdpll.lib

4. Executing Liberty frontend.
Imported 1 cell types from liberty file.

yosys> read_liberty -lib /home/mjcet/VSDBabySoC/VSDBabySoC/src/lib/avsdac.lib

5. Executing Liberty frontend.
Imported 1 cell types from liberty file.

yosys> read_liberty -lib /home/mjcet/VSDBabySoC/VSDBabySoC/src/lib/sky130_fd_sc_hd__tt_025C_1v80.lib

6. Executing Liberty frontend.
Imported 428 cell types from liberty file.

yosys> t am Dr Raheem
```

Level III

Synth -top vsdbabysoc.v

```
yosys> synth -top vsdbabysoc

7. Executing SYNTH pass.

7.1. Executing HIERARCHY pass (managing design hierarchy).

7.1.1. Analyzing design hierarchy..
Top module: \vsdbabysoc
Used module: \rvmyth
Used module: \clk_gate

7.1.2. Analyzing design hierarchy..
Top module: \vsdbabysoc
Used module: \rvmyth
Used module: \clk_gate
Removed 0 unused modules.
Mapping positional arguments of cell rvmyth.gen_clkP_CPU_rs2_valid_a2 (clk_gate
).
Mapping positional arguments of cell rvmyth.gen_clkP_CPU_rs1_valid_a2 (clk_gate
).
Mapping positional arguments of cell rvmyth.gen_clkP_CPU_rd_valid_a5 (clk_gate)
```

```
7.25.2. Analyzing design hierarchy..
Top module: \vsdbabysoc
Used module: \rvmyth
Used module: \clk_gate
Removed 0 unused modules.

7.26. Printing statistics.

=== clk_gate ===

Number of wires: 5
Number of wire bits: 5
Number of public wires: 5
Number of public wire bits: 5
Number of memories: 0
Number of memory bits: 0
Number of processes: 0
Number of cells: 0
```

```
mjcet@vsd: ~/VSDBabySoC/VSDBab... x root@  
=== rvmyth ===  
  
Number of wires: 4663  
Number of wire bits: 8290  
Number of public wires: 267  
Number of public wire bits: 3894  
Number of memories: 0  
Number of memory bits: 0  
Number of processes: 0  
Number of cells: 6849  
  $_ANDNOT_ 1180  
  $_AND_ 59  
  $_AOI3_ 104  
  $_AOI4_ 153  
  $_DFF_P_ 1273  
  $_MUX_ 1456  
  $_NAND_ 84  
  $_NOR_ 92  
  $_NOT_ 964  
  $_OAI3_ 168  
  $_OAI4_ 387  
  $_ORNOT_ 62  
  $_OR_ 666  
  $_XNOR_ 80  
  $_XOR_ 114  
  clk_gate 7
```

```
mjcet@vsd: ~/VSDBabySoC/VSDBab... x root@vsd:~$ yosys -i -p vsdbabysoc.yosys -s vsdbabysoc.yosys

=== vsdbabysoc ===

Number of wires:          9
Number of wire bits:      18
Number of public wires:   9
Number of public wire bits: 18
Number of memories:       0
Number of memory bits:    0
Number of processes:      0
Number of cells:          3
    avsdac                1
    avsdpll                1
    rvmyth                 1

=== design hierarchy ===

vsdbabysoc                1
    rvmyth                 1
        clk_gate           7

Number of wires:          4707
Number of wire bits:      8343
Number of public wires:   311
Number of public wire bits: 3947
Number of memories:       0
Number of memory bits:    0
Number of processes:      0
```

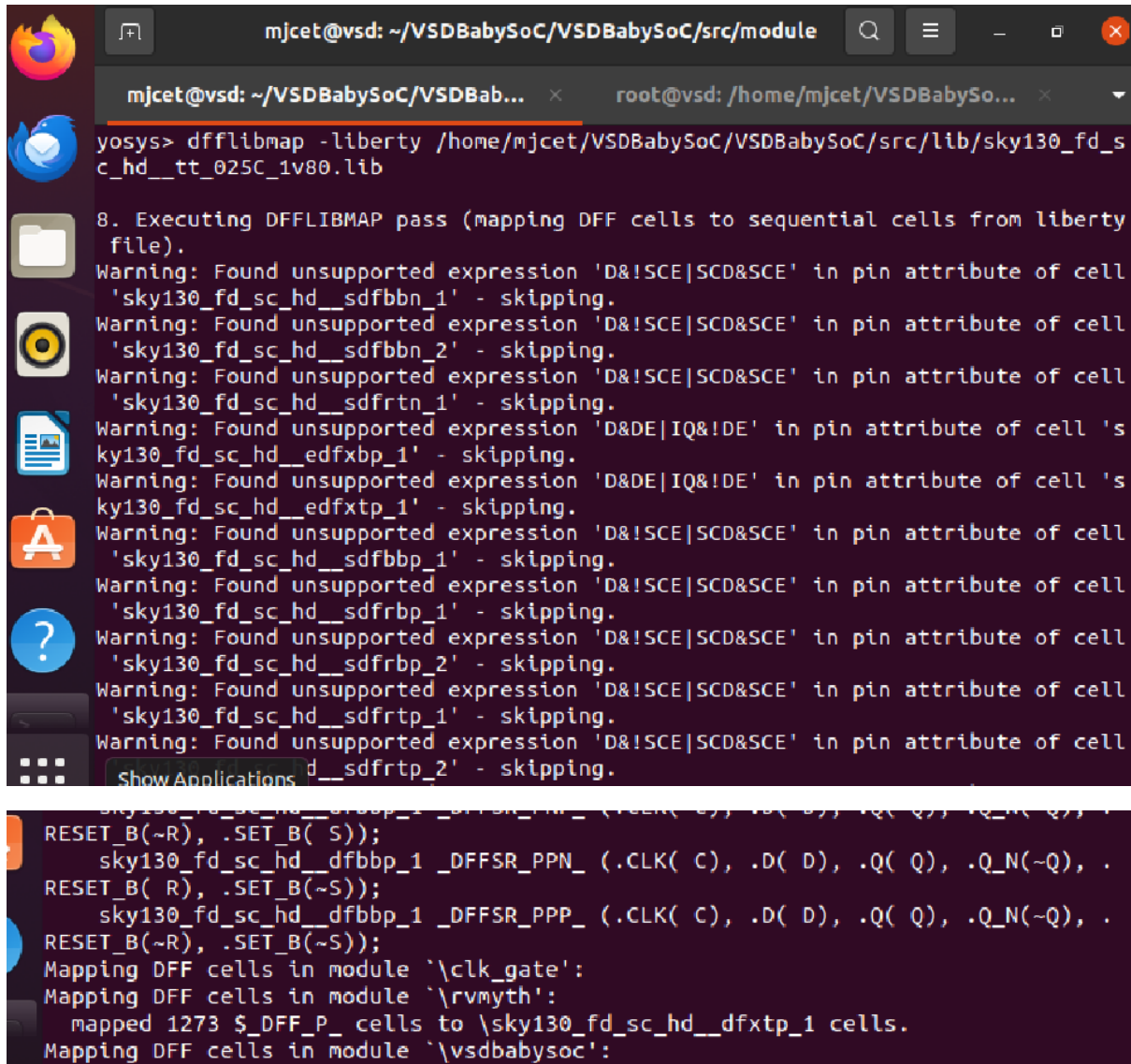
```
7.27. Executing CHECK pass (checking for obvious problems).
checking module clk_gate..
checking module rvmyth..
checking module vsdbabysoc..
found and reported 0 problems.

yosys> i am Dr Raheem
```

Level IV

D Flip-Flop to Standard Cells

Dfflibmap -liberty



```
mjcet@vsd: ~/VSDBabySoC/VSDBabySoC/src/module
yosys> dfflibmap -liberty /home/mjcet/VSDBabySoC/VSDBabySoC/src/lib/sky130_fd_sc_hd_tt_025C_1v80.lib

8. Executing DFFLIBMAP pass (mapping DFF cells to sequential cells from liberty file).
Warning: Found unsupported expression 'D&!SCE|SCD&SCE' in pin attribute of cell 'sky130_fd_sc_hd__sdfbnn_1' - skipping.
Warning: Found unsupported expression 'D&!SCE|SCD&SCE' in pin attribute of cell 'sky130_fd_sc_hd__sdfbnn_2' - skipping.
Warning: Found unsupported expression 'D&!SCE|SCD&SCE' in pin attribute of cell 'sky130_fd_sc_hd__sdftrn_1' - skipping.
Warning: Found unsupported expression 'D&DE|IQ&!DE' in pin attribute of cell 'sky130_fd_sc_hd__edfxbp_1' - skipping.
Warning: Found unsupported expression 'D&DE|IQ&!DE' in pin attribute of cell 'sky130_fd_sc_hd__edfxtp_1' - skipping.
Warning: Found unsupported expression 'D&!SCE|SCD&SCE' in pin attribute of cell 'sky130_fd_sc_hd__sdfbbp_1' - skipping.
Warning: Found unsupported expression 'D&!SCE|SCD&SCE' in pin attribute of cell 'sky130_fd_sc_hd__sdfrbp_1' - skipping.
Warning: Found unsupported expression 'D&!SCE|SCD&SCE' in pin attribute of cell 'sky130_fd_sc_hd__sdfrbp_2' - skipping.
Warning: Found unsupported expression 'D&!SCE|SCD&SCE' in pin attribute of cell 'sky130_fd_sc_hd__sdfrrp_1' - skipping.
Warning: Found unsupported expression 'D&!SCE|SCD&SCE' in pin attribute of cell 'sky130_fd_sc_hd__sdfrrp_2' - skipping.

sky130_fd_sc_hd__dfbnn_1 _DFFSR_PPN_ (.CLK( C), .D( D), .Q( Q), .Q_N(~Q), .RESET_B(~R), .SET_B( S));
sky130_fd_sc_hd__dfbnn_1 _DFFSR_PPN_ (.CLK( C), .D( D), .Q( Q), .Q_N(~Q), .RESET_B( R), .SET_B(~S));
sky130_fd_sc_hd__dfbnn_1 _DFFSR_PPN_ (.CLK( C), .D( D), .Q( Q), .Q_N(~Q), .RESET_B(~R), .SET_B(~S));
Mapping DFF cells in module '\clk_gate':
Mapping DFF cells in module '\rvmyth':
mapped 1273 $_DFF_P_ cells to \sky130_fd_sc_hd__dfxtp_1 cells.
Mapping DFF cells in module '\vsdbabysoc':
```

Level VI

Optimization and Technology Mapping

```
yosys> opt
```

9. Executing OPT pass (performing simple optimizations).

9.1. Executing OPT_EXPR pass (perform const folding).

Optimizing module clk_gate.

Optimizing module rvmyth.

Optimizing module vsdbabysoc.

9.2. Executing OPT_MERGE pass (detect identical cells).

Finding identical cells in module '\clk_gate'.

Finding identical cells in module '\rvmyth'.

Finding identical cells in module '\vsdbabysoc'.

Removed a total of 0 cells.

9.3. Executing OPT_MUXTREE pass (detect dead branches in mux trees).

Running muxtree optimizer on module \clk_gate..

Creating internal representation of mux trees.

No muxes found in this module.

Running muxtree optimizer on module \rvmyth..

Creating internal representation of mux trees.

No muxes found in this module.

Running muxtree optimizer on module \vsdbabysoc..

```
yosys> abc -liberty /home/mjct/VSDBabySoC/VSDBabySoC/src/lib/sky130_fd_sc_hd__tt_025C_1v80.lib
```

10. Executing ABC pass (technology mapping using ABC).

10.1. Extracting gate netlist of module '\clk_gate' to '<abc-temp-dir>/input.blif'..

Extracted 0 gates and 0 wires to a netlist network with 0 inputs and 0 outputs. Don't call ABC as there is nothing to map.

Removing temp directory.

10.2. Extracting gate netlist of module '\rvmyth' to '<abc-temp-dir>/input.blif'..

Extracted 5569 gates and 6794 wires to a netlist network with 1225 inputs and 1173 outputs.

10.2.1. Executing ABC.

Running ABC command: berkeley-abc -s -f <abc-temp-dir>/abc.script 2>&1

ABC: ABC command line: "source <abc-temp-dir>/abc.script".

ABC:

ABC: + read_blif <abc-temp-dir>/input.blif

ABC: + read_lib -w /home/micet/VSDBabySoC/VSDBabySoC/src/lib/sky130_fd_sc_hd__tt_025C_1v80.lib


```
ABC RESULTS: sky130_fd_sc_hd__o32ai_1 cells: 3
ABC RESULTS: sky130_fd_sc_hd__o41a_1 cells: 2
ABC RESULTS: sky130_fd_sc_hd__o41ai_1 cells: 3
ABC RESULTS: sky130_fd_sc_hd__or3_1 cells: 5
ABC RESULTS: sky130_fd_sc_hd__or4_1 cells: 3
ABC RESULTS: sky130_fd_sc_hd__xnor2_1 cells: 87
ABC RESULTS: sky130_fd_sc_hd__xor2_1 cells: 45
ABC RESULTS: internal signals: 4396
ABC RESULTS: input signals: 1225
ABC RESULTS: output signals: 1173
Removing temp directory.

10.3. Extracting gate netlist of module '\vsdbabysoc' to '<abc-temp-dir>/input.blif'..
Extracted 0 gates and 0 wires to a netlist network with 0 inputs and 0 outputs.
Don't call ABC as there is nothing to map.
Removing temp directory.

yosys> i am Dr Raheem
```

Level VII

Perform Final clean-up and renaming

```
yosys> flatten

11. Executing FLATTEN pass (flatten design).
Using template rvmyth for cells of type rvmyth.
Using template clk_gate for cells of type clk_gate.
<suppressed ~8 debug messages>
No more expansions possible.
Deleting now unused module clk_gate.
Deleting now unused module rvmyth.

yosys> setundef -zero

12. Executing SETUNDEF pass (replace undef values with defined constants).

yosys> clean -purge
Removed 393 unused cells and 7107 unused wires.

yosys> rename -enumaerate
ERROR: Invalid number of arguments!

yosys> rename -enumerate
```


Statistics

```
yosys> stat

13. Printing statistics.

=== vsdbabysoc ===

Number of wires:          3181
Number of wire bits:      5579
Number of public wires:   3181
Number of public wire bits: 5579
Number of memories:       0
Number of memory bits:    0
Number of processes:      0
Number of cells:          5233
  avsdac                 1
  avsdpll                 1
  sky130_fd_sc_hd__a211oi_0 3
  sky130_fd_sc_hd__a21io_1  1
  sky130_fd_sc_hd__a21oi_1 352
  sky130_fd_sc_hd__a21boi_0 2
  sky130_fd_sc_hd__a21o_1   11
  sky130_fd_sc_hd__a21oi_1  704
  sky130_fd_sc_hd__a22io_1  13
  sky130_fd_sc_hd__a22oi_1  75
  sky130_fd_sc_hd__a222oi_1 185
  sky130_fd_sc_hd__a22o_1   35
```

Level IX

Synthesis Netlist

```
yosys> write_verilog -noattr /home/mjcet/VSDBabySoC/VSDBabySoC/output/post_synt
h_sim/vsdbabysoc.synth.v

17. Executing Verilog backend.
Dumping module '\vsdbabysoc'.
```

POST Synthesis and Simulation Waveforms of vsdbabysoc.v

Note: Unable to generate the post_synth_sim.out file

```
iverilog ../output/synth/vsdbabysoc.synth1.v -DPOST_SYNTH_SIM -DFUNCTIONAL -  
DUNIT_DELAY=#1 -I ./module/avsddac.v ./module/avsdpll.v -I  
./gls_model/primitives.v ./gls_model/sky130_fd_sc_hd.v ./module/testbench.v
```

Errors in synthesis elaborations

```
./gls_model/sky130_fd_sc_hd.v:82626: error: Unknown module type: sky130_fd_sc_h  
d__udp_mux_2to1  
./gls_model/sky130_fd_sc_hd.v:82629: error: Unknown module type: sky130_fd_sc_h  
d__udp_dff$P  
./gls_model/sky130_fd_sc_hd.v:82627: error: Unknown module type: sky130_fd_sc_h  
d__udp_mux_2to1  
./gls_model/sky130_fd_sc_hd.v:82628: error: Unknown module type: sky130_fd_sc_h  
d__udp_mux_2to1  
./gls_model/sky130_fd_sc_hd.v:82629: error: Unknown module type: sky130_fd_sc_h  
d__udp_dff$P  
416 error(s) during elaboration.  
*** These modules were missing:  
    sky130_fd_sc_hd__udp_dff$NSR referenced 6 times.  
    sky130_fd_sc_hd__udp_dff$P referenced 17 times.  
    sky130_fd_sc_hd__udp_dff$PR referenced 12 times.  
    sky130_fd_sc_hd__udp_dff$PS referenced 10 times.  
    sky130_fd_sc_hd__udp_dlatch$P referenced 13 times.  
    sky130_fd_sc_hd__udp_dlatch$PR referenced 10 times.  
    sky130_fd_sc_hd__udp_dlatch$LP referenced 1 times.  
    sky130_fd_sc_hd__udp_mux_2to1 referenced 35 times.  
    sky130_fd_sc_hd__udp_mux_2to1_N referenced 3 times.  
    sky130_fd_sc_hd__udp_mux_4to2 referenced 3 times.  
***
```

