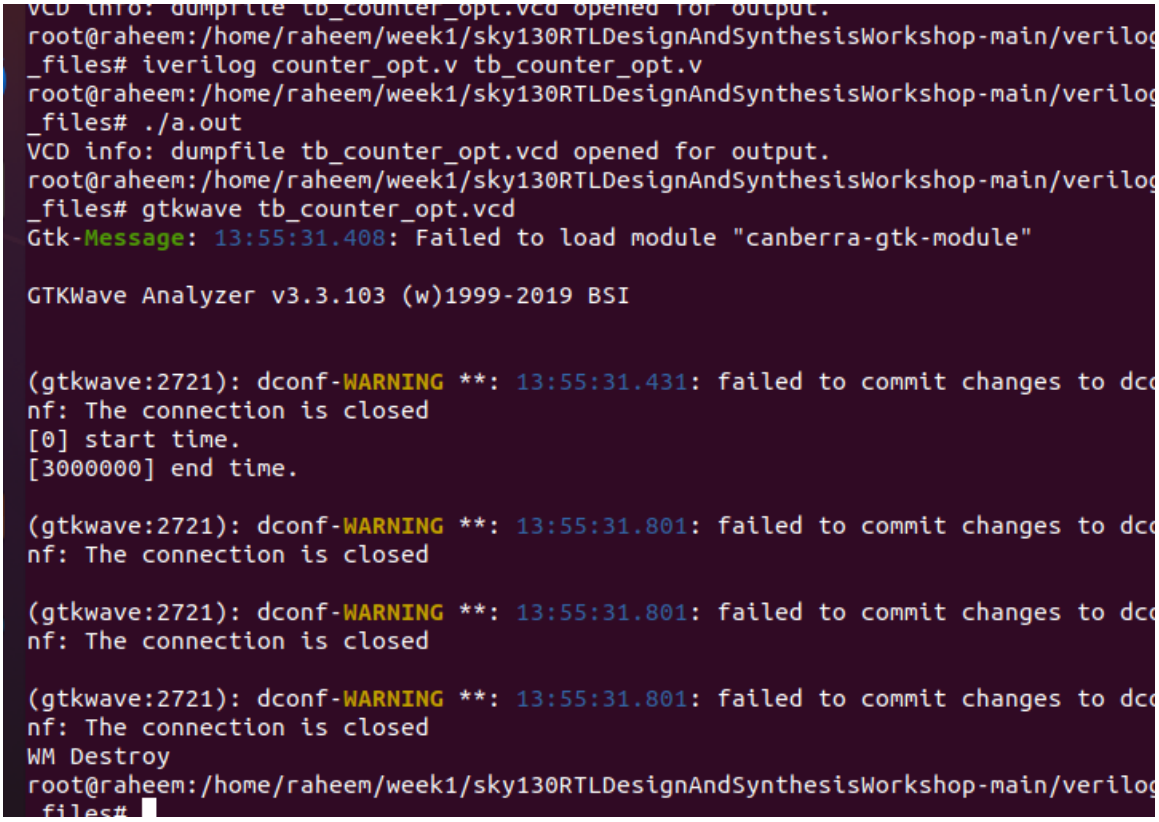
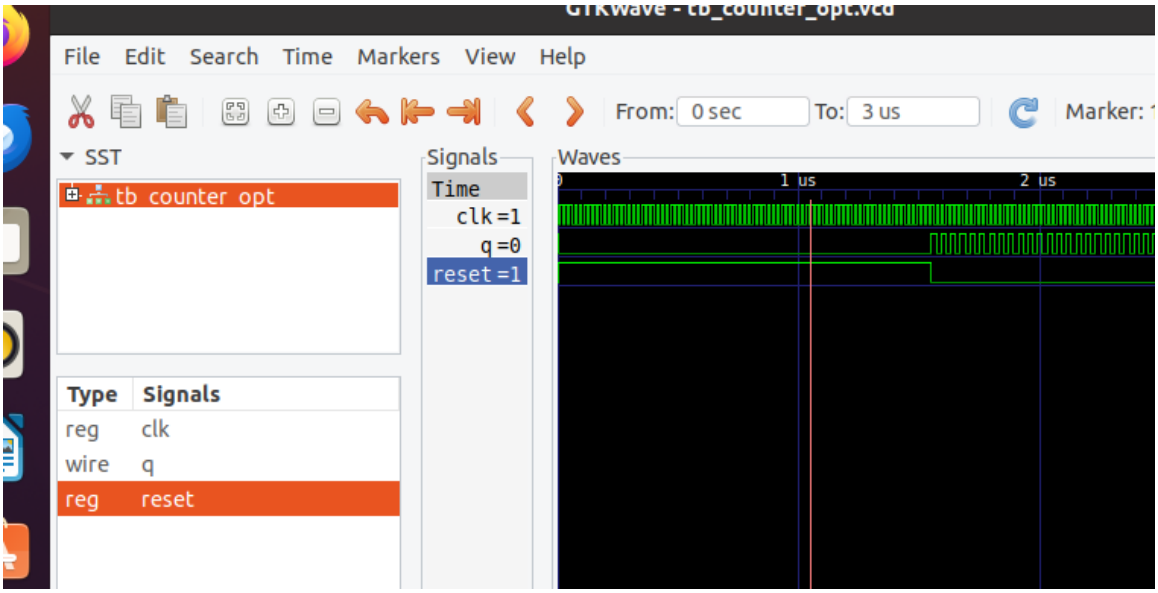
counter_opt .v

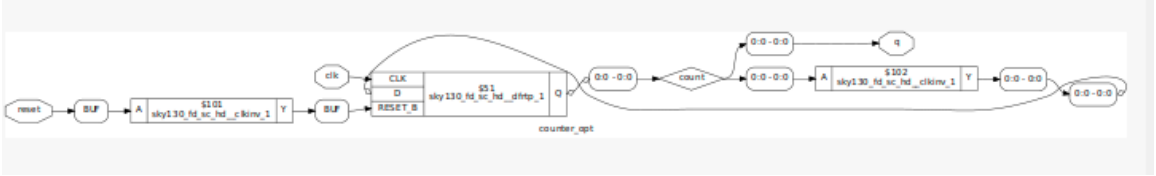





```
3.25.2. Analyzing design hierarchy..
Top module:  \counter_opt
Removed 0 unused modules.

3.26. Printing statistics.

=== counter_opt ===

   Number of wires:                 5
   Number of wire bits:             9
   Number of public wires:          4
   Number of public wire bits:      6
   Number of memories:              0
   Number of memory bits:           0
   Number of processes:             0
   Number of cells:                 2
     $_DFF_PP0_                     1
     $_NOT_                         1

3.27. Executing CHECK pass (checking for obvious problems).
checking module counter_opt..
found and reported 0 problems.
```

```
));
    sky130_fd_sc_hd__dfrtp_1 _DFF_PN0_ (.CLK( C), .D( D), .Q( Q), .RESET_B(
;
    sky130_fd_sc_hd__dfstp_2 _DFF_PN1_ (.CLK( C), .D( D), .Q( Q), .SET_B( R)
    sky130_fd_sc_hd__dfrtp_1 _DFF_PP0_ (.CLK( C), .D( D), .Q( Q), .RESET_B(~
;
    sky130_fd_sc_hd__dfstp_2 _DFF_PP1_ (.CLK( C), .D( D), .Q( Q), .SET_B(~R)
    sky130_fd_sc_hd__dfbbn_1 _DFFSR_NNN_ (.CLK_N( C), .D( D), .Q( Q), .Q_N(~
 .RESET_B( R), .SET_B( S));
    sky130_fd_sc_hd__dfbbn_1 _DFFSR_NNP_ (.CLK_N( C), .D( D), .Q( Q), .Q_N(~
 .RESET_B(~R), .SET_B( S));
    sky130_fd_sc_hd__dfbbn_1 _DFFSR_NPN_ (.CLK_N( C), .D( D), .Q( Q), .Q_N(~
 .RESET_B( R), .SET_B(~S));
    sky130_fd_sc_hd__dfbbn_1 _DFFSR_NPP_ (.CLK_N( C), .D( D), .Q( Q), .Q_N(~
 .RESET_B(~R), .SET_B(~S));
    sky130_fd_sc_hd__dfbbp_1 _DFFSR_PNN_ (.CLK( C), .D( D), .Q( Q), .Q_N(~Q)
RESET_B( R), .SET_B( S));
    sky130_fd_sc_hd__dfbbp_1 _DFFSR_PNP_ (.CLK( C), .D( D), .Q( Q), .Q_N(~Q)
RESET_B(~R), .SET_B( S));
    sky130_fd_sc_hd__dfbbp_1 _DFFSR_PPN_ (.CLK( C), .D( D), .Q( Q), .Q_N(~Q)
RESET_B( R), .SET_B(~S));
    sky130_fd_sc_hd__dfbbp_1 _DFFSR_PPP_ (.CLK( C), .D( D), .Q( Q), .Q_N(~Q)
RESET_B(~R), .SET_B(~S));
Mapping DFF cells in module `\counter_opt':
  mapped 1 $_DFF_PP0_ cells to \sky130_fd_sc_hd__dfrtp_1 cells.

yosys> abc -libverty ../lib//sky130_fd_sc_hd__tt_025C_1v80.lib
```

```
ABC: + &dch -f
ABC: + &nf
ABC: + &put
ABC: + write_blif <abc-temp-dir>/output.blif

6.1.2. Re-integrating ABC results.
ABC RESULTS:   sky130_fd_sc_hd__clkinv_1 cells:        2
ABC RESULTS:        internal signals:        0
ABC RESULTS:           input signals:        2
ABC RESULTS:          output signals:        2
Removing temp directory.
```

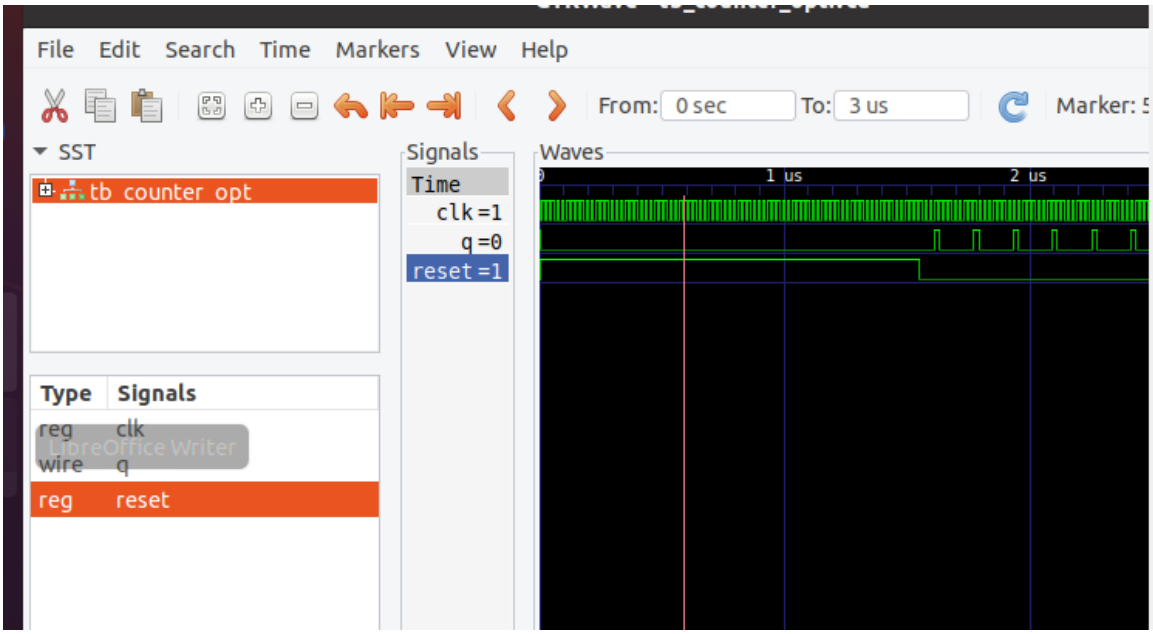


Counter_opt2.v

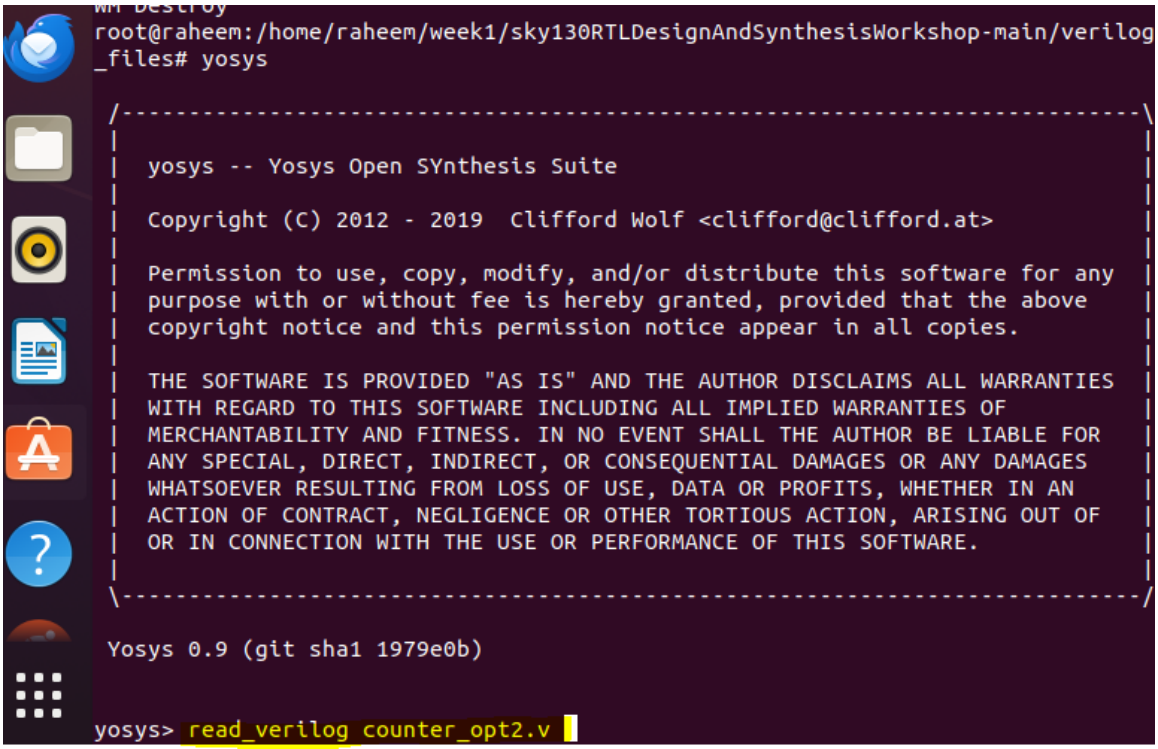
```
_files# ls *coun*
bad_counter.v    good_counter.v     tb_counter_opt.v     tb_ripple_counter.v
counter_opt2.v   ripple_counter.v   tb_counter_opt.vcd
counter_opt.v    tb_bad_counter.v   tb_good_counter.v
root@raheem:/home/raheem/week1/sky130RTLDesignAndSynthesisWorkshop-main/verilog
_files# iverilog counter_opt2.v tb_counter_opt.v
```

./a.out

gtkwave tb_counter_opt.vcd



counter_opt2.v synthesis


root@raheem:/home/raheem/week1/sky130RTLDesignAndSynthesisWorkshop-main/verilog_files# yosys
yosys -- Yosys Open SYnthesis Suite
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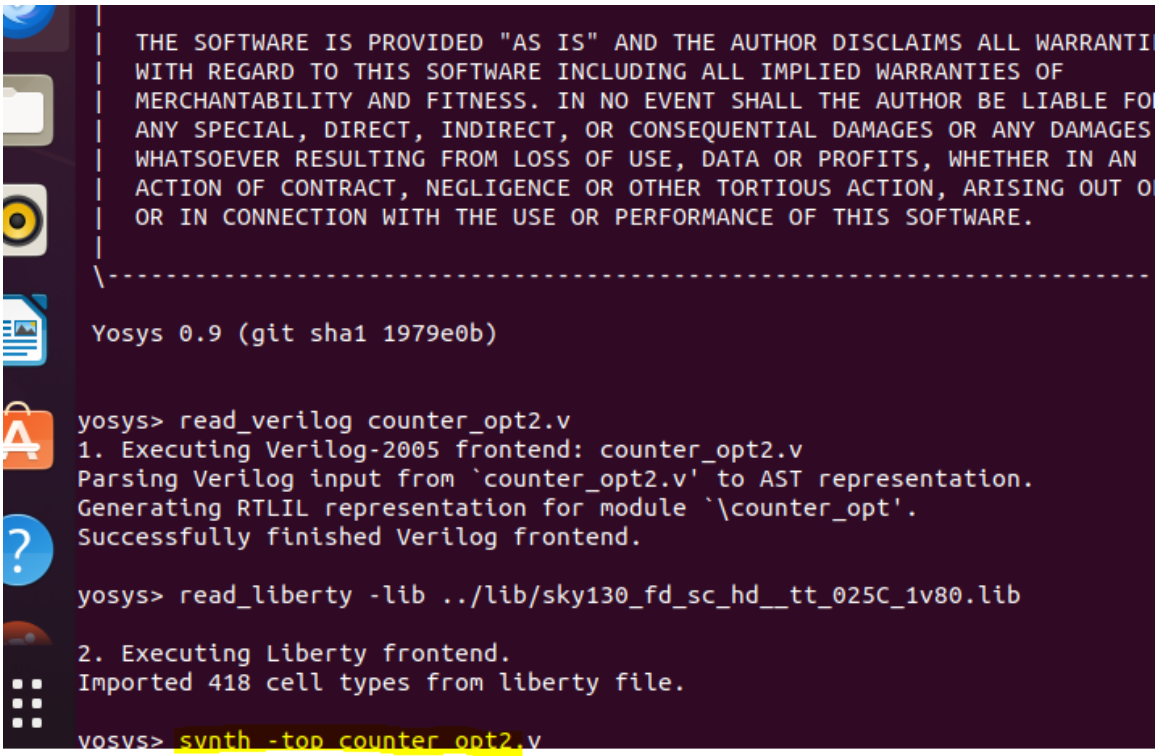
Yosys 0.9 (git sha1 1979e0b)
yosys> read_verilog counter_opt2.v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ACTION OF CONTRACT, NEGLIGENCE OR OTHER TORTIOUS ACTION, ARISING OUT O
OR IN CONNECTION WITH THE USE OR PERFORMANCE OF THIS SOFTWARE.
Yosys 0.9 (git sha1 1979e0b)
yosys> read_verilog counter_opt2.v
1. Executing Verilog-2005 frontend: counter_opt2.v
Parsing Verilog input from `counter_opt2.v' to AST representation.
Generating RTLIL representation for module `\counter_opt'.
Successfully finished Verilog frontend.
yosys> read_liberty -lib ../lib/sky130_fd_sc_hd__tt_025C_1v80.lib
2. Executing Liberty frontend.
Imported 418 cell types from liberty file.
yosys> synth -top counter_opt2.v

```
Top module:  \counter_opt
Removed 0 unused modules.

6.26. Printing statistics.

=== counter_opt ===

   Number of wires:                 7
   Number of wire bits:            11
   Number of public wires:          4
   Number of public wire bits:      6
   Number of memories:              0
   Number of memory bits:           0
   Number of processes:             0
   Number of cells:                 9
     $_ANDNOT_                      1
     $_AND_                         1
     $_DFF_PP0_                     3
     $_NOT_                         1
     $_OR_                          1
     $_XOR_                         2

6.27. Executing CHECK pass (checking for obvious problems).
checking module counter_opt..
found and reported 0 problems.
```

```
8.1.2. Re-integrating ABC results.
ABC RESULTS:   sky130_fd_sc_hd__clkinv_1 cells:        4
ABC RESULTS:   sky130_fd_sc_hd__nand2_1 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__nor3b_1 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__xnor2_1 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__xor2_1 cells:         1
ABC RESULTS:        internal signals:        2
ABC RESULTS:           input signals:        4
ABC RESULTS:          output signals:        7
Removing temp directory.

yosys> show
```