Rvmyth

The rvmyth module is a simple RISC-V based processor. It outputs a 10-bit digital signal (OUT) to be converted by the DAC.
[rvmyth](https://github.com/kunalg123/rvmyth/)

Inputs:

- CLK: Clock signal generated by the PLL.

- reset: Initializes or resets the processor.

Outputs:

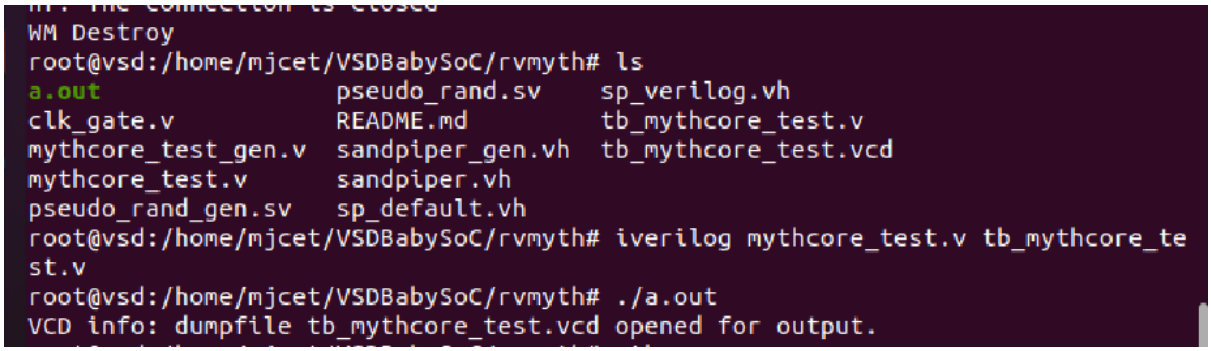
- OUT: A 10-bit digital signal representing processed data to be sent to the DAC.

Tools needed to simulate rvmyth

1. iverilog
2. gtkwave

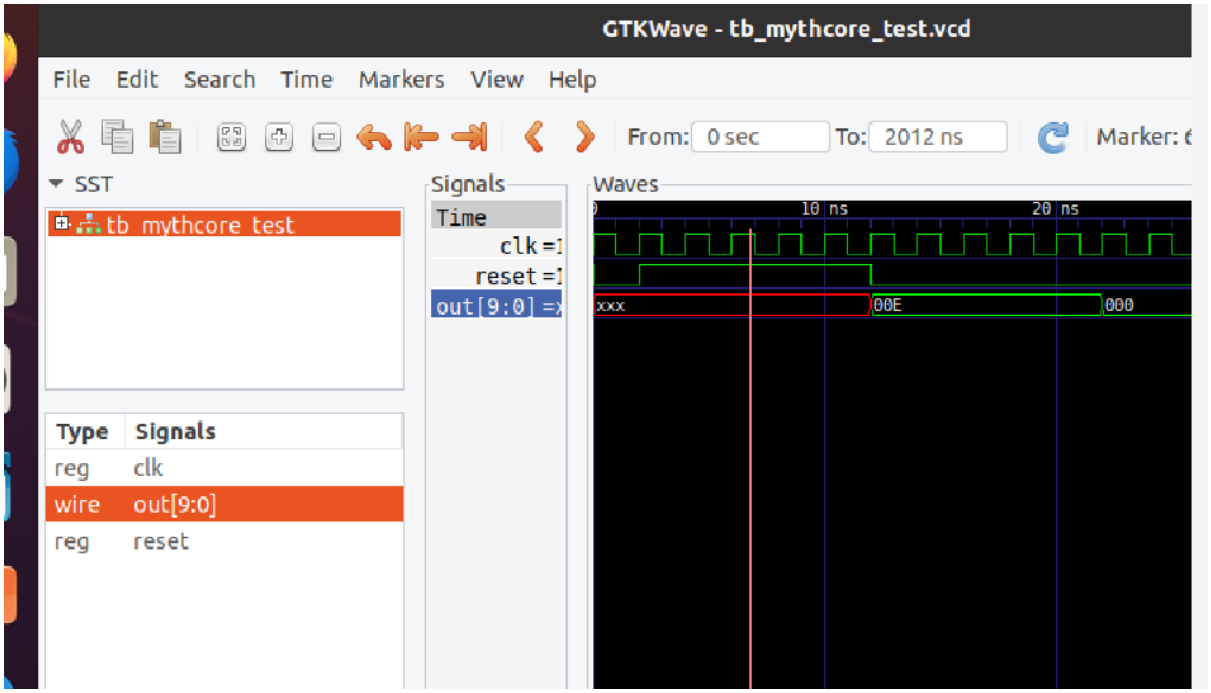
Steps to simulate rvmyth

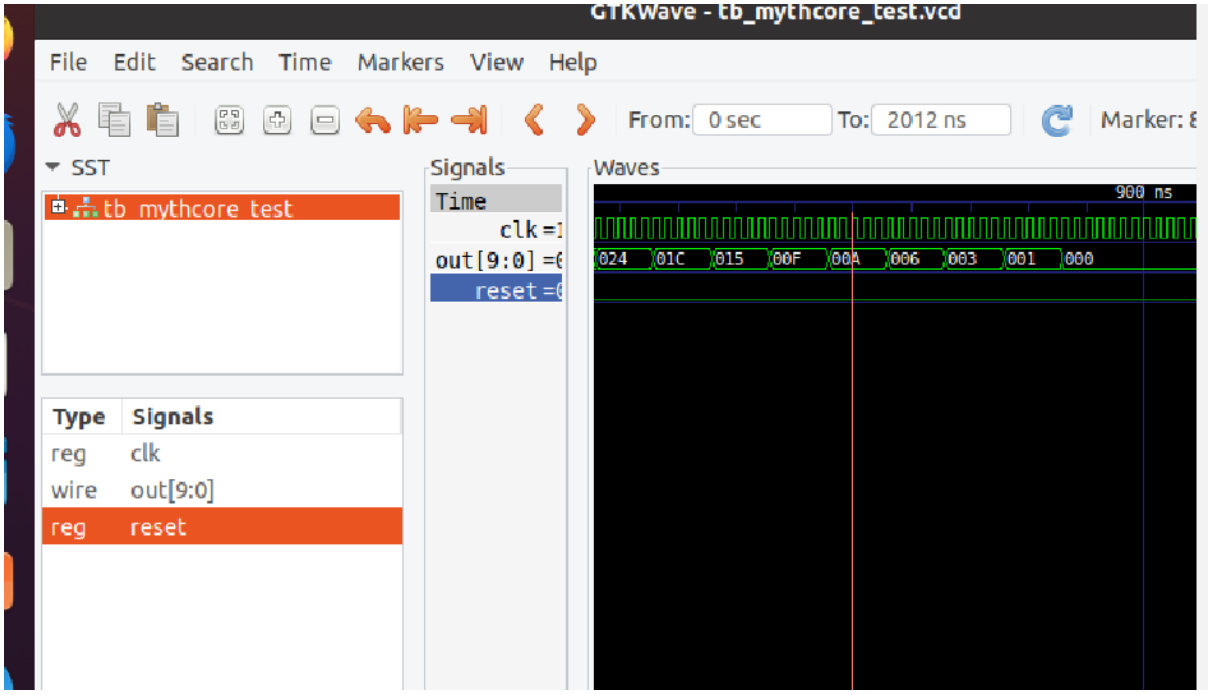
1. git clone https://github.com/kunalg123/rvmyth/
2. cd rvmyth
3. iverilog mythcore_test.v tb_mythcore_test.v
4. ./a.out
5. gtkwave tb_mythcore_test.vcd

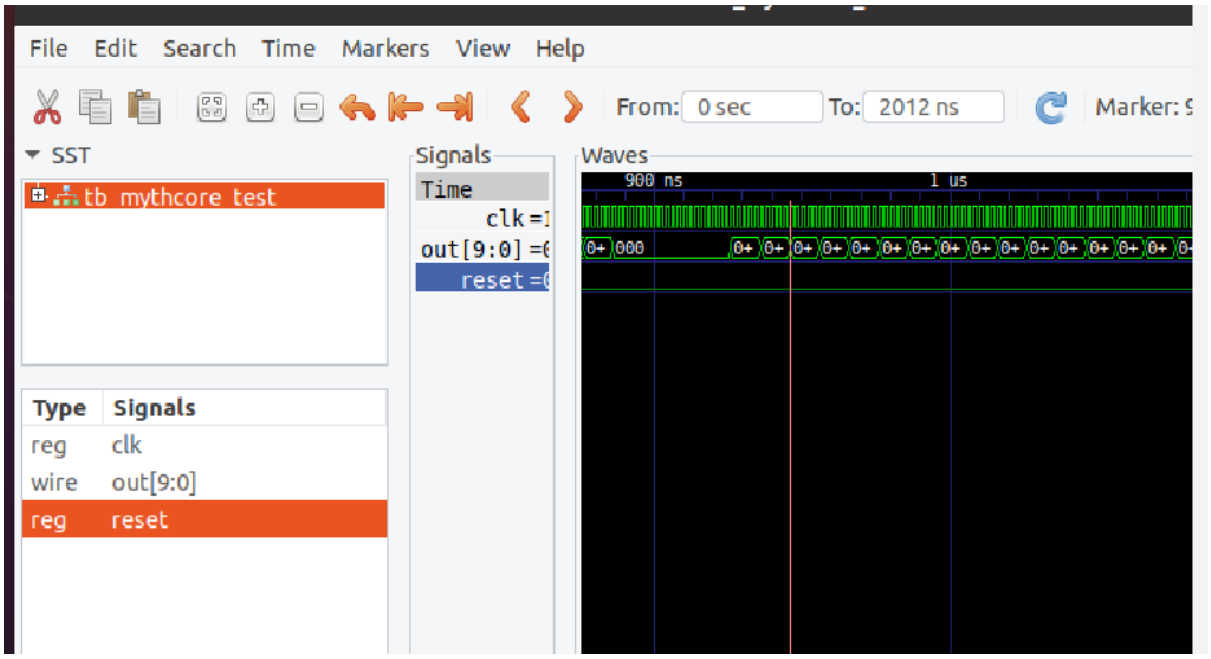


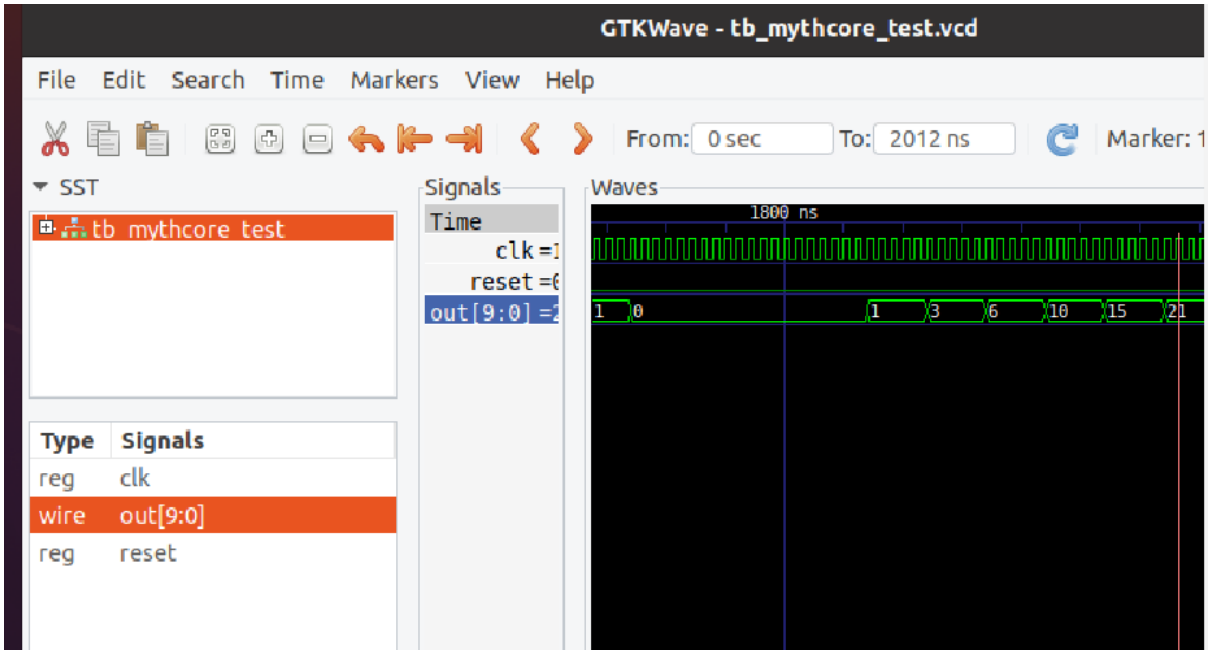
```
root@vsd:/home/mjcet/VSDBabySoC# ls
images  LICENSE  Makefile  output  README.md  rvmyth  src
root@vsd:/home/mjcet/VSDBabySoC# cd rvmyth
root@vsd:/home/mjcet/VSDBabySoC/rvmyth# iverilog mythcore_test.v tb_mythcore_te
st.v
root@vsd:/home/mjcet/VSDBabySoC/rvmyth# ./a.out
VCD info: dumpfile tb_mythcore_test.vcd opened for output.
root@vsd:/home/mjcet/VSDBabySoC/rvmyth# gtkwave tb_mythcore_test.vcd
```

Reset =1 output is undefined




GTKWave - tb_mythcore_test.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 2012 ns
SST
tb_mythcore_test
Signals
Time
clk
out[9:0]
reset
Waves
900 ns
024 01C 015 00F 00A 006 003 001 000
Type Signals
reg clk
wire out[9:0]
reg reset


File Edit Search Time Markers View Help
From: 0 sec
To: 2012 ns
SST
tb_mythcore_test
Signals
Time
clk
out[9:0]
reset
Waves
900 ns
1 us
0+ 000
Type Signals
reg clk
wire out[9:0]
reg reset



Inputs

CLK clock signal is generated form the PLL RESET is initialize the processor

Outputs:

OUT: 10 bit Digital Signal Processing data processed