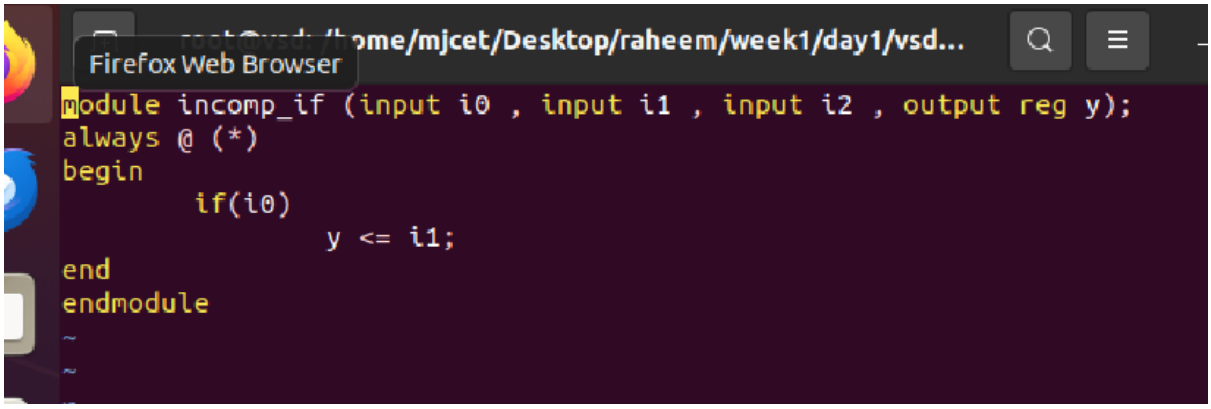
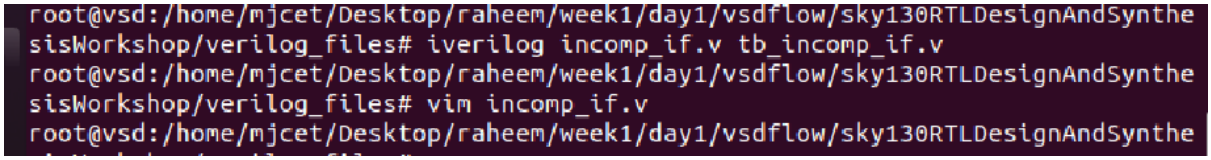
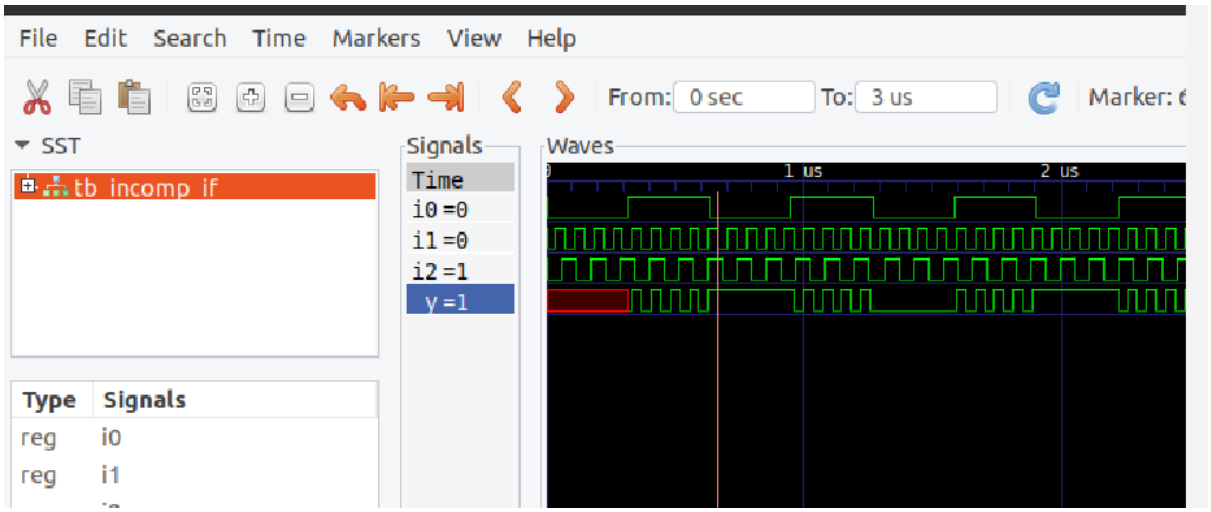
Incomp_if Statement

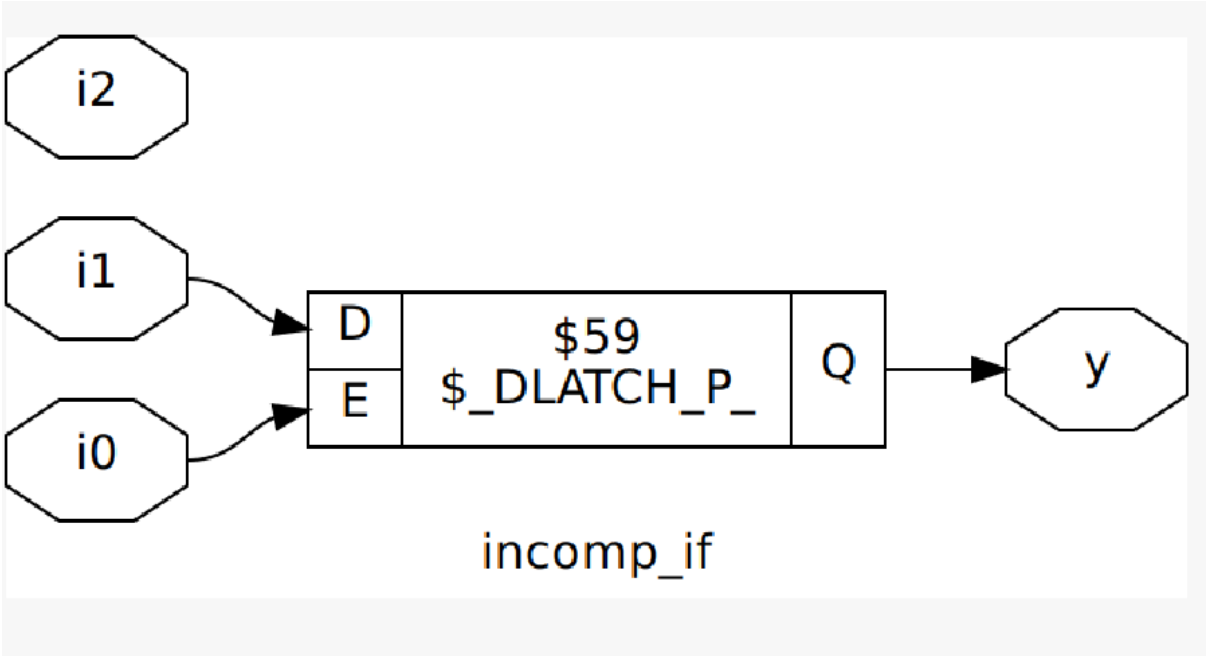






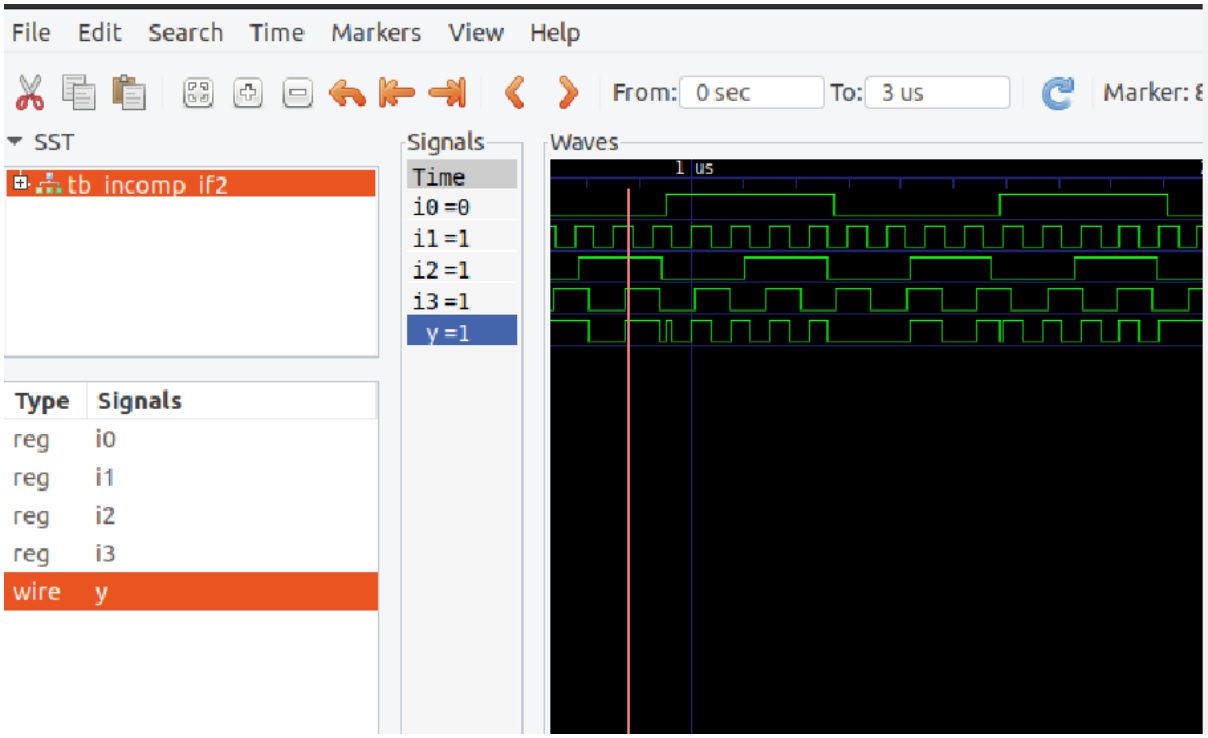
Synthesis

```
3.26. Printing statistics.

=== incomp_if ===

   Number of wires:                 4
   Number of wire bits:             4
   Number of public wires:          4
   Number of public wire bits:      4
   Number of memories:              0
   Number of memory bits:           0
   Number of processes:             0
   Number of cells:                 1
     $_DLATCH_P_                    1

3.27. Executing CHECK pass (checking for obvious problems).
checking module incomp_if..
found and reported 0 problems.
```



Incomp_if2.v

```
End of script. Logfile hash: d07ef12ca4
CPU: user 0.99s system 0.11s, MEM: 47.30 MB total, 37.37 MB resident
Yosys 0.9 (git sha1 1979e0b)
Time spent: 55% 1x share (0 sec), 24% 2x read_liberty (0 sec), ...
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthesisWorkshop/verilog_files# iverilog incomp_if2.v tb_incomp_if2.v
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthesisWorkshop/verilog_files# ./a.out
VCD info: dumpfile tb_incomp_if2.vcd opened for output.
root@vsd:/home/mjcet/Desktop/raheem/week1/day1/vsdflow/sky130RTLDesignAndSynthesisWorkshop/verilog_files# gtkwave tb_incomp_if2.vcd
Gtk-Message: 22:29:59.550: Failed to load module "canberra-gtk-module"

GTKWave Analyzer v3.3.103 (w)1999-2019 BSI
```



```
3.26. Printing statistics.

=== incomp_if2 ===

   Number of wires:                 7
   Number of wire bits:             7
   Number of public wires:          5
   Number of public wire bits:      5
   Number of memories:              0
   Number of memory bits:           0
   Number of processes:             0
   Number of cells:                 3
     $_DLATCH_P_                    1
     $_MUX_                         1
     $_OR_                          1

3.27. Executing CHECK pass (checking for obvious problems).
checking module incomp_if2..
found and reported 0 problems.
```

```
ABC: + &get -n
ABC: + &dch -f
ABC: + &nf
ABC: + &put
ABC: + write_blif <abc-temp-dir>/output.blif

4.1.2. Re-integrating ABC results.
ABC RESULTS:   sky130_fd_sc_hd__mux2_1 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__or2_0 cells:         1
ABC RESULTS:        internal signals:        0
ABC RESULTS:           input signals:        4
ABC RESULTS:          output signals:        2
Removing temp directory.
```