

## RCA Ripple Carry Adder

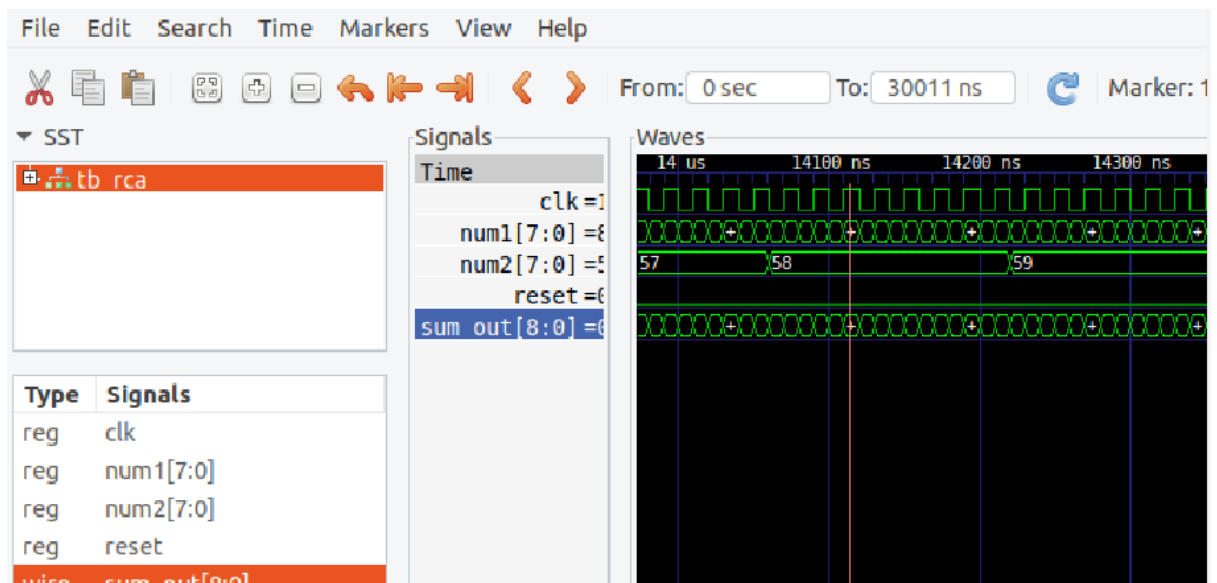
```
module rca (input [7:0] num1 , input [7:0] num2 , output [8:0] sum);
wire [7:0] int_sum;
wire [7:0] int_co;

genvar i;
generate
    for (i = 1 ; i < 8 ; i=i+1) begin
        fa u_fa_1 (,a(num1[i]),b(num2[i]),c(int_co[i-1]),co(int_co[i]),sum(int_sum[i]));
    end
endgenerate
fa u_fa_0 (,a(num1[0]),b(num2[0]),c(1'b0),co(int_co[0]),sum(int_sum[0]));

assign sum[7:0] = int_sum;
assign sum[8] = int_co[7];
```

```
ay1/vsdf/flow/sky130RTLDesignAndSynthesisWorkshop/verilog_files# iverilog rca.v f
a.v tb_rca.v
root@vsd:/home/njcet/Desktop/raheem/week1/day1/vsdf/flow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# ./a.out
VCD info: dumpfile tb_rca.vcd opened for output.
root@vsd:/home/njcet/Desktop/raheem/week1/day1/vsdf/flow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# gtkwave tb_r
tb_rca.v          tb_rca.vcd          tb_ripple_counter.v
root@vsd:/home/njcet/Desktop/raheem/week1/day1/vsdf/flow/sky130RTLDesignAndSynthe
sisWorkshop/verilog_files# gtkwave tb_rca.vcd
Gtk-Message: 13:50:46.999: Failed to load module "canberra-gtk-module"

GTKWave Analyzer v3.3.103 (w)1999-2019 BSI
```



```

rca                                1
fa                                 8

Number of wires:                    69
Number of wire bits:                105
Number of public wires:             45
Number of public wire bits:         81
Number of memories:                 0
Number of memory bits:              0
Number of processes:                0
Number of cells:                    40
  $_NAND_                           8
  $_NOT_                             8
  $_OAI3_                            8
  $_XNOR_                           8
  $_XOR_                             8

4.27. Executing CHECK pass (checking for obvious problems).
checking module fa..
checking module rca..
found and reported 0 problems.

```

#### 5.1.2. Re-integrating ABC results.

```
ABC RESULTS: sky130_fd_sc_hd__maj3_1 cells:      1
ABC RESULTS: sky130_fd_sc_hd__xor3_1 cells:      1
ABC RESULTS:      internal signals:      3
ABC RESULTS:      input signals:      3
ABC RESULTS:      output signals:      2
Removing temp directory.
```

```
5.2. Extracting gate netlist of module '\rca' to '<abc-temp-dir>/input.blif'..
Extracted 0 gates and 0 wires to a netlist network with 0 inputs and 0 outputs.
Don't call ABC as there is nothing to map.
Removing temp directory.
```