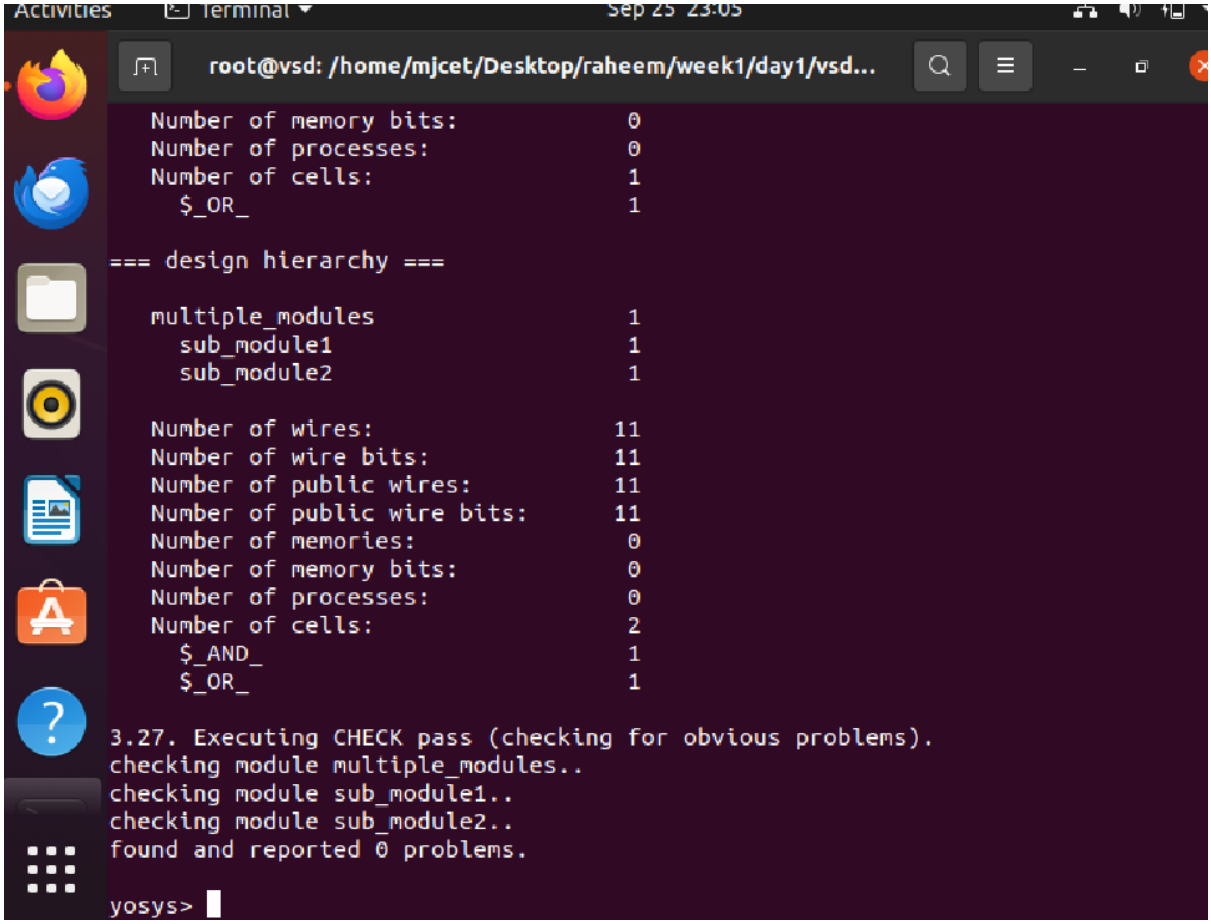
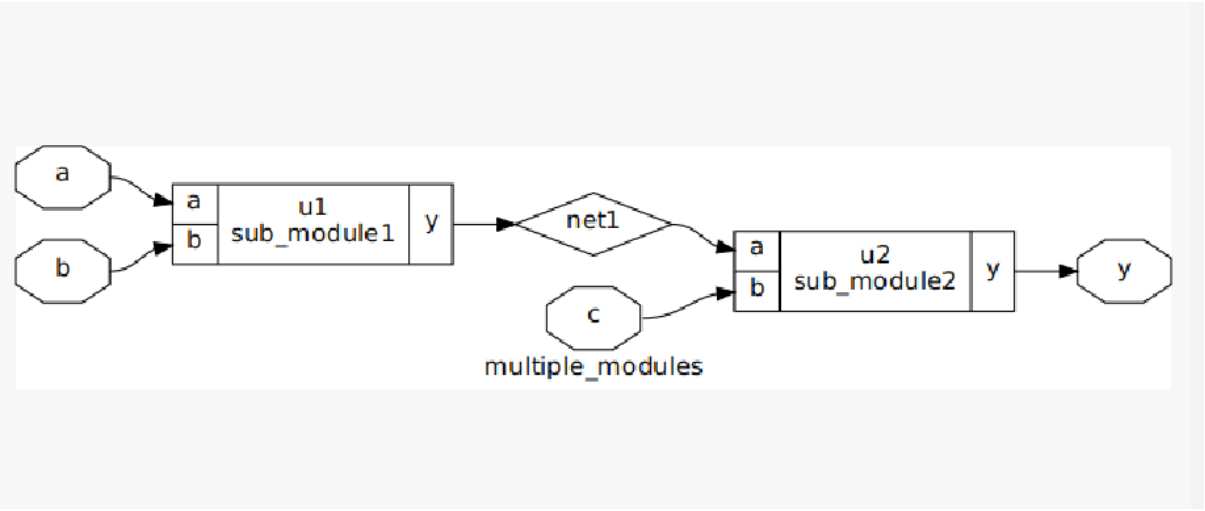
Multiple_modules.v Flat vs Herarchical

```
 Yosys 0.9 (git sha1 1979e0b)


yosys> read_liberty -lib ../lib/sky130_fd_sc_hd__tt_025C_1v80.lib
1. Executing Liberty frontend.
Imported 418 cell types from liberty file.

yosys> read_verilog multiple_modules
multiple_modules.v       multiple_modules_flat.v  multiple_modules_hier.v

yosys> read_verilog multiple_modules
multiple_modules.v       multiple_modules_flat.v  multiple_modules_hier.v

yosys> read_verilog multiple_modules.v

2. Executing Verilog-2005 frontend: multiple_modules.v
Parsing Verilog input from `multiple_modules.v' to AST representation.
Generating RTLIL representation for module `\sub_module2'.
Generating RTLIL representation for module `\sub_module1'.
Generating RTLIL representation for module `\multiple_modules'.
Successfully finished Verilog frontend.
```




```
ABC: + retime
ABC: + strash
ABC: + &get -n
ABC: + &dch -f
ABC: + &nf
ABC: + &put
ABC: + write_blif <abc-temp-dir>/output.blif

4.3.2. Re-integrating ABC results.
ABC RESULTS:   sky130_fd_sc_hd__or2_0 cells:        1
ABC RESULTS:        internal signals:        0
ABC RESULTS:           input signals:        2
ABC RESULTS:          output signals:        1
Removing temp directory.
```

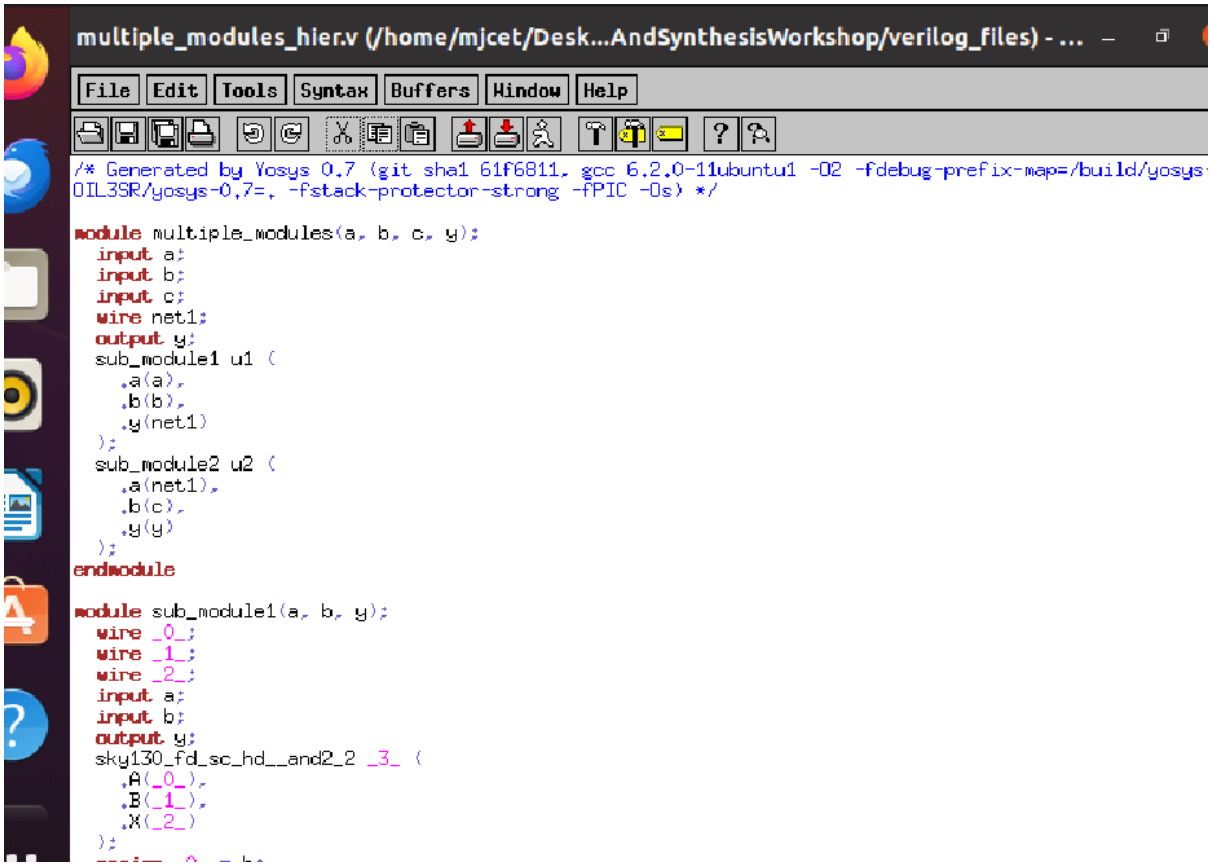



```
yosys> write_verilog -noattr multiple_module_net.v

7. Executing Verilog backend.
Dumping module `\multiple_modules'.
Dumping module `\sub_module1'.
Dumping module `\sub_module2'.
```

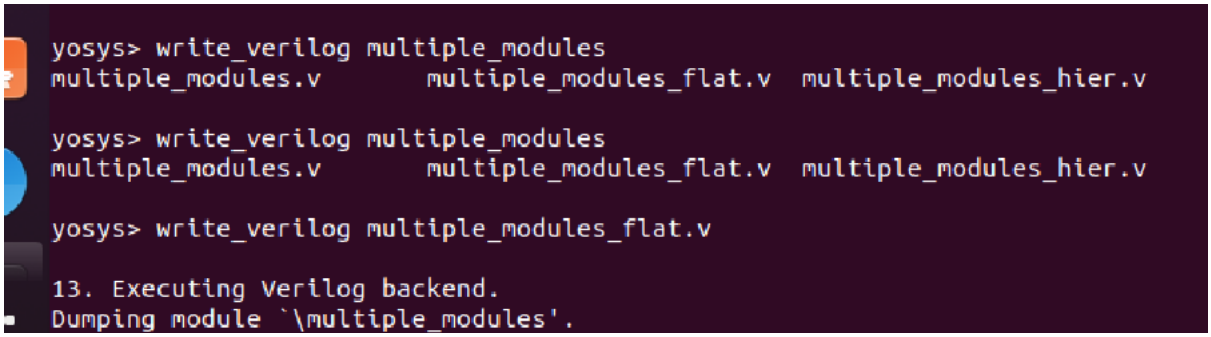
Multiple _module_hier

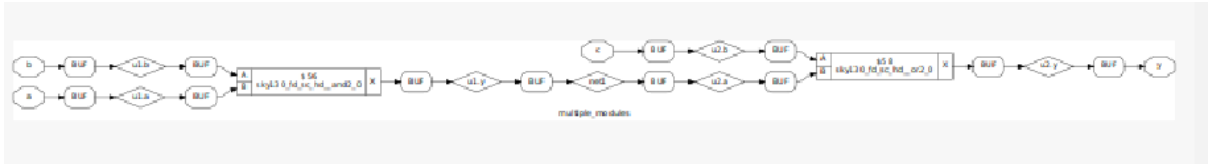
```
yosys> write_verilog -noattr multiple_module_hier.v

10. Executing Verilog backend.
Dumping module `\multiple_modules'.
Dumping module `\sub_module1'.
Dumping module `\sub_module2'.

yosys> !gvim multiple_modules_hier.v

11. Shell command: gvim multiple_modules_hier.v
E285: Failed to create input context
E285: Failed to create input context
```

Multiple _module_flat



multiple _modules_flat

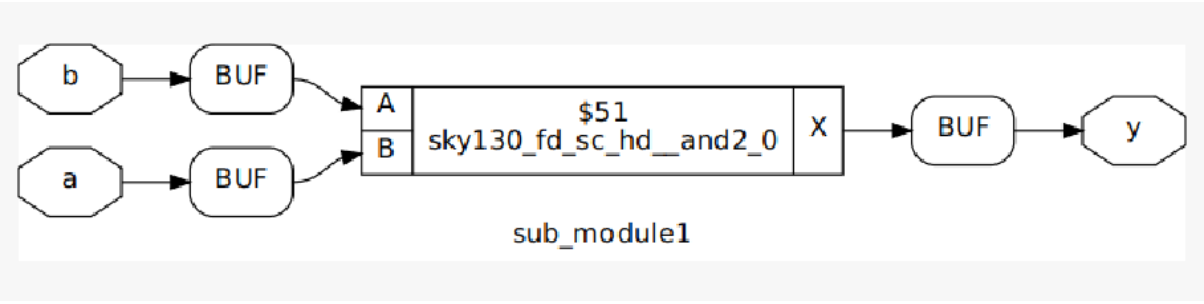




Submodule

```
3.25.2. Analyzing design hierarchy..
Top module:  \sub_module1
Removed 0 unused modules.

3.26. Printing statistics.

=== sub_module1 ===

   Number of wires:                 3
   Number of wire bits:             3
   Number of public wires:          3
   Number of public wire bits:      3
   Number of memories:              0
   Number of memory bits:           0
   Number of processes:             0
   Number of cells:                 1
     $_AND_                         1

3.27. Executing CHECK pass (checking for obvious problems).
checking module sub_module1..
```

```
ABC: + write_blif <abc-temp-dir>/output.blif

4.1.2. Re-integrating ABC results.
ABC RESULTS:   sky130_fd_sc_hd__and2_0 cells:        1
ABC RESULTS:        internal signals:        0
ABC RESULTS:           input signals:        2
ABC RESULTS:          output signals:        1
Removing temp directory.

yosys> show

5. Generating Graphviz representation of design.
Writing dot description to `/root/.yosys_show.dot'.
Dumping module sub_module1 to page 1.
Exec: { test -f '/root/.yosys_show.dot.pid' && fuser -s '/root/.yosys_show.dot.
pid'; } || ( echo $$ >&3; exec xdot '/root/.yosys_show.dot'; ) 3> '/root/.yosys
_show.dot.pid' &
```


b
BUF
a
BUF
A
B
$51
sky130_fd_sc_hd__and2_0
X
BUF
y
sub_module1