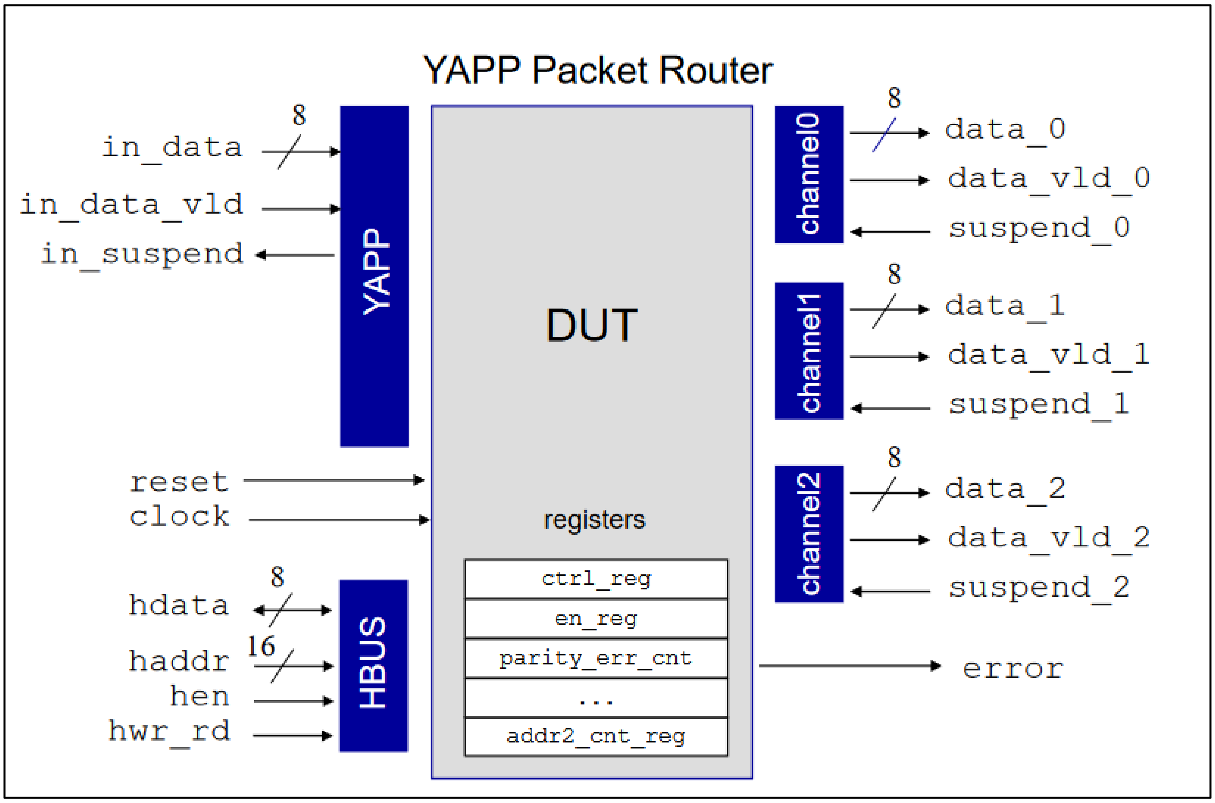
YAPP Router Specification

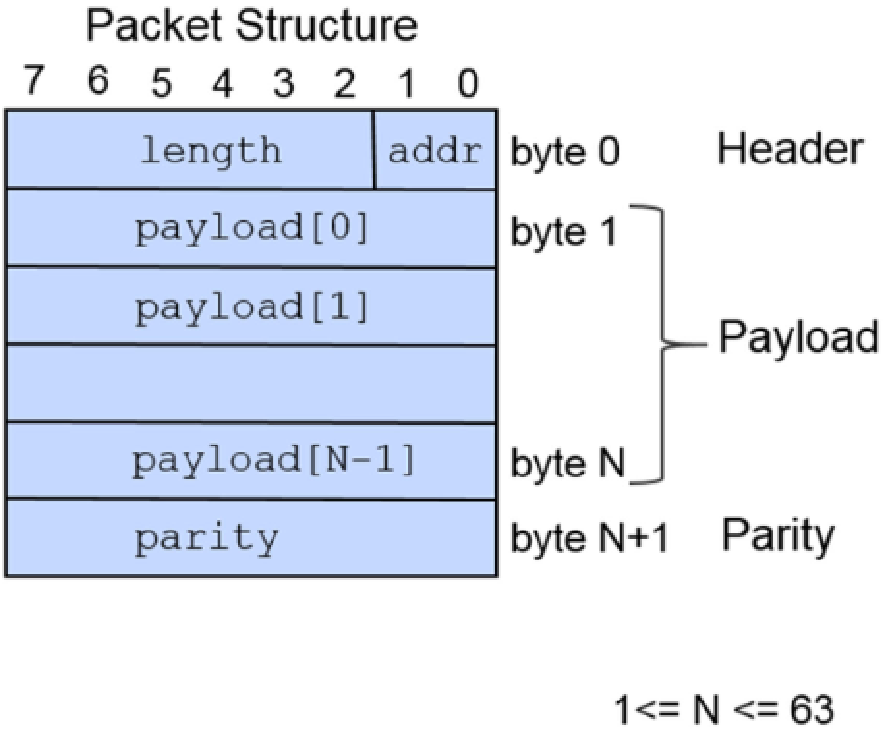
The YAPP router accepts data packets on a single input port, in_data, and routes the packets to one of three output channels: channel0, channel1 or channel2. The input and output ports have slightly different signal protocols. The router also has an HBUS host interface for programming registers that are described in the next section.

High-Level Diagram – YAPP Router(Yet Another Packet Protocol)



Packet Data Specification

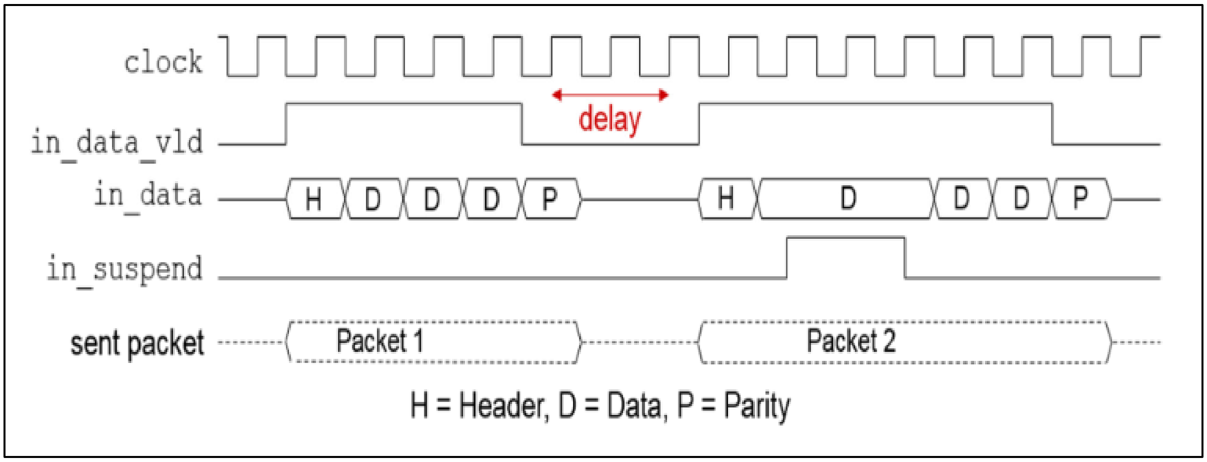
A packet is a sequence of bytes with the first byte containing a header, the next variable set of bytes containing payload, and the last byte containing parity.
The header consists of a 2-bit address field and a 6-bit length field. The address field is used to determine which output channel the packet should be routed to, with the address 3 being illegal.
The length field specifies the number of data bytes (payload).
A packet can have a minimum payload size of 1 byte and a maximum size of 63 bytes.
The parity should be a byte of even, bitwise parity, calculated over the header and payload bytes of the packet.



Input Port Protocol

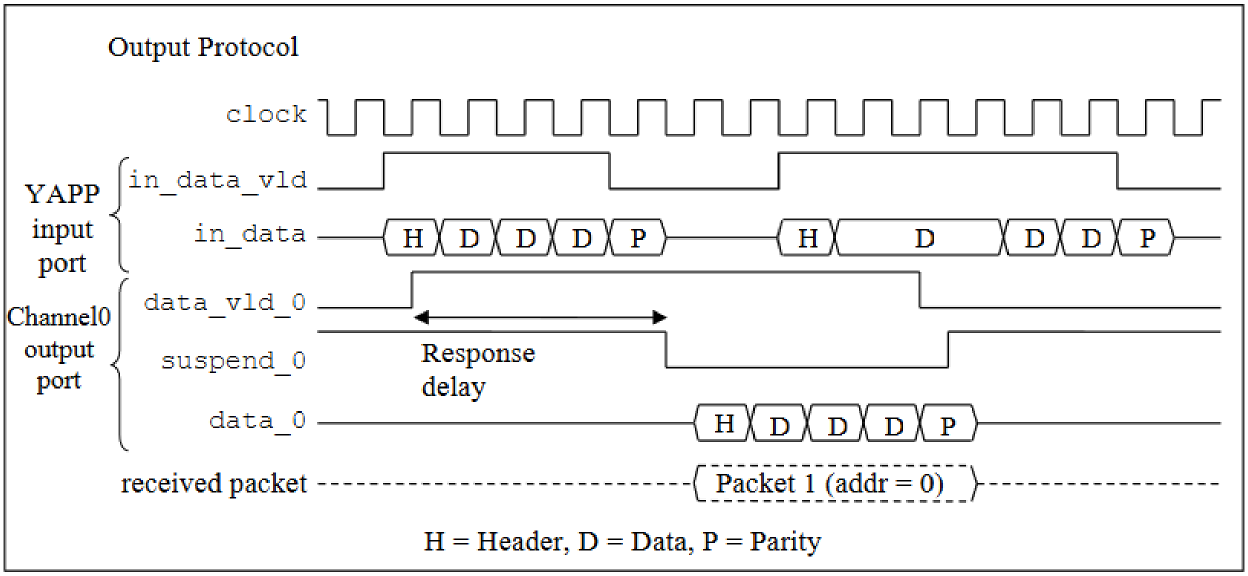
All input signals are active high and are to be driven on the falling edge of the clock. The in_data_vld signal must be asserted on the same clock when the first byte of a packet (the header byte) is driven onto the in_data bus. As the header byte contains the address, this tells the router to which output channel the packet needs to be routed. Each subsequent byte of data needs to be driven on the data bus with each new falling clock.

After the last payload byte has been driven, on the next falling clock, the in_data_vld signal must be de-asserted, and the packet parity byte needs to be driven. The input data cannot change while in_suspend signal is active (indicating FIFO full). The error signal asserts when a packet with bad parity is detected, within 1 to 10 cycles.



Output Port Protocol (Channel Ports)

All output signals are active high and are to be sampled on the falling edge of the clock. Each output port is internally buffered by a FIFO of depth 16 and a width of 1 byte. The router asserts the data_vld_x signal when valid data appears on the data_x output bus. The suspend_x input signal must then be de-asserted on the falling clock edge in which data is read from the data_x bus. As long the suspend_x signal remains inactive, the data_x bus drives a new valid packet byte on each rising clock edge.



Packet Router DUT Registers

The packet router contains internal registers that hold configuration information. These registers are accessed through the host interface port. Register characteristics are as follows:

address	register	reset	field	field name	policy	description
0x1000	ctl_reg	0x3f	5:0	maxpktsize	RW	Maximum packet length
			7:6		RW	Unused
0x1001	en_reg	0x01	0	router_en	RW	Router enable
			1	parity_err_cnt_en	RW	Parity error count enable
			2	Oversize_pkt_cnt_en	RW	Length error count enable
			3	[reserved]	RW	Not implemented
			4	addr0_cnt_en	RW	Address 0 packet count enable
			5	addr1_cnt_en	RW	Address 1 packet count enable
			6	addr2_cnt_en	RW	Address 2 packet count enable
			7	addr3_cnt_en	RW	Address 3 packet count enable
0x1004	parity_err_cnt_reg	0x00	7:0		RO	Packet parity error count
0x1005	oversized_pkt_cnt_reg	0x00	7:0		RO	Packet length error count
0x1006	addr3_cnt_reg	0x00	7:0		RO	Address 3 packet count
0x1009	addr0_cnt_reg	0x00	7:0		RO	Address 0 packet count
0x100a	addr1_cnt_reg	0x00	7:0		RO	Address 1 packet count
0x100b	addr2_cnt_reg	0x00	7:0		RO	Address 2 packet count

If the input packet length is greater than the maxpktsize field of the ctrl_reg register, then the router drops the entire packet.

The router_en field of the en_reg register controls the enabling and disabling of the router. A disabled router drops all packets. Enabling or disabling the router during packet transmission will yield to unpredictable behavior.

The router counters are enabled by individual bits in en_reg. The router specification says that if these bits are changed while the router is processing a packet, then the router behavior is undefined.

The router counters are defined as follows:

parity_err_cnt_reg – incremented when a bad parity packet is received

oversized_pkt_cnt_reg – incremented when packet with length greater than maxpktsize is received.

addr3_cnt_reg – incremented when a packet with an illegal address (3) is received

addr0_cnt_reg – incremented when a packet with address 0 is received

addr1_cnt_reg – incremented when a packet with address 1 is received

addr2_cnt_reg – incremented when a packet with address 2 is received

Router Memories

The router contains two memory blocks as follows:

Start Address	Name	Size	Policy	Description
0x1010	Yapp_pkt_mem	[0:63]	RO	Stores the bytes of the last packet received by the yapp router.
0x1100	Yapp_mem	[0:255]	RW	"Scratch" memory

Host Interface Port Protocol (HBUS)

All input signals are active high and are to be driven on the **falling** edge of the clock. The host portprovides synchronous read/write access to program the router.

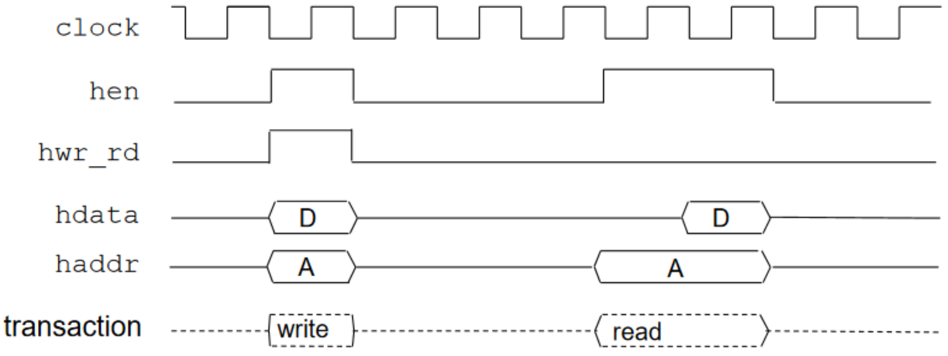
A WRITE operation takes one clock cycle as follows:

- hwr_rd and hen must be 1. Data on hdata is then clocked on the next rising clock edge into the register based on haddr decode.
- hen is driven to 0 in the next cycle.

A READ operation takes two clock cycles as follows:

- hwr_rd must be 0 and hen must be 1. In the first clock cycle, haddr is sampled and hdata is driven by the design under test (DUT) in the second clock cycle.
- hen is then driven low after cycle 2 ends. This will cause the DUT to tri-state the hdata bus.

The HBUS port provides synchronous read/write access to program the router.



A = Address, D = Data