UTM UNIVERSITI TEKNOLOGI MALAYSIA
RESEARCH UNIVERSITY
School of Computing

FINAL EXAMINATION SEMESTER I 2018/2019

COURSE CODE	**:**	**SCSR1013**
COURSE TITLE	**:**	**DIGITAL LOGIC**
PROGRAM	**:**	**SCSR/SCSJ/SCSB/SCSV/SCSP**
TOTAL TIME	**:**	**3 HOURS (09:00 – 12:00)**
DATE	**:**	**29 DECEMBER 2018 (SATURDAY)**
VENUE	**:**	**DEWAN SULTAN ISKANDAR HALL**

(GENERAL INSTRUCTION):

Answer all questions from Part A and Part B. Show ALL your works.

Write ALL your answers in the answer booklet EXCEPT:

1. **Part A: Objectives – answer at Page 9 in question booklet.**
2. **Part B: Question 4 – answer at Figure 5 and Figure 6 in question booklet.**

This exam will contribute 35% towards the total marks of 100%.

Warning!

Students who are caught cheating during the examination will be reported to the disciplinary board for possible suspension of the student for one or two semesters.

Name	
Matric No.	
Year / Course	
Section (Circle)	**01 / 02 / 03 / 04 / 05 / 06 / 07 / 08 / 09 / 10**
Lecturer (Circle)	**Mr Firoz / Ms Marina / Dr Mazura / Dr Mohd Foad Mr Muhalim / Dr Raja Zahilah / Mrs Rashidah**

This question booklet consists of 10 pages including the front page.

PART A – OBJECTIVES: 20 MARKS

1. Which of the following functions can be used to detect how many empty slots available in a parking lot?

   A. Encoder
   B. Comparator
   C. Multiplexer
   D. Parity Generator

2. What gates should you use to decode the binary number 0011 with an active-LOW decoder?

   A. OR and NAND gates
   B. AND and NOR gates
   C. NOT and AND gates
   D. NOT and NAND gates

3. Which statement about DEMUX is FALSE?

   A. It is also known as data selector.
   B. A decoder can also be used as a DEMUX.
   C. A DEMUX reverses the function of a MUX.
   D. It takes digital information from one line and distributes it to a given number of output lines.

4. Choose the TRUE statement regarding parity checker.

   A. Parity checker is used to correct an error in the received data.
   B. Parity checker is used to determine numbers of bit 1 in the data.
   C. OR gate is used in parity checker to check for inequality.
   D. Parity checker is produced using parallel adder.

5. Which of the statement is FALSE about latch and flip-flop?

   A. Both devices are memory elements.
   B. Both devices need clock input in order to change the output state.
   C. Latch output is fully dependent on input level triggered.
   D. Flip-flop output is changing at either at negative or positive clock triggered.

6. If the data select lines of the MUX in Figure 1 are $S_1S_0 = 11$, what would the output be?

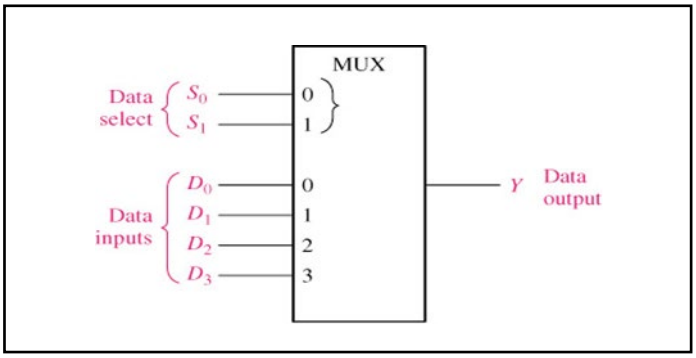


Figure 1

A. LOW
B. HIGH
C. Equal to D_0
D. Equal to D_3

7. Which of the statement is TRUE about sequential logic circuit versus combinational logic circuit design?

A. Both circuits have closed loop feedback from output to the input.
B. Gated-SR flip flop can be included in combinational logic circuit.
C. Clock must be supplied to the input in the combinational logic circuit.
D. Sequential logic circuit must have memory element device.

8. Choose the TRUE statement about the output of S-R flip-flop.

A. The output is SET when S = 0 and R = 1.
B. The output $\bar{Q} = 0$ when S = 1 and R = 0
C. The output is toggle when both inputs are high.
D. The output is invalid when both inputs are low.

9. Choose the FALSE statement regarding the flip-flop asynchronous input:

A. The output Q = 1 when $\overline{PRE} = 0$ and $\overline{CLR} = 1$.
B. The flip-flop is CLEAR when $\overline{PRE} = 1$ and $\overline{CLR} = 0$.
C. The output will depends on inputs S and R when both $\overline{PRE}$ and $\overline{CLR}$ are low.
D. The flip-flop will no longer asynchronous when both $\overline{PRE}$ and $\overline{CLR}$ are high.

10. The output Q can be represented by the following flip-flop (negative-edged clock) EXCEPT:

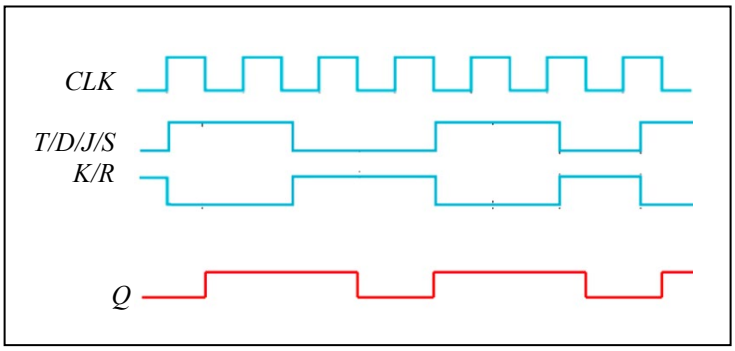


Figure 2

A. S-R flip-flop.
B. J-K flip-flop.
C. D flip-flop.
D. T flip-flop

11. Which of the following is considered as medium priority input(s)?

A. Clock
B. $\overline{PRE}$
C. T
D. J and K

12. Choose the CORRECT statement about asynchronous counter.

A. Low-frequency applications are limited because of internal propagation delays.
B. High-frequency applications are limited because of internal propagation delays.
C. Asynchronous counters are suitable for use in high- and low-frequency counting applications.
D. Asynchronous counters do not have propagation delays and this limits their use in high-frequency applications.

13. How many flip-flops are required to produce MOD 32 binary counter?

A. 3
B. 45
C. 5
D. 6

14. Three cascaded MOD 5 counters have an overall modulus of _____.

A. 5
B. 25
C. 125
D. 500

15. Using four cascaded CTR DIV 16, how many states must be deleted to achieve MOD 50,000?

A. 50,000
C. 25,536
B. 65,536
D. 15,536

16. A bidirectional 4-bit shift register is storing the nibble 1110. The nibble 0111 is waiting to be entered on the serial data-input line (MSB is inserted first). After two clock pulses, the shift register is storing _____.

A. 1110
C. 1000
B. 0111
D. 1001

17. The group of bits 10110111 is serially shifted (right-most bit first) into an 8-bit parallel output shift register with an initial state 11110000. After two clock pulses, the register contains _____.

A. 10111000
C. 11110000
B. 10110111
D. 11111100

18. What type of register would have a complete binary number shifted in one bit at a time and have all the stored bits shifted out one at a time?

A. Parallel-in Parallel-out (PIPO)
C. Serial-in Parallel-out (SIPO)
B. Parallel-in Serial-out (PISO)
D. Serial-in Serial-out (SISO)

19. How many states available in a 4-bit Johnson counter sequence?

A. 1
C. 4
B. 3
D. 8

20. Which statement is FALSE?

A. Johnson counter needs no decoder.
B. n bit binary counter produce 2^n states.
C. The last output of Ring counter is connected to its first input.
D. Ring counter is made of SISO registers.

PART B – SUBJECTIVES: 80 MARKS

Assume MSB is the left most bit for all questions.

QUESTION 1 [15 MARKS]

a) Draw a block diagram of 3-bit adder, using both half and full adders. Show clearly all the inputs and outputs in your diagram when input A = 101 and B = 011 are added. [*6 marks*]

b) Draw a logic gate function that would test 2-bit numbers for equality. Name the function. [*4 marks*]

c) Build a truth table for a three inputs decoder with active-high outputs. However, if the value of the input corresponds to 5 or 7, then all output lines should signal an error (bit 1). [*5 marks*]

QUESTIONS 2 [15 MARKS]

LSB is inserted first.

a) Design a 5-bit ring counter using D flip-flop with its initial value 01100. [*5 marks*]

b) By using sequence table, show the output of the ring counter for 10 clock cycles. [*3 marks*]

c) Draw the state diagram of the designed ring counter and determine its MOD. [*2 mark*s]

d) Generate the timing diagram. [*5 marks*]

QUESTIONS 3 [35 MARKS]

a) An asynchronous counter with the following specification:

- Recycle count down from 12 to 0
- Positive edge flip-flops
- Using JK flip-flops, use Q_0 as LSB.

i. Determine the number of flip-flops required. [*1 marks*]

ii. Design an active low decoder for the asynchronous counter. [*1 mark*]

iii. Draw the circuit connection for the asynchronous counter. [*4 marks*]

b) Analyse the following circuit as shown in Figure 3.

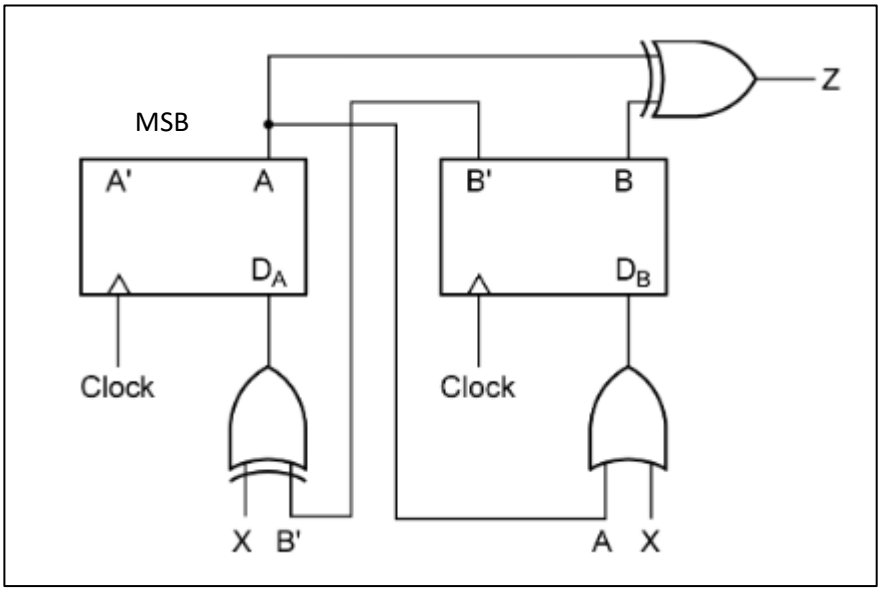


Figure 3

i. Get Boolean expression for the input D_A, D_B and output Z. Derive the next state equation by converting Boolean expression into flip-flop characteristic equations. Use A_+ and B_+ for the next state. [*2 marks*]

ii. From the next state equation, produce the next state table. Use X as input.[*4 marks*]

iii. Produce the state diagram of the circuit shown in Figure 3. [*3 marks*]

c) Design a synchronous counter using T flip-flop that repeats counting from 0 to 7 when X = 0, but turns to 0 whenever X = 1. The output Y will become 1 whenever the counter reaches 0 and 7. Draw the state diagram. Show all your works. [*20 marks*]

QUESTIONS 4 [15 MARKS]

a) Gated SR and D latches are cascaded together as shown in Figure 4. If input of the latches is given as in the timing diagram (refer Figure 5), draw the output of Q1 and Q2. Give comments for each of the state changes in Q1 and Q2. Write your answer in Figure 5. [*7 marks*]

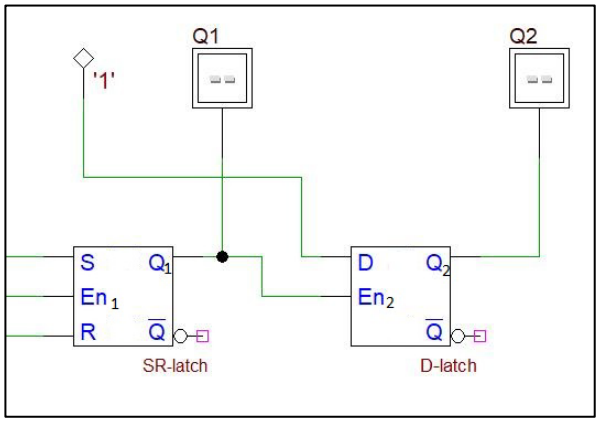


Figure 4: Two cascaded Gated SR and D latches

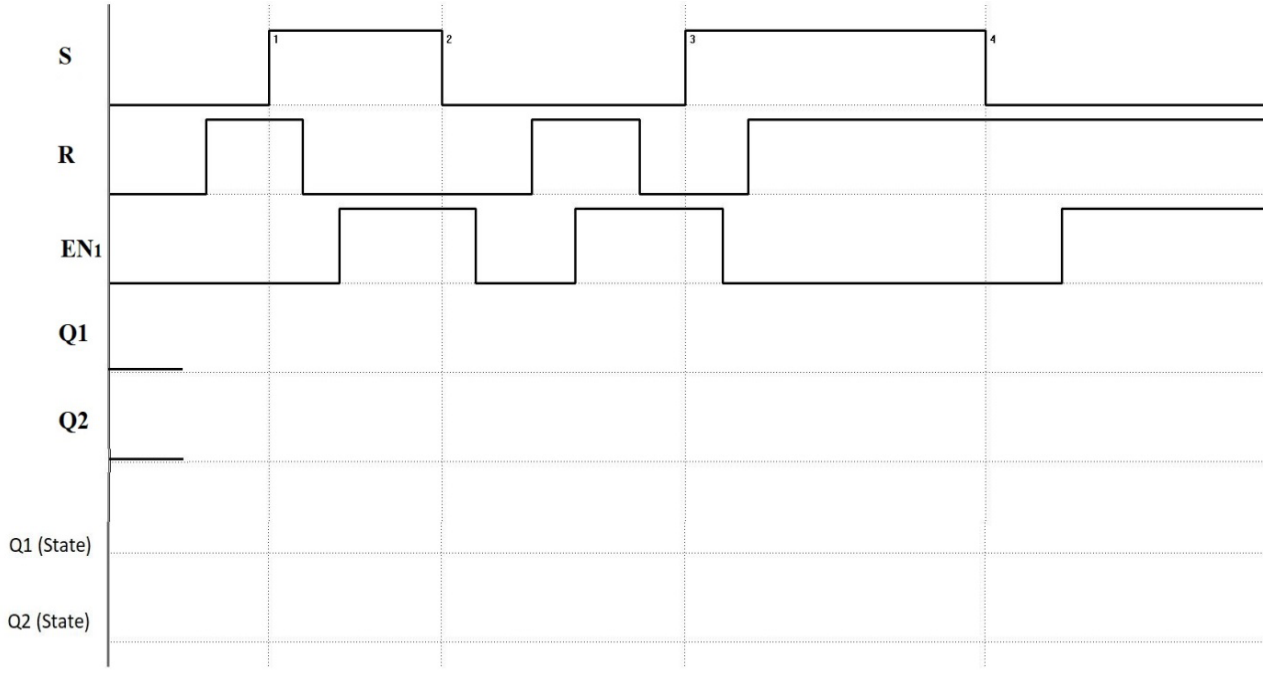
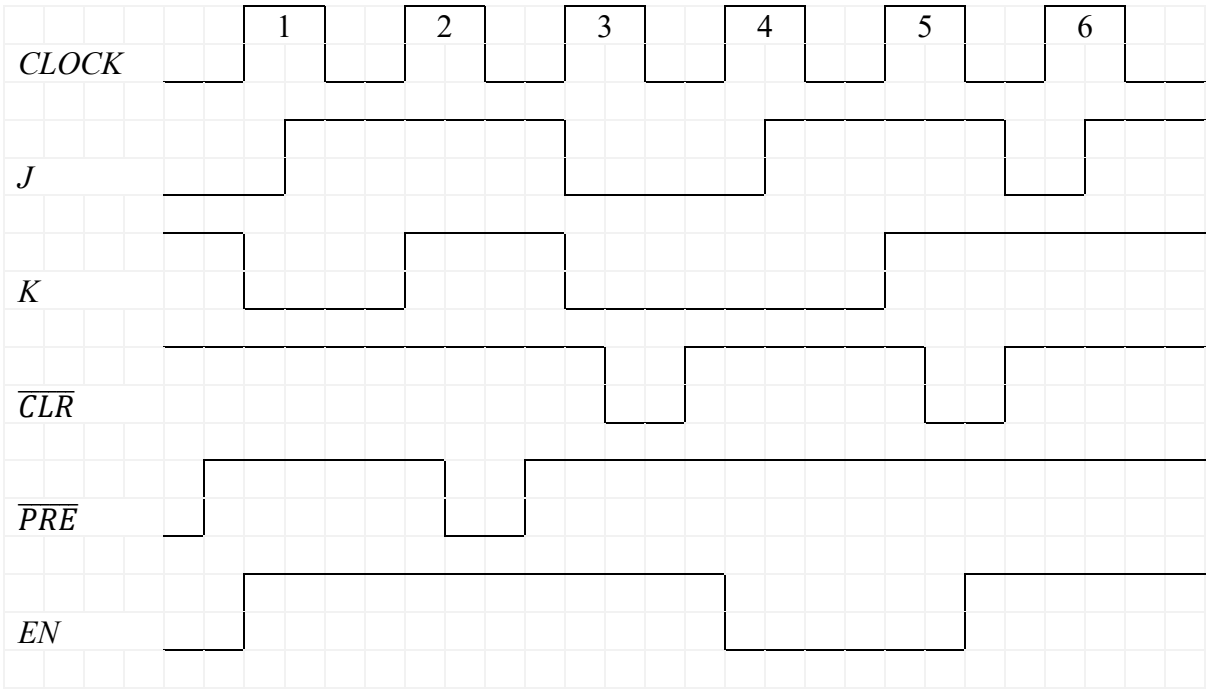


Figure 5: Cascaded Gated-SR and D latches timing diagram

b) Consider the following timing diagram for a J-K flip-flop with output Q is initially LOW.



i) Q

ii)

iii) Q_{new}

Figure 6

Answer the following questions in the above Figure 6.

i) Suppose that it is a negative-edge J-K flip-flop. Draw the waveform of output Q. [*3 marks*]

ii) Write the state of the output at CLOCK 4 and 6. [*2 marks*]

iii) If the FF is positive-edge and JK inputs are always HIGH, draw the new output Q_{new}. Assume the initial value is LOW. [*3 marks*]

ANSWER SHEET

Name	
Matric No	
Lecturer (Circle)	**Mr Firoz / Ms Marina / Dr Mazura / Dr Mohd Foad** **Mr Muhalim / Dr Raja Zahilah / Mrs Rashidah**

PART A (OBJECTIVES)

Mark your answer clearly.

Example: =A= =B= =C= =D=

20

1. =A= =B= =C= =D=

2. =A= =B= =C= =D=

3. =A= =B= =C= =D=

4. =A= =B= =C= =D=

5. =A= =B= =C= =D=

6. =A= =B= =C= =D=

7. =A= =B= =C= =D=

8. =A= =B= =C= =D=

9. =A= =B= =C= =D=

11. =A= =B= =C= =D=

12. =A= =B= =C= =D=

13. =A= =B= =C= =D=

14. =A= =B= =C= =D=

15. =A= =B= =C= =D=

16. =A= =B= =C= =D=

17. =A= =B= =C= =D=

18. =A= =B= =C= =D=

19. =A= =B= =C= =D=

10. =A= =B= =C= =D= **20.** =A= =B= =C= =D=