STRUCTURED QUESTIONS (100 MARKS)

(INSTRUCTION: This question booklet has 7 questions. Please write the answers for all questions in the answer booklet. Show all your working steps.)

QUESTION 1 [15 *Marks*]

(a) Consider the initial contents for some registers as given in **Figure 1**. Assume that the two lines of instructions given in **Figure 2** are executed based on these initial contents. Calculate the final contents of registers EAX, EBX, and EDX after the instructions have been executed. [4 *Marks*]

```
EAX=770C0810  EBX=7FFD0410  ECX=00000000  EDX=00400001
ESI=00000000  EDI=00000000  EBP=0012FF94  ESP=0012FF8C
EIP=00401025  EFL=00000A82  CF=0  SF=1  ZF=0  OF=1
```

Figure 1

```
MOV    AX, 200h
MUL    BX
```

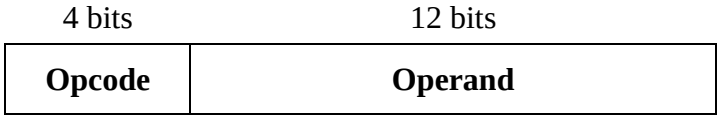
Figure 2

(b) Consider a 16 bits system that uses even parity. Calculate 8028h + 803Ah in binary and based on the result, determine the value for each of the flags shown in **Table 1**. [4 *Marks*]

Table 1

ZF	SF	CF	OF	AF	PF

(c) Given an ISA (Instruction Set Architecture) format is as in **Figure 3**:



Opcode: 0001_2 = MOV, 0101_2 = SUB

Figure 3

Trace the execution of instruction cycle for memory address 39Dh as shown in **Table 2**. Given the initial values as in **Table 3**, complete the instruction cycle by writing the contents of the related CPU registers with the respective microoperations. [7 *Marks*]

Table 2

Memory Address	Memory Content (Hex)	Instruction/Data
39C	1743	`MOV AX,9Ah`
39D	5743	`SUB AX,NUM`
39E		
…	…	…
743	000A	`NUM`
744	0F00	

Table 3

Clock	IP/PC	MAR	MBR	IR	AX	Microoperations
t_0	39D				009A	IP/PC = 39D

QUESTION 2 [17 *Marks*]

(a) **Table 4** illustrates the segments of a pipeline with the registers' interface delay is 5 ns. Based on the given information in **Table 4**, calculate the following:

Table 4

Segment	Execution Times (ns)
Fetch Instruction (FI)	50
Decode Instruction (DI)	45
Fetch Operand (FO)	40
Execute Instruction (EI)	45
Write Operand (WO)	35

i) The cycle time of non-pipeline and pipeline. [4 *Marks*]

ii) The execution time of 100 tasks for non-pipeline and pipeline. [4 *Marks*]

iii) The real Speedup, *S*. [2 *Marks*]

iv) The maximum Speedup, S_{max}. [1 *Mark*]

(b) Consider the assembly program in **Figure 4** is executed in a pipeline that consists of these segments: *Fetch Instruction* (FI), *Decode Instruction* (DI), *Execute Instruction* (EI) and *Write Operand* (WO). Based on the instructions given in **Figure 4**, determine which instruction(s) have the following hazards and rewrite the instructions using the proposed solutions.

```
I1:              MOV     AX, BX
I2:              ADD     CX, AX
I3:              INC     DX
I4:              JMP     TARGET
I5:              MOV     BX, 5
I6:              INC     CX
. . . . .
I12:   TARGET    DEC     AX
```

Figure 4

i) Data dependency and solve using Delayed Load. [3 *Marks*]

ii) Branch difficulty and solve using Delayed Branch and Rearranging Instructions. [3 *Marks*]

QUESTION 3 [12 *Marks*]

Consider a system uses vertical microinstruction format with a control memory that consists of 128 words and each word consists of 20 bits as illustrated in **Figure 5**. The system also consists of 4 status conditions for branching and 9 bits microoperation with 3 fields.

Microoperation	Select	Address

Figure 5

(a) Based on **Figure 5**, calculate the size (in bits) of the following:

i) The Select and Address fields. [3 *Marks*]

ii) The Branch bits in the Select field. [3 *Marks*]

(b) Based on the answer in (a), and the symbolic microinstructions given in **Table 5**, complete the 20 bits microinstruction fields as listed in **Table 6**, for microinstructions (i), (ii) and (iii). [6 *Marks*]

Table 5

	Label	Address	Microinstruction			
(i)	ADD	0000100	NOP	I	CALL	INDRCT
(ii)			READ	U	JMP	NEXT
(iii)			ADD	U	JMP	FETCH
	FETCH	1000000	. . .			
	INDRCT	1000011	. . .			

(*Remark: Use the binary code for microinstruction fields in **Appendix A** on page* 11.)

Table 6

	Microoperation (F1, F2, F3)	Select (CD, BR)	Address
(i)			
(ii)			
(iii)			

QUESTION 4 [12 *Marks*]

(a) Consider the following different types of memory:

- *Hard Disk Drive (HDD)*
- *Dynamic Random Access Memory (DRAM)*
- *Static Random-Access Memory (SRAM)*
- *Registers*

i) List the memory types based on memory pyramid hierarchy position from top to bottom. [2 *Marks*]

ii) Based on memory pyramid hierarchy, briefly explain how speed, and cost per bit differs from top to bottom. [2 *Marks*]

(b) Consider the main memory is divided into blocks. The memory word is 8 bits and the size of a block is 8 words.

i) What is the capacity of the main memory, if the total number of blocks in the memory is 128? [2 *Marks*]

ii) How many blocks in the main memory if the memory capacity is 64 Kbits? [2 *Marks*]

(c) Consider the memory capacity is 32 Kbytes and the total of banks is 4.

i) Calculate the bits for the Word in bank and the Bank address. [2 *Marks*]

ii) Based on the answer in (i), draw the address format used for both Low-Order Interleaving (LOI) and High-Order Interleaving (HOI). [2 *Marks*]

QUESTION 5 [15 *Marks*]

(a) A main memory contains 32 words while the cache has only 8 words.

i) Using Direct mapping, identify the fields of the main memory address. [1 *Mark*]

ii) **Table 7** illustrates a main memory and its content for some addresses. Complete **Table 8** as they respond to a series of request (in hexadecimal address) as in the following. [5 *Marks*]

19, 1A, 15, 12, 19

Table 7

Address (Hex)	Address (Binary)	Content (Hex)
1A	11010	B1
19	11001	A1
18	11000	F1
17	10 111	B2
16	10 110	E1
15	10 101	C1
14	10100	A2
13	10011	C2
12	10010	D1

Table 8

Line	Tag	Content (Hex)
111		
110		
101		
100		
011		
010		
001		
000		

(i) Cache memory

Tag	Line

(ii) Request

Hit	Miss	Update Cache	Read	Write

(iii) Read/Write operation cache

(b) Given the main memory address format using Block Direct mapping is shown in **Figure 6**. Consider each main memory word is 16 bits.

Tag	Block	Word
7 bits	8 bits	3 bits

Figure 6

i) Calculate the main memory capacity. [2 *Marks*]

ii) Calculate the total cache words. [1 *Mark*]

iii) Calculate the cache word size (in bits). [2 *Marks*]

(c) Consider a main memory address format is given in **Figure 7**. Supposed the program generates the memory address 167Bh. Determine the tag and word in cache memory using Fully Associative mapping. [2 *Marks*]

Tag	Word
11 bits	2 bits

Figure 7

(d) Suppose a single cache fronting a main memory. The access time of the main memory and the cache is 250 ns and 15 ns respectively. Calculate the Effective Access Time (EAT) given the hit rate is 95%. [2 *Marks*]

QUESTION 6 [14 *Marks*]

(a) List the advantages of Direct Memory Access (DMA) as opposed to Interrupt-driven I/O? [4 *Marks*]

(b) **Figure 8** illustrates the bus timing diagram for writing data to the disk drive operations which is executed by DMA and controller. Determine the process for the following period of clocks. [3 *Marks*]

(i) $t_0 - t_2$

(ii) $t_3 - t_7$

(iii) t_8

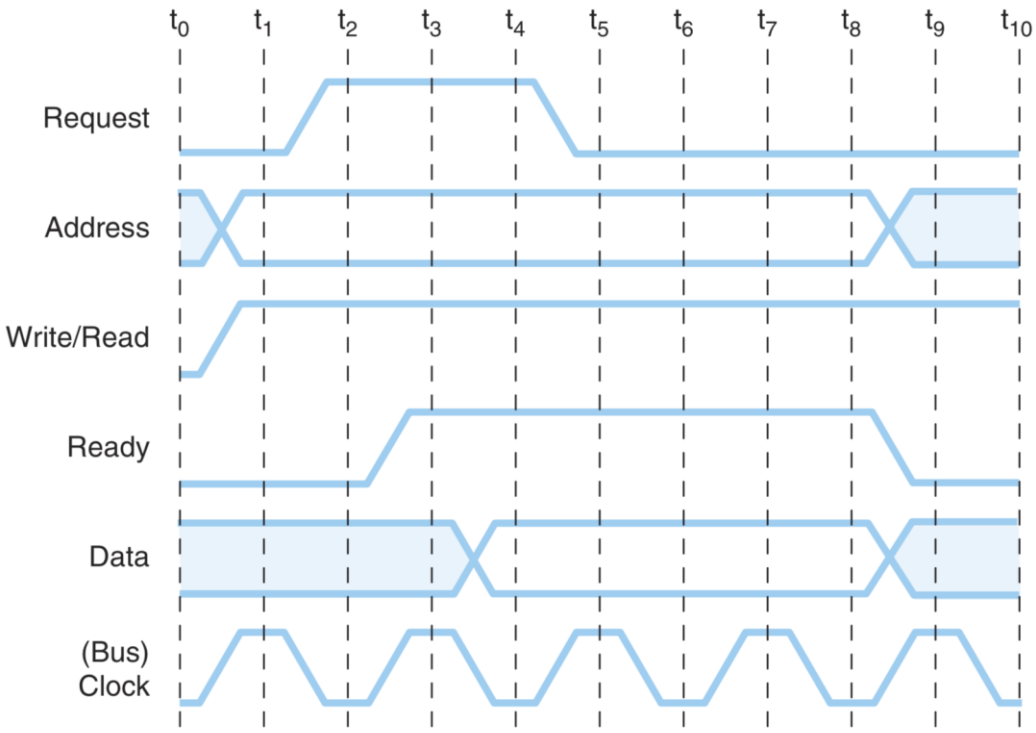


Figure 8

(c) Consider the four data disks and one parity disk are used in RAID Level 3 as shown in **Figure 9**. Determine the bits for data regeneration labeled as (i) to (iv). [2 *Marks*]

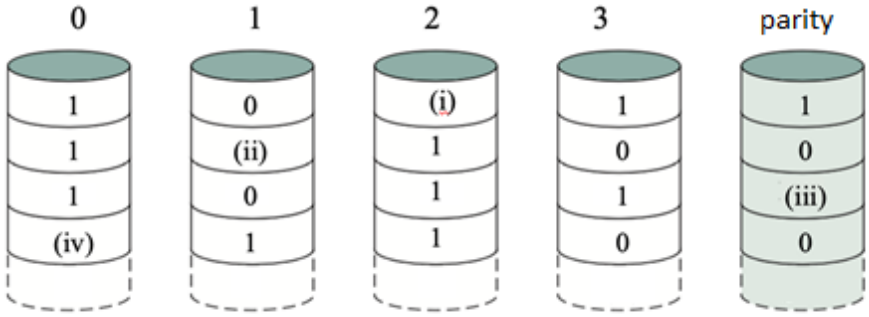


Figure 9

(d) Consider the five data disks are used in RAID Level 5 (Block-Level Distributed Parity) as shown in **Figure 10**. It has four blocks of data and one parity block.

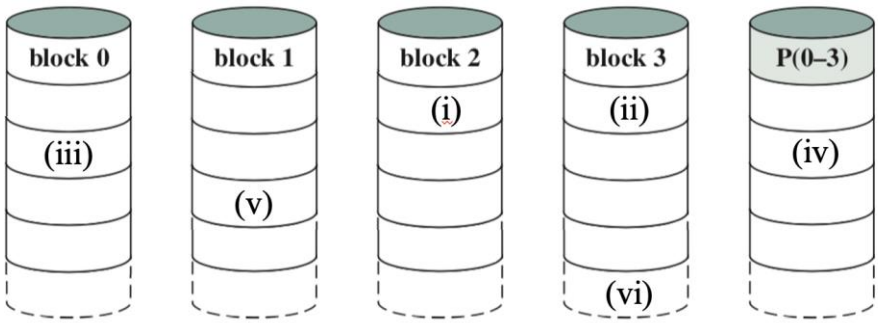


Figure 10

i) Briefly describe the implementation of the parity strips of this RAID Level 5 compared to RAID Level 4. (Remark: Identify the related scheme used). [2 *Marks*]

ii) Consider that 23 blocks are required to be added in the disks. Determine the content of data blocks and parity block labeled as (i) to (vi). [3 *Marks*]

QUESTION 7 [15 *Marks*]

(a) **Table 9** shows the information on program A that needs to be executed by computer X. Given the clock cycle time for computer X is 200 ps and the total instructions of program A are 1 million.

Table 9

Instruction type	CPI	Instruction mix (%)	Clock cycles
Arithmetic	3	30	(i)
Load/Store	2	50	(ii)
Branch	4	20	(iii)

i) Calculate the clock cycles for each Instruction type and write the answers for (i), (ii) and (iii) as in **Table 9**. [2 *Marks*]

ii) Calculate the average CPI and the CPU execution time. [3 *Marks*]

iii) Calculate the CPU Clock rate and MIPS rate. [2 *Marks*]

(b) **Table 10** shows the Execution frequency and time for 3 different programs run by CPU A, B and C.

Table 10

Program	Execution frequency (%)	Execution time (ns)		
		CPU A	CPU B	CPU C
P	50	1000	900	800
Q	30	650	300	200
R	20	200	100	50

i) Calculate the Weighted Average for CPU A, B and C. [3 *Marks*]

ii) Identify the fastest CPU and how many percentage (%) it is faster than the slowest CPU. [2 *Marks*]

iii) Assume that CPU C is normalized to CPU A, calculate the Geometric Mean for CPU C. [3 *Marks*]

--- End of Questions ---

Appendix A

(Microinstruction fields)

F1	Microoperation	Symbol
000	None	NOP
001	AC ← AC + DR	ADD
010	AC ← 0	CLRAC
011	AC ← AC + 1	INCAC
100	AC ← DR	DRTAC
101	AR ← DR(0-10)	DRTAR
110	AR ← PC	PCTAR
111	M[AR] ← DR	WRITE

F2	Microoperation	Symbol
000	None	NOP
001	AC ← AC - DR	SUB
010	AC ← AC ∨ DR	OR
011	AC ← AC ∧ DR	AND
100	DR ← M[AR]	READ
101	DR ← AC	ACTDR
110	DR ← DR + 1	INCDR
111	DR(0-10) ← PC	PCTDR

F3	Microoperation	Symbol
000	None	NOP
001	AC ← AC ⊕ DR	XOR
010	AC ← AC'	COM
011	AC ← shl AC	SHL
100	AC ← shr AC	SHR
101	PC ← PC + 1	INCPC
110	PC ← AR	ARTPC
111	Reserved	

CD	Condition	Symbol	Comments
00	Always = 1	U	Unconditional branch
01	DR(15)	I	Indirect address bit
10	AC(15)	S	Sign bit of AC
11	AC = 0	Z	Zero value in AC

BR	Symbol	Function
00	JMP	CAR ← AD if condition = 1
		CAR ← CAR + 1 if condition = 0
01	CALL	CAR ← AD, SBR ← CAR + 1 if condition = 1
		CAR ← CAR + 1 if condition = 0
10	RET	CAR ← SBR (Return from subroutine)
11	MAP	CAR(2-5) ← DR(11-14), CAR(0,1,6) ← 0