SECTION A

MULTIPLE-CHOICE QUESTIONS (30 MARKS)

(INSTRUCTION: Please answer all 20 questions on the answer sheet on page 16)

PART I (each question contribute 1 mark)

1. The following are **TRUE** about the design of an asynchronous counter, **EXCEPT**:
   A) Design a decoder to decode the mod of the truncated sequence.
   B) Connect all inputs of the flip-flops with the HIGH signal.
   C) Connect all flip-flops to a common clock.
   D) The flip-flops must be in a cascaded arrangement.

2. How many invalid states for a MOD 5 of 4-bit asynchronous counter have?
   A) 4
   B) 5
   C) 11
   D) 16

3. Consider a 4-bit ripple counter using J-K flip-flops with a negative edge. If the clock of the last flip-flop is connected to Q_2, what is the counting direction for the counter?
   A) Count up.
   B) Count down.
   C) Count up-down.
   D) Count up or down.

4. What is the J-K flip-flop state in the excitation table when $Q_n = Q_{n+1} = 1$?
   A) J = 0, K = X

B) J = 1, K = X

C) J = X, K = 1

D) J = X, K = 0

5. If the counter never goes to the maximum count from any state in order, and goes back to the first count, this counting sequence is referred to as _____.

A) Recycle sequence.

B) Truncated sequence.

C) Arbitrary sequence.

D) Saturated sequence.

6. Consider the state diagram of a synchronous counter, as shown in Figure 1. Choose the c**orrect statement** describing the counter.

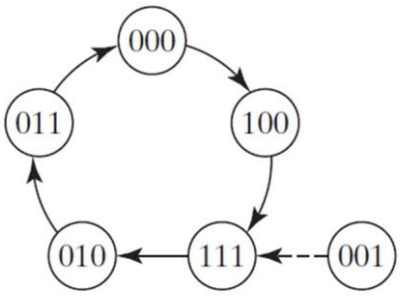


Figure 1

A) This is representing an arbitrary sequence counting.

B) The counter also known as MOD-6 counter.

C) This is also known as an up-down synchronous counter.

D) The counter is using 3 different flip-flops.

7. Consider 3 cascaded decade counter performing a frequency divider. If the original clock is 5MHz, what is the output frequency for the second counter?

   A) 1667.7MHz

   B) 0.05MHz

   C) 500KHz

   D) 5KHz

8. Select the best answer for this question.

   A) digital multiplexer is a combinational circuit that selects _____ A) One digital information from several sources and transmits the selected one.

   B) Much digital information and convert them into one.

   C) Many decimal inputs and transmits the selected information.

   D) Many decimal outputs and accepts the selected information.

9. Figure 2 shows a 4-bit binary-to-gray converter. Determine the logic condition of the gray code at the outputs (W X Y Z) if the binary inputs are 1011_2.

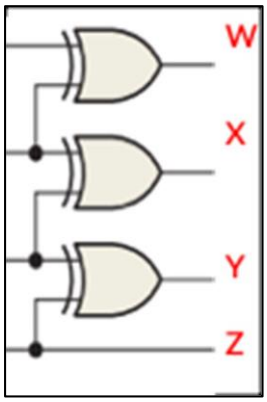


Figure 2

   A) 0111

   B) 0101

   C) 1111

   D) 1110

10. Which of the following choices correctly completes the statement?
SR is a register in which binary data can be stored, and this data can be shifted to the left or right when a signal is applied. SR stands for:

A) Storage Register

B) Shift Register

C) Sequential Register

D) System Register

PART II (each question contribute 2 marks)

11. Consider the Table 1 shows a portion of the T flip-flop transition table. Choose the correct input of the flip-flop.

Table 1

	Present State			Next State			FF Transition Table		
	Q_2	Q_1	Q_0	Q_{2+}	Q_{1+}	Q_{0+}	T_2	T_1	T_0
i.	1	0	0	1	0	1	0	0	1
ii.	0	1	0	1	1	1	1	1	1
iii.	1	1	0	0	0	0	1	1	0
iv.	0	0	1	0	1	1	0	1	0

A) i, ii, iii

B) i, ii, iv

C) i, iii, iv

D) ii, iii, iv

12. Assume that a 4-bit serial in/serial out (SISO) shift register is initially clear. It enters 1 1 0 0 data in serial order. What will be the 4-bit pattern after the second clock pulse? (MSB bit first).

A) 1100

B) 1111

C) 0011

D) 0000

13. Figure 3 illustrates a 3-by-8 decoder with 2 enable inputs G1 (active-high), and G2' (active-low). All inputs must be active to enable the decoder to function. Determine the correct input and output logic condition of the decoder.

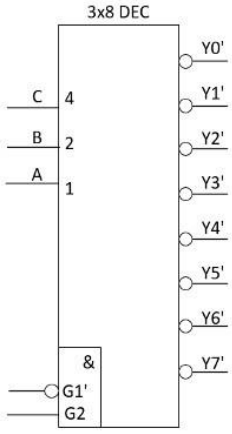


Figure 3

A) G1'=0, G2=1, CBA = 010, Y_7'=1, Y_6'=1, Y_5'=0, Y_4'=1, Y_3'=1, Y_2'=0, Y_1'=1', Y_0'=1

B) G1'=1, G2=0, CBA = 101, Y_7'=1, Y_6'=1, Y_5'=0, Y_4'=1, Y_3'=1, Y_2'=0, Y_1'=1', Y_0'=1

C) G1'= 0 G2=1, CBA = 111, Y_7'=1, Y_6'=1, Y_5'=1, Y_4'=1, Y_3'=0, Y_2'=1, Y_1'=1', Y_0'=1

D) G1'=0 G2=1, CBA = 110, Y_7'=1, Y_6'=0, Y_5'= 1, Y_4'=1, Y_3'=1, Y_2'=1, Y_1'=1', Y_0'=1

14. Figure 4 shows a 4-bit parallel adder logic diagram. Determine the logic conditions at all outputs if the logic conditions of the inputs are

$A_3 – A_0$ = 0111, $B_3 – B_0$ = 0110, C_0 = 1

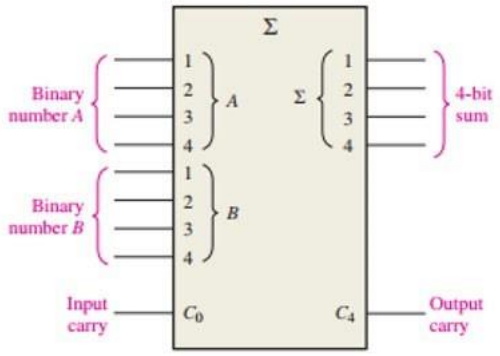


Figure 4

A) $S_3 S_2 S_1 S_0 = 1100, C_4 = 1$

B) $S_3 S_2 S_1 S_0 = 1101, C_4 = 0$

C) $S_3 S_2 S_1 S_0 = 1101, C_4 = 1$

D) $S_3 S_2 S_1 S_0 = 1100, C_4 = 0$

15. Figure 5 shows a logic diagram of IC 74HC147, a decimal-to-BCD encoder, which is a priority encoder (HPRI - highest value input has priority). All of its 10 inputs and 4 outputs are active-LOW.

Choose the correct logic conditions at its outputs for a given binary combination at its inputs.

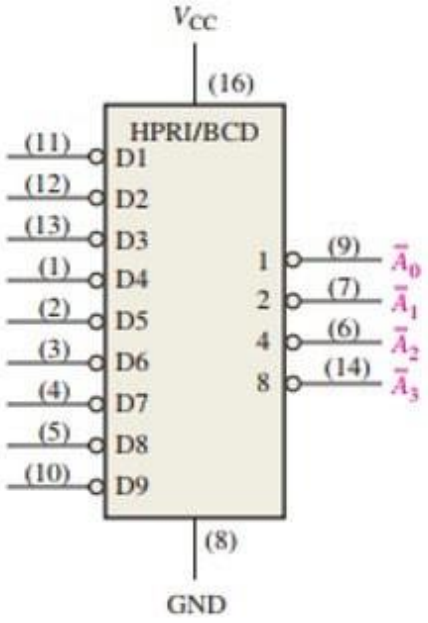


Figure 5

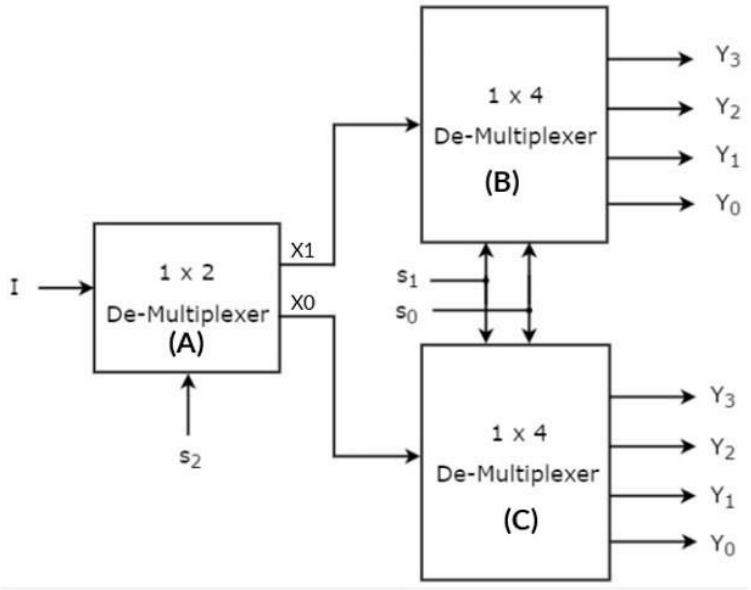
A) Input: I9 = 1, I8 = 0, I7 = 0, I6 = 0, I5 = 0, I4 = 0, I3 = 0, I2 = 0, I1 = 0
Output: A3’ = 1, A2’ = 0, A1’= 0, A0’ = 1

B) Input: I9 = 1, I8 = 1, I7 = 0, I6 = 1, I5 = 0, I4 = 1, I3 = 1, I2 = 1, I1 = 1
Output: A3’ = 1, A2’ = 0, A1’= 0, A0’ = 0

C) Input: I9 = 0, I8 = 0, I7 = 0, I6 = 1, I5 = 0, I4 = 1, I3 = 0, I2 = 0, I1 =0
Output: A3' = 0, A2' = 1, A1'=1, A0' = 0

D) Input: I9 = 1, I8 = 1, I7 = 1, I6 = 1, I5 = 0, I4 = 1, I3 = 0, I2 = 0, I1 =0 Output: A3' = 0, A2' = 0, A1'=1, A0' = 1

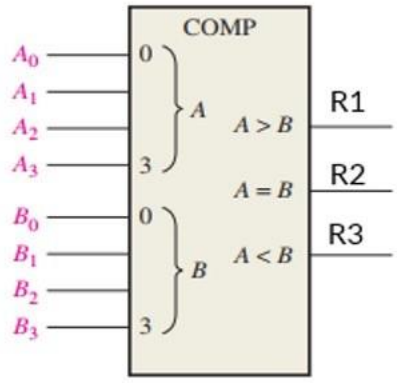
16. Figure 6 shows a block diagram of a network of demultiplexer. Where will data at I be transmitted to if inputs S_2 S_1 S_0 = 101?



A) Y1 of DeMux - B
B) Y1 of DeMux - C
C) Y2 of DeMux - B
D) Y2 of DeMux–C

Figure 6

17. Figure 7 shows a logic symbol of a 4-bit comparator. Determine the logic conditions at RI R2 and R3 if the logic conditions at the inputs
are: A_3 A_2 A_1 A_0 = 1011 and B_3 B_2 B_1 B_0 = 0011



A) R1=LOW, R2=R3=HIGH

B) R1=R2=LOW, R3=HIGH

C) R1=HIGH R2= R3=LOW

D) R1=HIGH R2= LOW R3=HIGH

Figure 7

18. Figure 8 shows a 9-bit binary parity bit checker/ generator logic symbol.

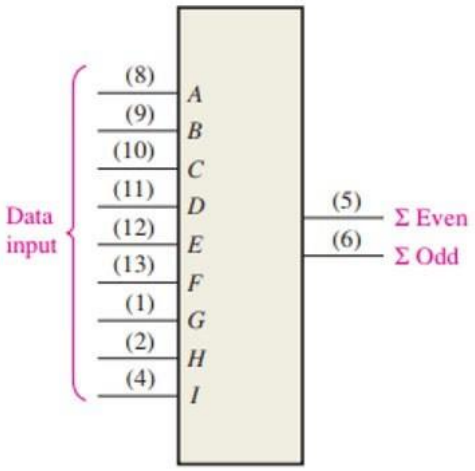
- When the device is used as an even/odd parity checker, the output will produce logic HIGH at relevant outputs, as shown in the device function table in Table Q8.
- When used as even parity generator, the device uses the parity bit produced at output $\sum$ **odd**. Alternatively, when used as an odd parity generator, the device uses the parity bit produced at output $\sum$ **even**. They showed this function Table 8.

Determine the logic condition of the outputs if the logic condition at the inputs are 101101011 and the device functions as:

(i) even parity checker

(ii) odd parity generator

Table 8



Number of Inputs A–I that Are High	Outputs Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

Figure 8

A) (i) Even =1, Odd = 0 (ii) Even=1, Odd=0

B) (i) Even =1, Odd = 0 (ii) Even=0, Odd=1

C) (i) Even =0, Odd = 1 (ii) Even=0, Odd=1

D) (i) Even =0, Odd = 1 (ii) Even=1, Odd=0

19. Refer to the shift register in the following the Figure 9. For SIPO, determine the correct output.

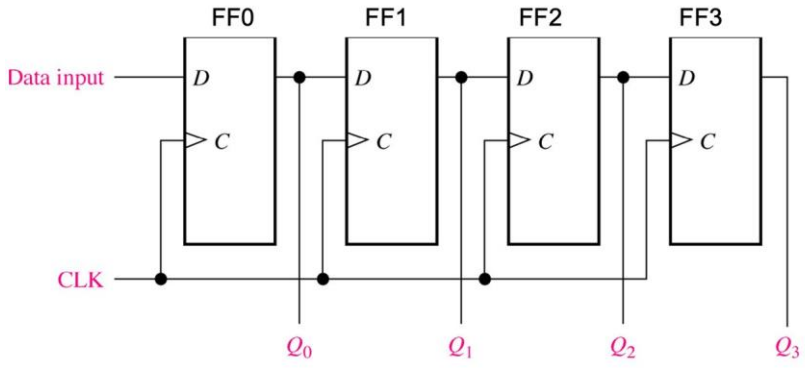


Figure 9

A) Q_3 only

B) Q_2 and Q_3 only

C) Q_1, Q_2 and Q_3 only

D) Q_0, Q_1, Q_2 and Q_3

20. Refer to the Johnson Counter in the following Figure 10. If the referred counter is initially at 0 0 0 0 state, determine the state of A B C D after 6^{th} clock.

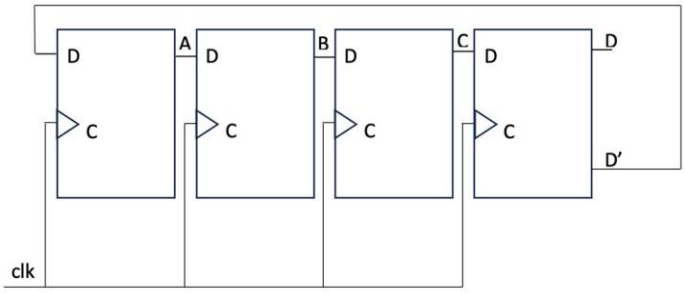


Figure 10

A) 1 1 1 1

B) 0 1 1 1

C) 0 0 1 1

D) 0 0 0 1

SECTION B

STRUCTURED QUESTIONS (70 MARKS)

(INSTRUCTION: Please answer all 5 questions in the answer booklet provided.)

QUESTION 1 [*10 Marks*]

Consider a 4-bit count up ripple counter is designed using J-K flip-flop with negative edge triggered clock.

(a) To transform the 4-bit count up ripple counter into a MOD 5 counter, create a decoder using a single gate. Sketch the complete design of the counter, ensuring the decoder is incorporated. Remember to include all the steps and calculations in your work.

[7 *Marks*]

(b) Draw the waveform outputs for 8 clock cycles. Assume the initial value of Qi = 0.

[3 *Marks*]

QUESTION 2 [*15 Marks*]

Consider a sequential circuit of a counter, as shown in Figure 11. It has an input *X*, an output *Y*, and two state variables Q_1Q_0. Generate the complete state diagram by analysing the circuit in Figure 11 . Show all your steps clearly.

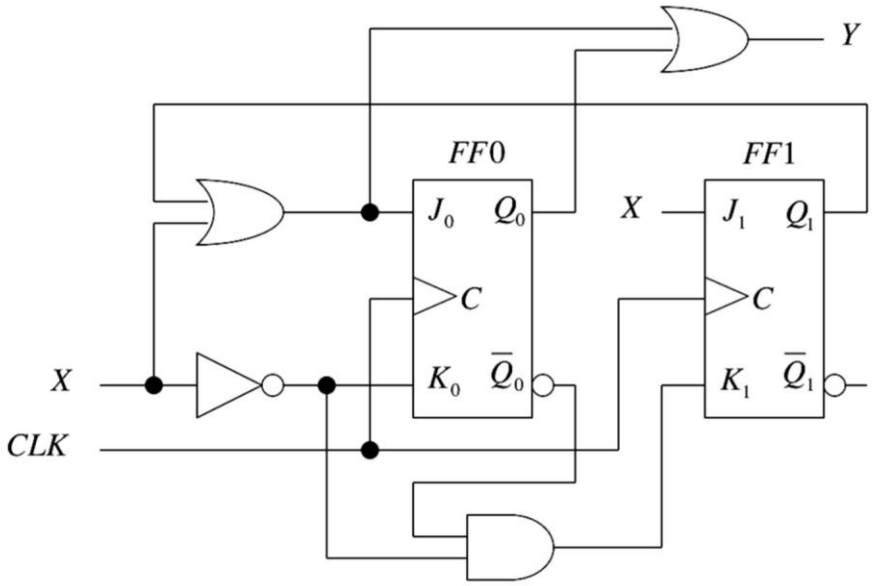


Figure 11

(a) What are the inputs Boolean expression for each flip-flop and the output Y?

[3 *Marks*]

(b) Derive the next-state equations by converting these excitation equations into JK flip-flop characteristic equations. [4 Marks]

(c) Produce a Next State Table. [4 Marks]

(d) Draw the state diagram for the counter. [4 Marks]

QUESTION 3 [*15 Marks*

Figure 12 displays a 1-to-8 multiplexer. Utilize the MUX to implement the given Boolean expression by assigning the select inputs of the MUX accordingly, where S2 is linked to D, S1 is linked to C, and S0 is linked to B.. Show all your workings and label all inputs and outputs of the MUX clearly.

$$f(D,C,B,A) = \overline{A}(C + \overline{DB}) + (\overline{B + \overline{A}C})$$

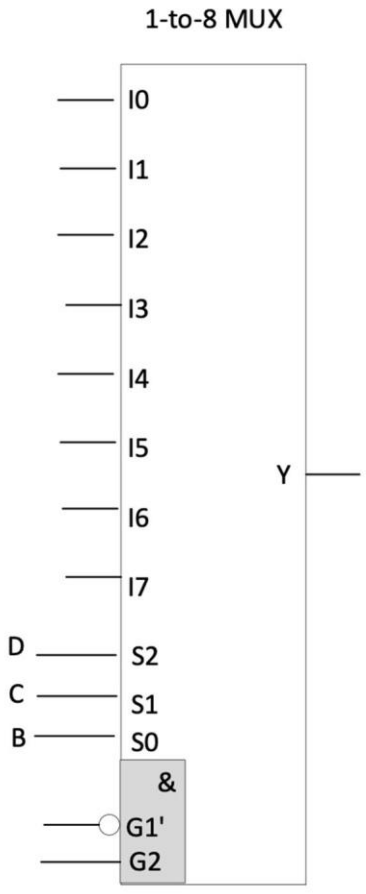


Figure 12

QUESTION 4 [12 *Marks*

Figure 13 shows a network of sequential logic devices consisting of gated D-latch and J-K flip-flops. Draw the digital waveforms of **Q1, Q2 and Q3** in the Appendix B Figure 14 on page 17.

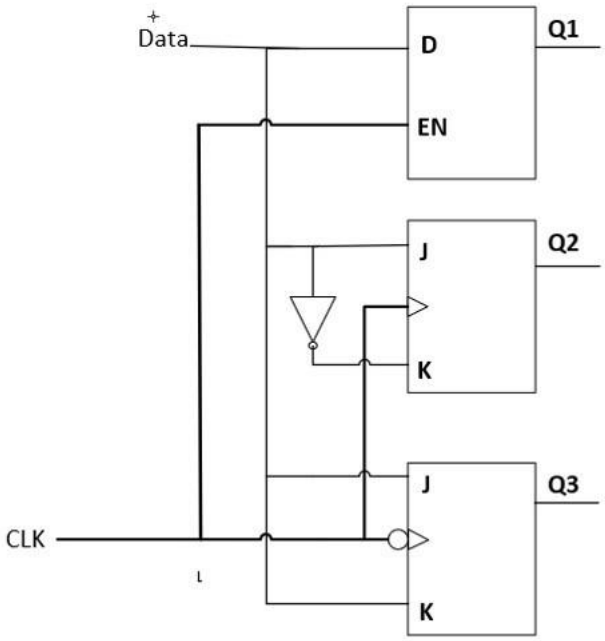


Figure 13

QUESTION 5 [18 Marks]

(a) Initially at t_0, a 5-bit SIPO shift register is cleared. Then, at t_1, the data word 19_{10} is serially entered. LSB is shifted in first.

i) Draw the circuit for a 5-bit SIPO using D flip-flop.

[5 *Marks*]

ii) Derive the content of the SIPO shift register at t_3? Show your works in a table form.

[3 *Marks*]

iii) Determine at what I can read clock cycle at the output and state the output.

[2 *Marks*]

(b) Answer the following questions based on a Johnson counter.

i) Draw the logic diagram for a MOD 8 Johnson counter.

[4 *Marks*]

ii) Write the counting sequence in a table form. Initially, the content of all flip-flops is binary '0'.

[4 *Marks*]

------- End of Question -------

Appendix A

NAME :				MARKS
MATRIC NO.:		SECTION:		

Example: =A=  =C= =D=

1)	=A=	=B=	=C=	=D=
2)	=A=	=B=	=C=	=D=
3)	=A=	=B=	=C=	=D=
4)	=A=	=B=	=C=	=D=
5)	=A=	=B=	=C=	=D=
6)	=A=	=B=	=C=	=D=
7)	=A=	=B=	=C=	=D=
8)	=A=	=B=	=C=	=D=
9)	=A=	=B=	=C=	=D=
10)	=A=	=B=	=C=	=D=
11)	=A=	=B=	=C=	=D=
12)	=A=	=B=	=C=	=D=
13)	=A=	=B=	=C=	=D=
14)	=A=	=B=	=C=	=D=
15)	=A=	=B=	=C=	=D=
16)	=A=	=B=	=C=	=D=
17)	=A=	=B=	=C=	=D=
18)	=A=	=B=	=C=	=D=

19)	=A=	=B=	=C=	=D=
20)	=A=	=B=	=C=	=D=

Appendix B

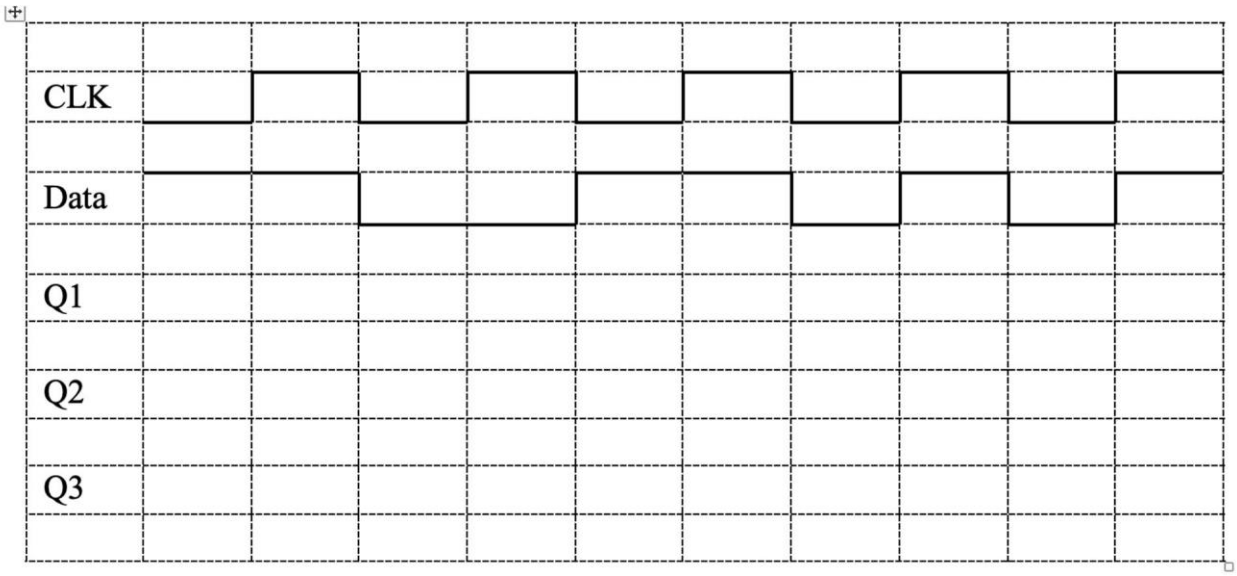


Figure 14 Answer for structured question Part B Question 4