

SECTION A

MULTIPLE CHOICE QUESTIONS (18 MARKS)

(INSTRUCTION: Please answer all 18 questions in the answer booklet provided.)

- 1) Computer _____ is attributes that visible to _____ and have direct impact on logical execution of a program, while computer _____ refer to the _____ units and their interconnections to realize the computer systems specification.
- A) architecture, programmer, organization, operational
 B) organization, operational, architecture, programmer
 C) systems, software, hierarchy, components
 D) engineering, systems, engineering, systems
- 2) The following specification is referring of Intel x86 Architecture evolution.

	Pentium III	Pentium 4	Core 2 Duo	Core i7 EE 4960X
Introduced	1999	2000	2006	2013
Clock speeds	450–660 MHz	1.3–1.8 GHz	1.06–1.2 GHz	4 GHz
Bus width	64 bits	64 bits	64 bits	64 bits
Number of transistors	9.5 million	42 million	167 million	1.86 billion
Feature size (nm)	250	180	65	22
Addressable memory	64 GB	64 GB	64 GB	64 GB
Virtual memory	64 TB	64 TB	64 TB	64 TB
Cache	512 kB L2	256 kB L2	2 MB L2	1.5 MB L2/15 MB L3
Number of cores	1	1	2	6

Based on the specification, what can you say about recent Core i7 processors compared to earlier Intel x86 processors?

- I. Core i7 processor has the highest clock speed
 II. Core i7 processor has the fewest numbers of density transistors in CPU
 III. Core i7 processor has multi-level of Cache memory system
 IV. Core i7 processor has highest number of cores

- A) I and II
 B) I, II and III
 C) I, III, and IV
 D) I, II, III and IV

- 20222023 / 2

- 8) Which of the following statement is **FALSE** for floating-point multiplication?
- A) The exponent for both numbers will be added.
 - B) The exponent for both numbers will be multiplied.
 - C) The decimal point of numbers must be aligned during the operation.
 - D) The decimal point after the operation is the addition of the decimal point of each fraction number.
- 9) Which of the following statement is **TRUE** for precision floating point?
- A) The IEEE-754 floating point format for double precision is 63 bits.
 - B) The IEEE-754 floating point format for single precision is 31 bits.
 - C) The IEEE-754 floating point format for both single and double precision biased exponent has 3 fields – sign bit, biased exponent, and fraction.
 - D) The IEEE-754 floating point format for both single and double precision biased exponent is 8 bits.
- 10) What is the radix for this 197 integer constant?
- A) No radix
 - B) Octal
 - C) Decimal
 - D) Hexadecimal
- 11) Which of the following cannot be used as identifiers?
- I. xCount
 - II. @count
 - III. _count
 - IV. +count
- A) I only
 - B) II and IV
 - C) I and III
 - D) II, III and IV

- 12) Choose a **TRUE** statement for the following instruction:

SUB valA, valB

- A) Value in valA and valB can be in different data type.
- B) Value in valA will be subtracted with value in valB and the result will be stored in valA.
- C) Value in valB will be subtracted with value in valA and the result will be stored in valB.
- D) The assembler will generate error.

- 13) What is the final value stored in BX register after executing the following instructions:

MOV BX, 100h

SUB BX, 65h

ADD BX, 4h

- | | |
|---------|---------|
| A) 009B | C) 009E |
| B) 009C | D) 009F |

- 14) What is the effect when the EQU directive is used in the instruction below?

Sum EQU 200

- A) Finds the first occurrence of Sum and assigns value 200 to it
- B) Assigns 200 bytes of memory starting the location of Sum
- C) Re-assigns the address of Sum by adding 200 to its original address
- D) Replaces every occurrence of Sum with 200

- 15) Choose a **CORRECT** sequence in implementing Instruction Execution Cycle by CPU.

- A) Fetch operands, decode, fetch, execute, store output.
- B) Fetch operands, execute, fetch, decode, store output.
- C) Fetch, decode, fetch operands, execute, store output.
- D) Fetch, execute, fetch operands, decode, store output.

16) How many addresses does the following instruction have?

```
MOVE Y, A
SUB   Y, B
```

- A) One-address instruction
- B) Two-address instruction
- C) Three-address instruction
- D) No-address instruction

17) Identify the datatype that can be represented using the following format?



- A) SDWORD
- B) DWORD
- C) QWORD
- D) SQWORD

18) Which of the following is not categorized under instruction types?

- A) Data processing
- B) Data storage
- C) I/O instructions
- D) Operands

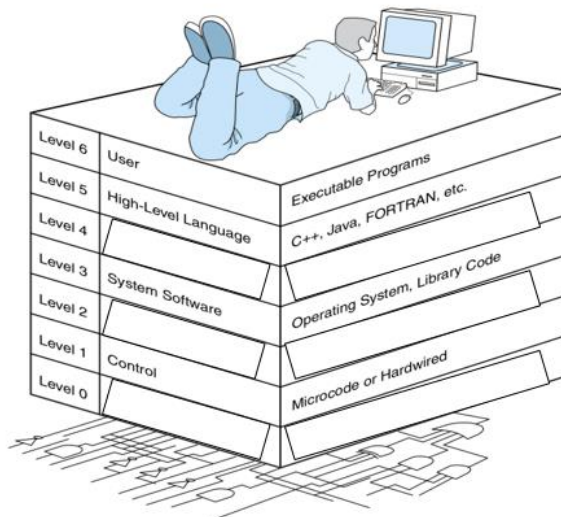
SECTION B

STRUCTURED QUESTIONS (52 MARKS)

(INSTRUCTION: Please answer all 6 questions in the answer booklet provided.)

QUESTION 1 [6 Marks]

- (a) Modern computer architecture was designed based on Von Neumann model. Briefly explain, what are the **THREE (3)** characteristics of Von Neumann model. [3 Marks]
- -
 -
- (b) In a complex computer system, divide and conquer approach is known as virtual machine abstraction layers as shown in the following figure. Briefly, explain what are the abstraction layers at level 4, level 2, and level 0 are. [3 Marks]



- i) Level 4: _____
- ii) Level 2: _____
- iii) Level 0: _____

QUESTION 2 [10 Marks]

Given an equation for w is:

$$w = p + q ;$$

where: $p = (-65_{10}) + 10010_2$; and $q = 9_{16} / 3_{10}$.

Based on this equation, answer the following questions. Show all the calculation works.

- (a) Calculate the value of p (in decimal) using 2's complement arithmetic. [3 Marks]
- b) Calculate the value of q (in decimal) using 4-bit binary arithmetic based on the steps given in Algorithm 1 by completing the calculation of all iterations in Table 1. [6 Marks]

Steps:
1 – Remainder (R) = R – D
2 – test new R
 2a - If ≥ 0 then Shift left Q (add 1 at LSB)
 2b - If < 0 then $R = D + R$, Shift left Q (add 0 at LSB)
3 – shift D right
 All bits done?
 If still $< (\text{max bit} + 1)$, repeat
 If $= (\text{max bit} + 1)$, stop

Algorithm 1: The Division Algorithm using the Hardware.

Table 1: The Division Iterations using the Hardware.

Iteration	Steps	Quotient (Q)	Divisor (D)	Remainder (R)
0	Initial value			

- (c) Find the value of w (in decimal and binary). [1 Mark]

QUESTION 3 [7 Marks]

For the following floating-point representation,

- (a) Identify the decimal number represented by this single precision float. Show your works. [4 Marks]

0	10000111	0000010.....0
---	----------	---------------

- (b) Perform the addition in binary. Show the workings and result in normalized form.

Notes: Round the fraction to 3 decimal digits for fraction) [3 Marks]

$$110.110 \times 2^{-3} + 10.011 \times 2^{-5}$$

QUESTION 4 [5 Marks]

Based on the given program, write the correct answer for the following program with CORRECT size format.

```
.data
mydata WORD 34, 1011b, 34h
mydata2 BYTE 23h, 2 DUP(1100b), 67q

.code
main PROC
    MOV AX, mydata           ; (a) AX = _____h
    MOV BX, AX               ; (b) BX = _____h
    MOV CL, mydata2+2        ; (c) CL = _____h
    MOV DX, mydata+5         ; (d) DX = _____h
exit
main ENDP
```

- (a) AX = _____h
 (b) BX = _____h
 (c) CL = _____h
 (d) DX = _____h

QUESTION 5 [9 Marks]

- (a) Find the data for the sequence of bytes (in hexadecimal) in memory. [5 Marks]

MyData WORD 1234, 2 DUP(1011b), 35q, 46h

Offset:	Value:	Offset:	Value:
0000:	<input type="text"/>	0005:	<input type="text"/>
0001:	<input type="text"/>	0006:	<input type="text"/>
0002:	<input type="text"/>	0007:	<input type="text"/>
0003:	<input type="text"/>	0008:	<input type="text"/>
0004:	<input type="text"/>	0009:	<input type="text"/>

- (b) Declare a string variable as **var** containing the word “MID TERM TEST” repeated 300 times and initialize it as null terminated string. [2 Marks]
- (c) Briefly describe the output for DumpRegs function. [2 Marks]

QUESTION 6 [15 Marks]

- (a) Given a coding of assembly language and its initial *DumpRegs* contents as shown in Figure 4.1 and Figure 4.2 respectively. Consider the first location of the data in the memory is 00406000.

1	.data				
2	MyArray1	BYTE	3h, 45h, 67h, 89h		
3	MyArray2	WORD	101h, 23h, 4567h		
4					
5	.code				
6	main PROC				
7	mov	ECX,	0		
8	mov	EAX,	0		
9					
10	mov	ESI, OFFSET MyArray1		; (i) ESI =	_____
11	mov	EDI, OFFSET MyArray2.		; (ii) EDI =	_____
12	mov	CL, [ESI]		; (iii) CL =	_____
13	mov	BX, word ptr [EDI+1]		; (iv) BX =	_____
14	add	ESI, 1000b			
15	mov	EDX, (ESI)		; (v) EDX =	_____
16	L1:				
17	mov	BX, MyArray2[EAX+2]		; (vi) BX =	_____
18	inc	EAX			
19	call	dumpregs			
20	LOOP	L1			
21	exit				

Figure 4.1

EAX=7000A080	EBX=00001B20	ECX=4F020123	EDX=00400004
ESI=00400000	EDI=00400008	EBP=0012FF94	ESP=0012FF8C
EIP=0040103D	EFL=00000246	CF=0	SF=0 ZF=1 OF=0

Figure 4.2

- i) How many bytes of the memory will be used to allocate the data for MyArray1 and MyArray2, respectively? [1 Mark]

- i) Write the content of each registers labeled as (i) – (vi) in Figure 4.1 as the instructions execute in sequence up to line 17. [6 Marks]

- ii) What is the value of the register used for the counter? [2 Marks]

- iii) What will be the final value of BX after completing the loop function? [2 Marks]

- iv) What are the addressing modes used in lines 10, 14, 15, and 17? [4 Marks]

----- End of Question -----
GOOD LUCK !