SECTION A

MULTIPLE CHOICE QUESTIONS (20 MARKS)

(INSTRUCTION: Please answer all 20 questions in the answer sheet on page 7.)

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1) Which of the following register is **NOT** known as control register?
   A) MAR
   B) EBX
   C) IR
   D) MBR

2) The following operations can cause interrupt, **EXCEPT**:
   A) A user break (such as Control+C) is issued.
   B) I/O is requested by the user or a program.
   C) Arithmetic with Overflow Flag (OF) is zero.
   D) A critical error occurs such as out of memory.

3) The instruction processing consists of the following stages, **EXCEPT**:
   A) Fetch cycle.
   B) Waiting cycle.
   C) Interrupt cycle.
   D) Execute cycle.

4) One instruction tries to write an operand before it is written by the previous instruction. This scenario is called _____.
   A) anti-dependency
   B) data dependency
   C) true dependency
   D) false dependency

5) Which of the following is **FALSE** about Control Hazards?

A) Major problems in designing an instruction pipeline is assuring a steady flow of instructions to initial stages of the pipeline.

B) Branch difficulty bring instructions into pipeline that will not subsequently discarded.

C) Branch difficulty occurs when the pipeline makes the wrong decision on a branch prediction.

D) Branch difficulty occurs when the pipeline change the PC value.

6) Which of the following statement is **FALSE**?

A) The control memory is programmed to update the required micro-operations.

B) Microprogrammed is systematic and any changes can be done through the micro-program.

C) Hardwired is a combinational circuit.

D) Hardwired is a fast operation that implemented direct to hardware.

7) The following components are the inputs of a control unit, **EXCEPT**:

A) Instruction Register

B) Instruction Pointer

C) Flags

D) Clock

8) For every single micro-operation, the control unit is allowed to generate a set of _____.

A) control memory

B) microprogram

C) control signals

D) registers

9) Which of the following below is **NOT** categorized under internal memory?

A) Register
B) Control memory
C) Cache
D) Virtual memory

10) Main memory is made up of _____ integrated circuit, but a portion of the memory maybe constructed with _____.

A) RAM, ROM
B) Cache, RAM
C) ROM, registers
D) RAM, virtual memory

11) Choose an advantage of LOI.

A) Produce memory interference.
B) Provide high reliability compared to HOI.
C) Easy memory extension.
D) Failure of any single bank will affect the whole system.

12) A main memory contains 32 words while the cache has only 8 words. Using direct address mapping, identify the tag size (bits) of the main memory address.

A) 2
B) 3
C) 5
D) 16

13) Suppose a main memory is mapped to a 4-way set associative cache having 16 blocks where each block contains 8 words. If the memory address is 1100111111010_2, what is the set used in the cache memory (in decimal)?

A) 2
B) 3
C) 4
D) 6

14) To improve the performance of cache, one must increase the hit ratio by using a better:

i. replacement algorithms.
ii. mapping algorithm.
iii. coding practices.
iv. strategies for write operations.

A) i and ii.
B) iiiand iv.
C) ii, iii and iv.
D) All of the above.

15) READ and WRITE are two common signals in processor communication with I/O module. These two signals are _____.

A) address signal
B) data signal
C) flag signal
D) control signal

16) The following statements are related to which data storage technology?

- *Lifetime estimation of media is 100 years.*
- *Data is recorded in a single spiral track, starting from the centre of the disk and spanning outward.*

A) Magnetic disk
B) Magnetic tape
C) Optical disk
D) RAID

17) The functions for I/O processors in channel I/O include:

i. Negotiates protocols.
ii. Issues device commands.
iii. Translates storage coding to memory coding..
iv. Delegates task for large files transfer to the host CPU

A) i, ii and iv.
B) i, ii and iii.
C) iii and iv.
D) ii and iii.

18) CPI can be defined as _____.

A) execution time for a program
B) execution time per clock cycle
C) average number of clock cycles per instruction
D) average instruction executed for the program

19) The following statement is **FALSE** regarding Performance Benchmarking.

A) It is the science of making objective assessments of the performance of one system over another.

B) It is a metric that is most often used by computer vendors to promote their systems' alleged superiority to all others.

C) It is the most common approach to assessing processor and computer system performance.

D) It is useful for assessing performance improvements obtained by upgrading a computer or its components.

20) The following statement is **TRUE** regarding Weighted Average based on the information given in Table 1.

Table 1.

Program	**Execution Frequency**	**System X execution time (sec)**	**System Y execution time (sec)**
A	0.65	150	85
B	0.35	100	60

A) System X is about 74% faster than System Y for this particular workload.

B) System Y is about 74% faster than System X for this particular workload.

C) Program A is about 74% faster than Program B for this particular workload.

D) Program B is about 74% faster than Program A for this particular workload.

ANSWER SHEET FOR SECTION A

NAME :				MARKS
MATRIC NO.:		SECTION :		

Example: =A=  =C= =D=

1)	=A=	=B=	=C=	=D=
2)	=A=	=B=	=C=	=D=
3)	=A=	=B=	=C=	=D=
4)	=A=	=B=	=C=	=D=
5)	=A=	=B=	=C=	=D=
6)	=A=	=B=	=C=	=D=
7)	=A=	=B=	=C=	=D=
8)	=A=	=B=	=C=	=D=
9)	=A=	=B=	=C=	=D=
10)	=A=	=B=	=C=	=D=
11)	=A=	=B=	=C=	=D=
12)	=A=	=B=	=C=	=D=
13)	=A=	=B=	=C=	=D=
14)	=A=	=B=	=C=	=D=
15)	=A=	=B=	=C=	=D=
16)	=A=	=B=	=C=	=D=
17)	=A=	=B=	=C=	=D=
18)	=A=	=B=	=C=	=D=
19)	=A=	=B=	=C=	=D=
20)	=A=	=B=	=C=	=D=

SECTION B

STRUCTURED QUESTIONS (80 MARKS)

(INSTRUCTION: Please answer all 7 questions in the provided answer booklet.)

QUESTION 1 [15 *Marks*]

ISA format was defined with 16 bit size and has the following format:

4 bit (*opcode*)	12 bit (*operand*)

Opcode: 0001_2 = MOV instruction, 0101_2 = ADD instruction

Trace the execution of instructions starting from address 300h to 301h as shown in Table 2. Complete (write) the contents for Table 3 in your answer booklet by showing all the related changes in CPU registers (control and general purpose registers) as well as the micro-operations for each Clock.

Table 2.

Memory Address (hex)	Memory Content (hex)	Instruction Data
300	1005	`MOV AX, 5h`
301	5945	`ADD AX,Val1`
302	1946	`MOV Val2,AX`
945	0006	
946	0007	

Table 3.

Clock	IP/PC	MAR	MBR	IR	AX	Micro-operations
t_0						
t_1						
…						

QUESTION 2 [10 *Marks*]

Figure 1 shows the segments of pipeline whereby each delay time is as follow:

- S1: 50 *ns*
- S2: (x +1) *ns*
- S3: 3x *ns*
- S4: (3+2x) *ns*
- S5: x *ns*

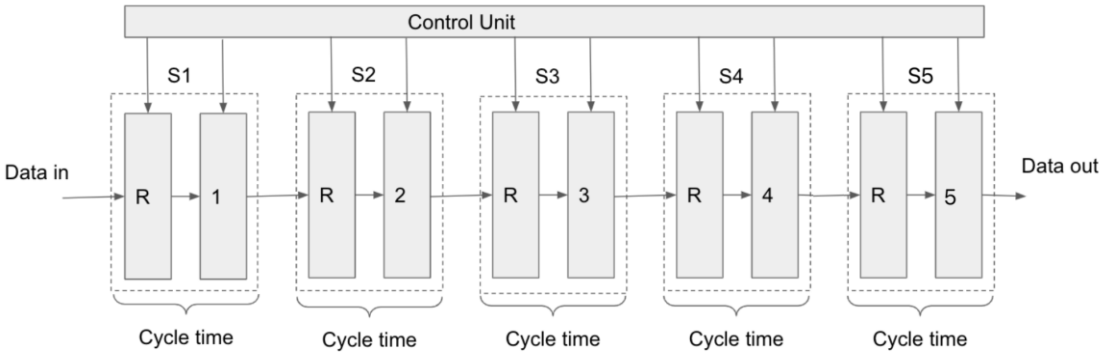

Figure 1.

The delay time for the interface register is 5ns.

(a) Calculate the delay time, x for S5 if the execution of 100 tasks using non pipeline is 8000 ns. [3 *Marks*]

(b) Calculate the total cycle time for non pipeline and pipeline. [2 *Marks*]

(c) Calculate the real speedup. [2 *Marks*]

(d) Based on the following instruction set, answer the following questions.

```
I1:        MOV AX, BX
I2:        ADD BX, CX
I3:        INC CX
I4:        JMP SAYA
I5:        MOV AX, 15
I6:        INC, BX
.......
I13: SAYA DEC AX
```

i) Consider 5 segments in a pipeline with branching problem. How many NOP needed to solve branching problem in the pipeline? [1 *Mark*]

ii) Rewrite the new instruction set by including NOP. [2 *Marks*]

QUESTION 3 [10 *Marks*]

Given the computer instruction fields as follow:

1011	1001……1000

(a) If the mapping bits from instruction code to microinstruction address are 01 xxxx 01. Identify the microinstruction address. [2 *Marks*]

(b) Given the control memory contents are as shown in Figure 2. Identify the micro-instruction routine from the address in Question 3(a). The control memory routine starts with the address 01100001. [2 *Marks*]

01100001	SUB routine …
01xxxx01	AND routine …
01xxxx01	MOV routine …
01xxxx01	MUL routine …
01xxxx01	JUMP routine …

Figure 2.

(c) Figure 3 shows the control unit microarchitecture. Name the components labeled as X and Y. Then, describe the function of all 4 components shown in the figure. [6 *Marks*]

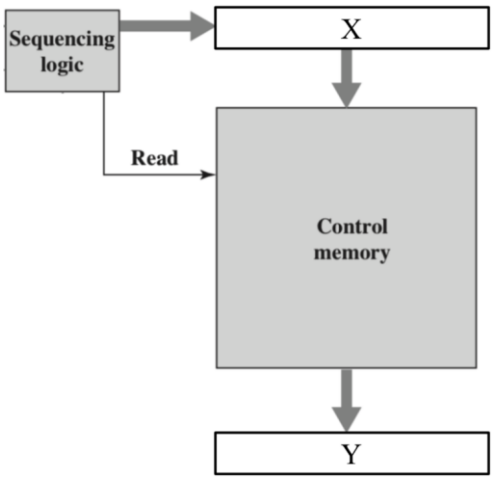

Figure 3.

QUESTION 4 [10 *Marks*]

(a) How many blocks are required for 256Kbit of program to be slotted into a main memory with the size of 8 bits of memory word and 8 words per block? [3 *Marks*]

(b) An address of 9Dh is stored in 2 memory banks using HOI.

i) Determine its bank capacity in bytes and number of bit(s) for bank address. [3 *Marks*]

ii) Draw the memory banks with the respective memory bank addresses. [4 *Marks*]

QUESTION 5 [15 *Marks*]

(a) Consider a 16 words direct mapped cache as shown in Table 4.

Table 4.

	(i)	(ii)	(iii)	(iv)	(v)	(vi)
Addresses	1111011	1010010	1111011	1100010	1100010	1010010
Hit or miss						
Read or write						

i) Determine the bits for tag field. Show your working. [2 *Marks*]

ii) Reconstruct (complete) Table 4 in your answer booklet and write the cache *miss* or *hit*, and the operation *read* or *write* in the columns labeled as (i) to (vi), which are responds to a series of request (main memory address in binary). Assume that the cache initially is empty. [3 *Marks*]

(b) Supposed a computer using block direct mapped cache has 2^{20} words of main memory and a cache of 64 blocks, where each cache block contains 16 words.

i) Calculate the tag size (bits). Show your working. [2 *Marks*]

ii) Draw the main memory address format, which is containing a generated program address A743h. Label clearly with the content (binary) and length (bits) for each field. [3 *Marks*]

(c) Supposed a computer using fully associative mapping of a 2^{16} binary cache memory with each block is 8 words. If the content of tag and the word of the cache memory are B62h and 7h respectively, determine is the memory address in hexadecimal? Show your working. [2 *Marks*]

(d) Suppose a single cache fronting a main memory, which has 80 nanosecond access time, and the cache memory has access time 10 nanoseconds. Calculate the Effective Access Time (EAT) if the hit rate is 90%. Show your working. [3 *Marks*]

QUESTION 6 [10 *Marks*]

(a) List the advantages of Direct Memory Access (DMA) I/O as opposed to Interrupt-driven I/O? [4 *Marks*]

(b) Consider a server with RAID Level 3 is shown in the Figure 4. Determine the bit for data regeneration labeled as (i) to (v) in the figure. [2 *Marks*]

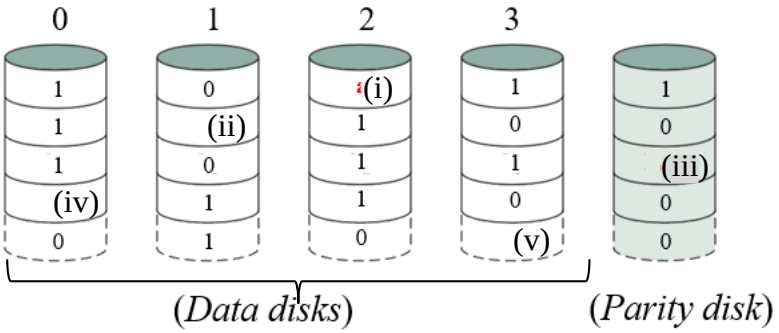

Figure 4.

(c) Figure 5 illustrates the bus timing diagram that describe bus operation for writing data to the disk drive. Reconstruct (complete) the contents of Table 5 in your answer booklet based on the listed Time, related to the process of writing data to the disk drive. [4 *Marks*]

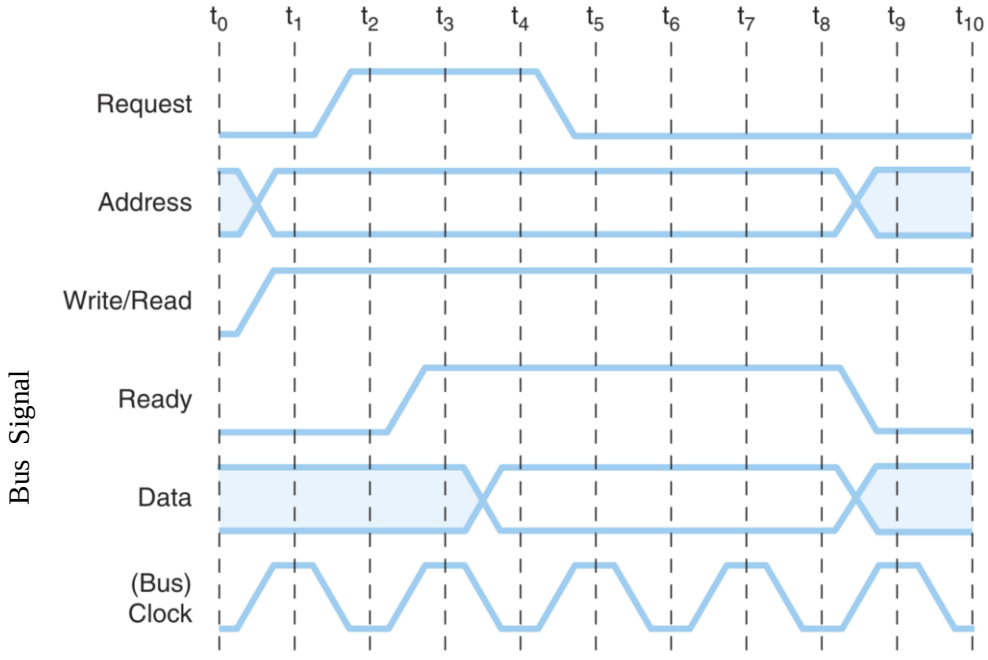

Figure 5.

Table 5.

Time	Bus Signal	Function
t_1		
t_2		
t_3		
t_{4-7}		

QUESTION 7 [10 *Marks*]

Consider a program that consists of four types of instruction is executed by Computer A and B is given in Table 6. Based on this table, answer the following questions.

Table 6.

	Computer A			Computer B		
Clock Rate	**600Ghz**			**800MHz**		
Instruction Type	**CPI**	**Instruction Mix (%)**	**Execution Time (sec)**	**CPI**	**Instruction Mix (%)**	**Execution Time (sec)**
Arithmetic	2	30	(i)	1	45	(v)
Move/Load	1	55	(ii)	2	40	(vi)
Jump	3	10	(iii)	4	5	(vii)
I/O	4	5	(iv)	5	10	(viii)

(a) Find the value of CPI and MIPS for Computer A and B. [4 *Marks*]

(b) Find the Execution Time of each Instruction Type for Computer A and B, which are labeled as (i) to (viii) in the table. [4 *Marks*]

(c) Compare the Relative Performance of the program for Computer A to B using the arithmetic and geometric means (Computer B is normalized to Computer A). Which computer is faster? [2 *Marks*]

---------- *End of Questions* ----------