EED2309 SEMICONDUCTOR DEVICES LABORATORY 9

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I am adding stuff here. I am now adding more stuff.

1 Theory

MOSFETs [Metal-Oxide Semiconductor Field-Effect Transistors] are a type of transistors. MOSFETs consist of two groups, n-channel and p-channel, both of which seperate into two as depletion and enhancement mode MOSFETs. This experiment will be focusing on n-channel enhancement mode MOSFETs, and throughout this report, we will be mentioning them as MOSFETs rather than clarifying the entire name.

Phyical structure of the MOSFET as shown in Figure 1 consists of a large **body**, made out of positively doped semiconductor material, upon which two heavily negatively doped regions are placed, called **source** and **drain**. Between these two heavily doped regions, seperated from the body with an insulating material, a conducting plate is placed, called the **gate**.

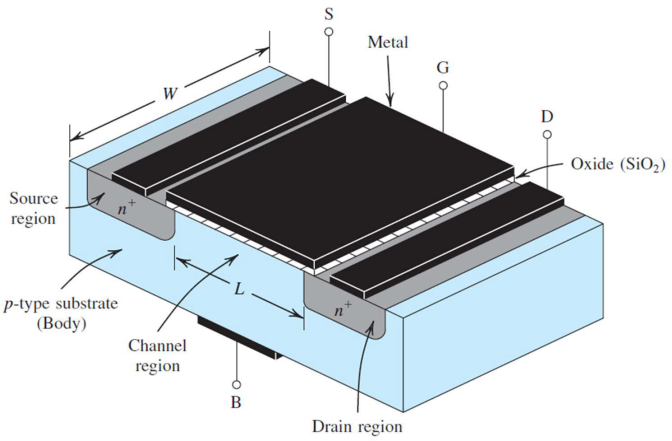


Figure 1: Physical structure of an n-channel enhancement mode MOSFET, [Sedra-Smith]

As can be seen, both drain and source forms a PN junction with the body, in opposite direction with respect to each other. Hence, if a voltage of either polarity were to be applied to drain and source, one of these PN junctions will be reverse biased, blocking any current flow between drain and the source.[1]This region is called the **cut-off** region, with very high effective resistance between drain and source.

Suppose for simplicity, the body and the source are tied together,[2] and every voltage is referanced from this potential. If a sufficiently high positive voltage is to be applied to the gate, the electric field created by this voltage between the gate plate and the body pulls electrons from the body and towards itself. This results in a high electron concentration between the drain and the source, essentially creating a channel filled with electrons between two negatively doped regions, thus creating a path for current to flow between the drain and source. This *sufficiently high* voltage is called **threshold voltage**, albeit, a bit ambigiously. For instance, the gate threshold voltage $V_{GS_{(th)}}$ denotes a voltage applied to the gate that allows an arbitrary but sufficient current flow from drain to source, at a specific drain voltage. **Zero bias threshold voltage** $V_{0_{th}}$ denotes the voltage required to fully form the channel.

[1]Ignoring junction breakdowns.

[2]As it usually is for discrete MOSFETs, though rarely is for IC MOSFETs.

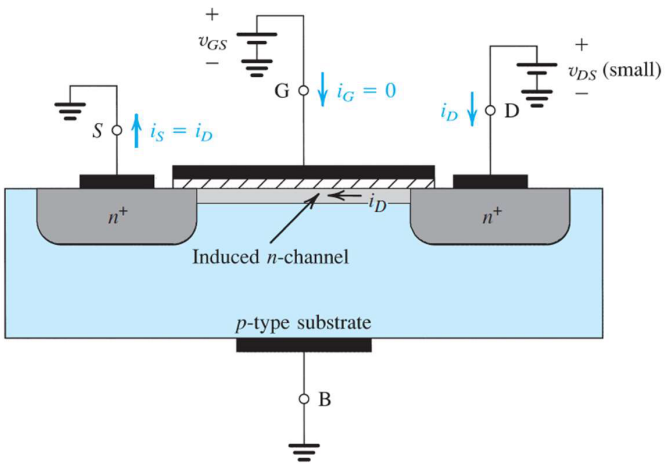


Figure 2

Either way, as the channel created, applying a small positive voltage at the drain results in an appreciable current flow. This **drain current**, or drain to source current, for relatively small drain voltage, appears to be linearly proportional to the drain voltage, hence the MOSFET behaves like a voltage controlled resistor, where its resistance is inversly proportional to the gate voltage, or more correctly, the difference between the gate voltage and the threshold voltage $V_{GS} - V_{th}$, which is conveniently named **overdrive voltage** V_{ov}. The relation is given below.

$$I_D = \left[\left(\mu_n C_{ox} \frac{W}{L}\right)\left(V_{GS} - V_{th} - \frac{1}{2}V_{DS}\right)\right] V_{DS} \tag{1}$$

The factor consisting of many terms is a constant that is determined by the physical structure of the MOSFET, let us define it as:

$$\kappa \triangleq \left(\mu_n C_{ox} \frac{W}{L}\right) \tag{2}$$

Then the expression looks simpler as:

$$I_D = \kappa \left(V_{GS} - V_{th} - \frac{1}{2}V_{DS}\right) V_{DS} \tag{3}$$

Which is a downward looking parabola. If we were to treat the V_{GS} as a constant, it can be seen that for sufficiently small V_{DS}, it looks like a line with its slope controlled by V_{GS}, and hence the voltage controlled resistor. This region, rather deceptively called the **linear region**, or the triode region.

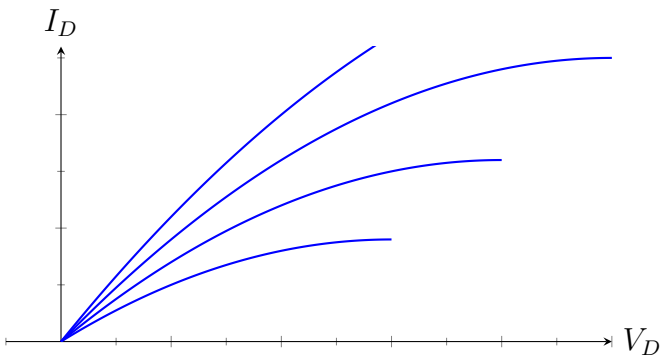


Figure 3: Linear Region Drain Current Curves, increasing V_{GS} at ccw.

It can be seen from the example plot that I_D loses its linear looking property as V_{DS} increases. Since the positive voltage applied to the drain, decreases the potential difference between the gate and the body near the drain, the channel narrows towards the drain, hence increasing the effective resistance between drain and source. This proportional increase in the effective resistance cannot be neglected for relatively large drain voltages.

As the curve flattens, as the parabola reaches its maximum, i.e., $V_{DS} = (V_{GS} - V_{th})$, the MOSFET enters anoter mode of operation, called the **saturation**. Here, the drain voltage increased such that the channel at the drain end has 0 thickness, called *channel pinch-off*. It is assumed that beyond this point, V_{DS} has no effect on the drain current, (channel cannot have a negative thickness, right?). Thus the drain current remains constant for V_{DS} above this value, or $V_{DS_{(sat)}}$.
The expression for drain current in this region is as follows.

$$I_D = \frac{1}{2}\kappa \left(V_{GS} - V_{th}\right)^2 \tag{4}$$

Here, the drain current is no longer a function of V_{DS}, hence will appear as constant against V_{DS}, and is a quadratic function of V_{GS}. In other words, the MOSFET behaves like an ideal current source, albeit, a non-linear one.

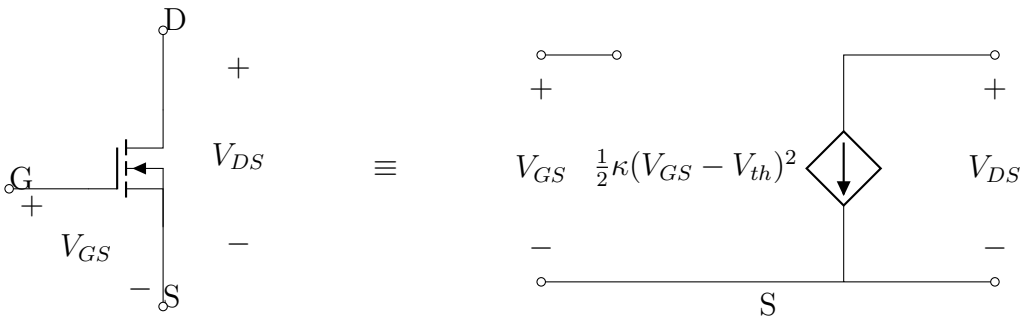
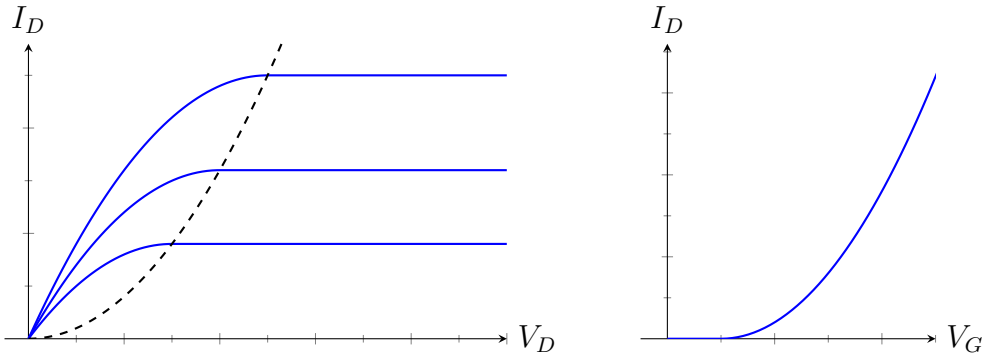


Figure 4: Equivalent ideal circuit for an NMOS operating at saturation region. $V_{DS} < (V_{GS} - V_{th})$



(a) $I_D - V_{DS}$ graph, linear-saturation regions.

(b) $I_D - V_{GS}$ graph, **on saturation region**.

Figure 5: Ideal $I_D - V_{DS}$ and $I_D - V_{GS}$ Characteristics

Combining these three cases, three regions of operation, a full expression for the drain current is as follows.

$$I_D = \begin{cases} 0, & V_{GS} < V_{th} \\ \kappa\left(V_{GS} - V_{th} - \frac{1}{2}V_{DS}\right)V_{DS}, & V_D \leq (V_{GS} - V_{th}) \\ \frac{1}{2}\kappa(V_{GS} - V_{th})^2, & V_{DS} > (V_{GS} - V_{th}) \end{cases} \qquad \kappa \triangleq \left(\mu_n C_{ox}\frac{W}{L}\right) \tag{5}$$

Of course, those perfectly constant drain currents looks a bit too good to be true. It was said that increasing the V_{DS} beyond $V_{DS_{(sat)}}$ would not have any effect. It, however, does. Increasing the V_{DS} beyond that causes the *pinched-off* point of the channel to seperate and move away from the drain, while it still maintains the conduction, it reduces the output resistance of the MOSFET from infinite to a finite value. To encompansate this effect, the equation can be modified as below, where λ is a device parameter in V^{-1}.

$$I_D = \begin{cases} 0, & V_{GS} < V_{th} \\ \kappa(1+\lambda V_{DS})\left(V_{GS} - V_{th} - \frac{1}{2}V_{DS}\right)V_{DS}, & V_D \leq (V_{GS} - V_{th}) \\ \frac{1}{2}\kappa(1+\lambda V_{DS})(V_{GS} - V_{th})^2, & V_{DS} > (V_{GS} - V_{th}) \end{cases} \tag{6}$$

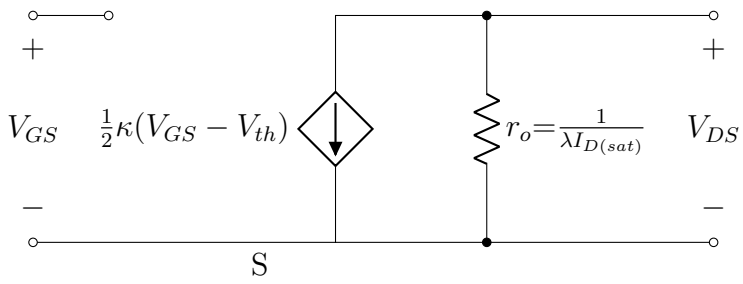
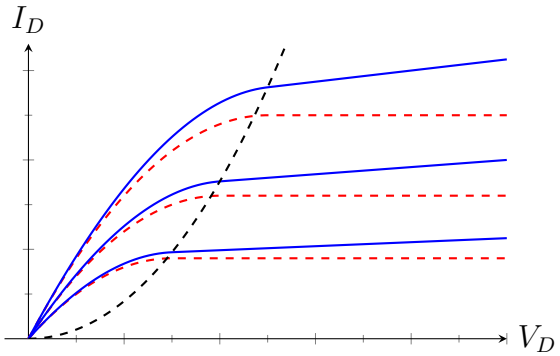
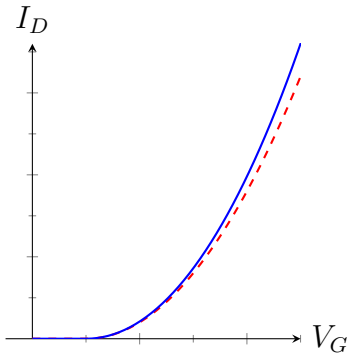


Figure 6: Equivalent ideal circuit for an NMOS operating at saturation region. $V_{DS} < (V_{GS} - V_{th})$
With finite output resistance.



(a) $I_D - V_{DS}$ graph, linear-saturation regions.



(b) $I_D - V_{GS}$ graph, **on saturation region**.

Figure 7: $I_D - V_{DS}$ and $I_D - V_{GS}$ Characteristics with finite output resistance. Ideal plots shown in dashed red.

Lastly, recall that the gate was insulated from the body with an insulating layer, two conducting surfaces seperated by an insulator, a capacitor! Of course, given the average size of these devices (structurally), this capacitance will be quite small, but it's still going to be effecting the operation of the MOSFET at high frequencies or fast switching operations. Since we have connected the body and source together, this capacitance appears between the gate and the source. What follows, of course, is another, smaller capacitance between the gate and the drain, but its effects are not as obvious as the gate-source capacitance. The equivalent circuit model can be improved by adding a capacitor into the input port.

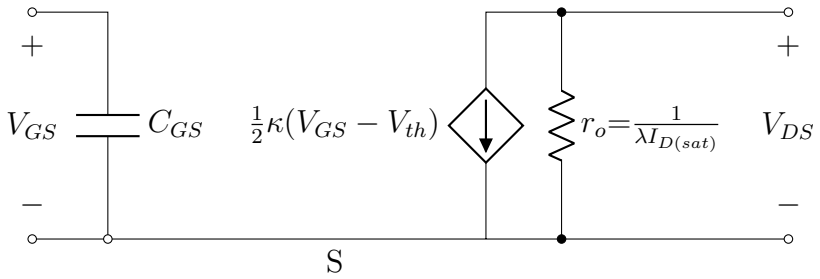


Figure 8: Equivalent circuit for an NMOS operating at saturation region $V_{DS} < (V_{GS} - V_{th})$.
With finite output resistance and gate-source capacitance.

2 Application and Results

2.1 V_{GS}–I_D Characteristics of N-Channel MOSFET

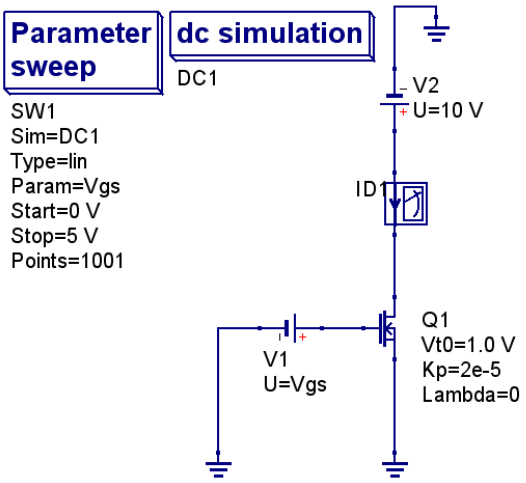


Figure 9: Experiment circuit for gate characteristic

To observe $V_{GS} - I_D$ characteristic of a n-channel MOSFET, the circuit as depicted above is constructed in QUCS. Under constant drain to source voltage $V_{DS} = 10\,\text{V}$, gate to source voltage V_{GS} is swept from $0\,\text{V}$ to $5\,\text{V}$. During which the drain current I_D is measured. The following graph is created by plotting I_D against V_{GS}.

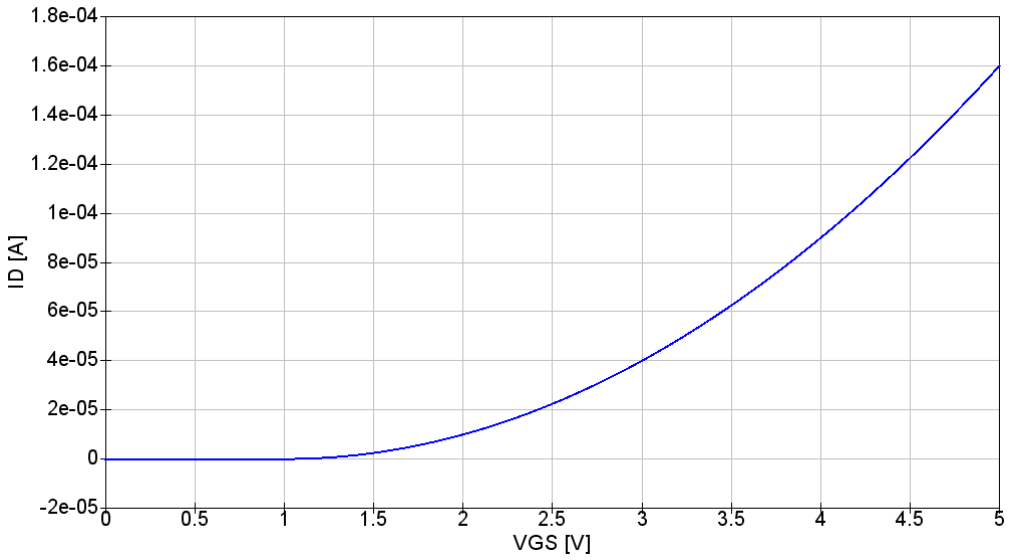


Figure 10: $V_{GS} - I_D$ characteristic graph

Notice that the simulation settings ensure that $V_D \geq V_{GS} - V_t$, so that the transistor remains saturated during the entire sweep. Since the expression for the drain current in this mode of operation is

$$I_D = \begin{cases} 0 & V_{GS} < V_{th} \\ \frac{1}{2}\kappa(V_{GS} - V_{th})^2 & V_{GS} \geq V_{th} \end{cases} \qquad \kappa \triangleq \mu_n C_{ox} \frac{W}{L_{eff}}$$

the graph is expected to be half of a parabola. Which is the case. It also can be seen from the graph that the drain current remains effectively 0 until the gate voltage surpasses the threshold voltage, in this case, 1 V.

V_{GS} [V]	Calculated [µA]	Simulation [µA]
1	0	3.97e-12
2	10	10
3	40	40
3	90	90
5	160	160

Table 1: Comparison of calculated values and simulation results

Simulation results agreed with calculations to 7 significant digits.

2.2 V_{DS}–I_D Characteristics of N-Channel MOSFET

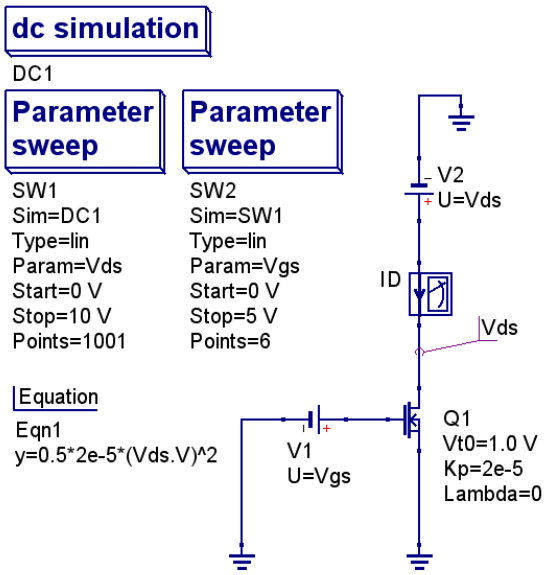


Figure 11: Circuit

To observe the $V_{DS} - I_D$ characteristics, experiment setup is changed by adding another parameter sweep for sweeping the drain voltage. Gate voltage sweep discretised and varied between 0 and 5 V with 1 V increments. I_D current is measured.

Family of drain current curves are plotted against V_{DS} and each one labelled.[3] The parabola $i = \frac{1}{2}\kappa(V_{DS})^2$ is also plotted with dashed black curve.

Simulation results again agree with theoratical calculations to 7 significant digits.

[3]Apart from V_{GS}={0,1} V since the plot doesn't allow to mark them seperately.

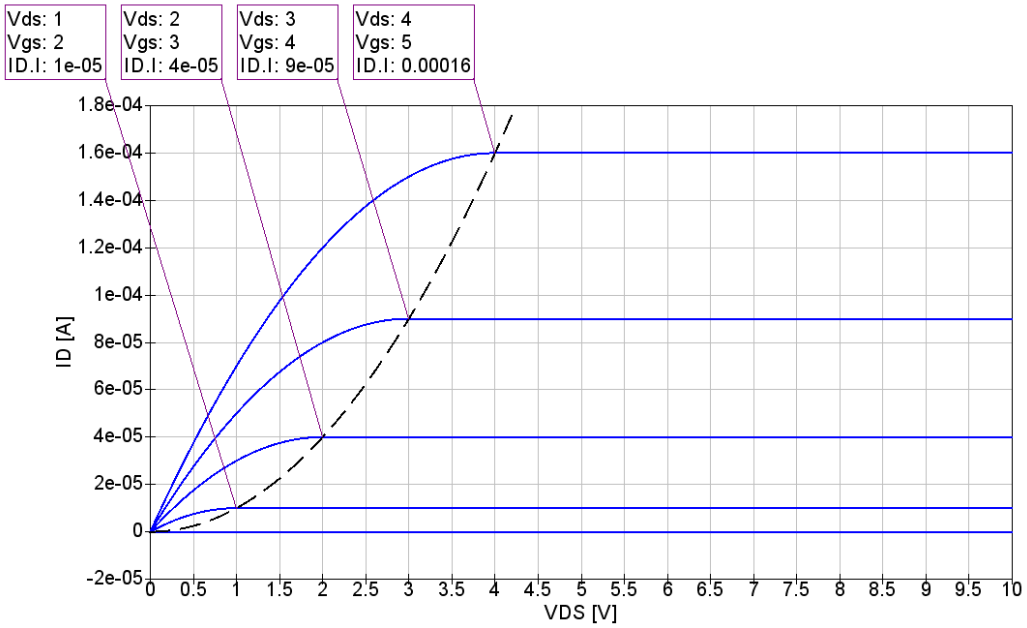


Figure 12: graph

As expected, for any gate voltage that doesn't put the transistor in cut-off, as V_{DS} increases, drain current starts more or less linear, eventually bending to form a downward looking parabola, and finally at the point $V_{DS} = (V_{GS} - V_{th})$, transistor saturates and I_D remains constant, independent of the V_{DS}. Increase in V_{GS} increases both the V_{DS} that saturates the transistor, and the I_D that flows when it saturates.

For $V_{GS} = 0\,\text{V}$ and $V_{GS} = 1\,\text{V}$, the drain current remains 0. Transistor is in cut-off region, since the electric field at the gate is lacking or not sufficient enough to form an inversion layer on the channel region. Since the structure of the MOSFET is so that there are two P-N junctions between drain and source with opposite directions, if a channel is not formed, there is a reverse biased P-N junction between drain and source for either polarity of the V_{DS}, hence no current can flow between drain and source.

2.3 Effect of Series Gate Resistor

In this part, a 1 kΩ resistor is introduced in series with the gate, to observe its effect on the $V_{DS} - I_D$ plot of the previous stage. Since gate of a MOSFET *draws no current*, this resistor appears completely irrelevant. And indeed, $V_{DS} - I_D$ plot in this setting is completely identical to that of previous stage. To avoid duplicating the entire stage, this barely modified schematic and the identical plot are not given seperately.

This gate resistor, however, starts doing interesting things, if looked correcty. By correctly, we mean, in time domain. Here, the circuit is carried into a transient simulation, with a relatively high frequency square wave of magnitude 5 V applied to the gate, with the 1 kΩ series resistor. However, since default parameters for the MOSFETs in QUCS apparently choosen so that the transistor is quite close to ideal[4], MOSFET is replaced by a real small signal discrete MOSFET, BSS123, that happens to be in QUCS library.

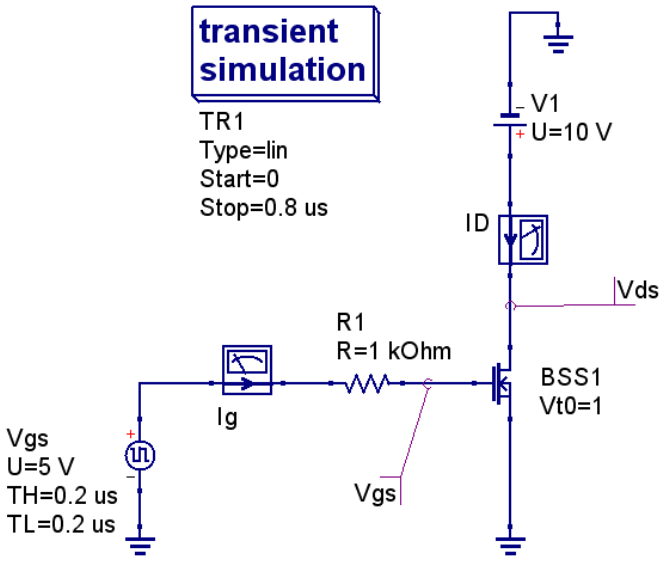


Figure 13: Transient simulation to see effect of series gate resistor.

[4] And there are way too many different capacitance parameters, and I wasn't sure what a realistic value would be anyway.

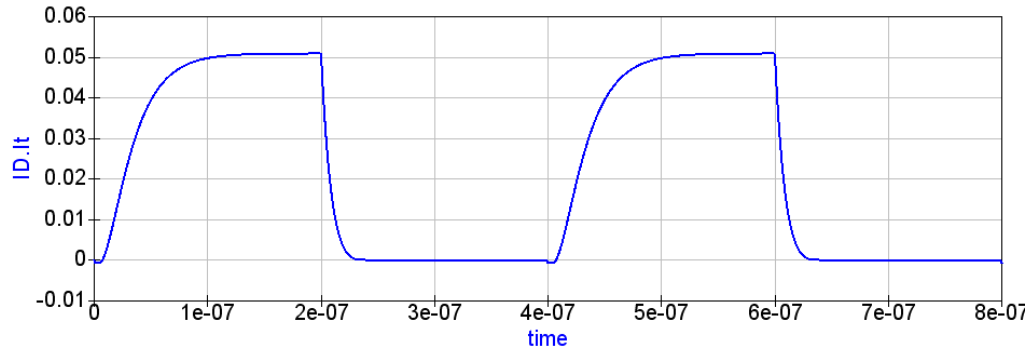


Figure 14

As a result, the drain current starts to behave awkwardly. Values, of course are different since the transistor is different, but what matters is the shape of the waveform, it looks *almost like capacitor charge-discharge pattern*. Indeed, if the voltage and the current at the gate were to be measured, we see the following graph.

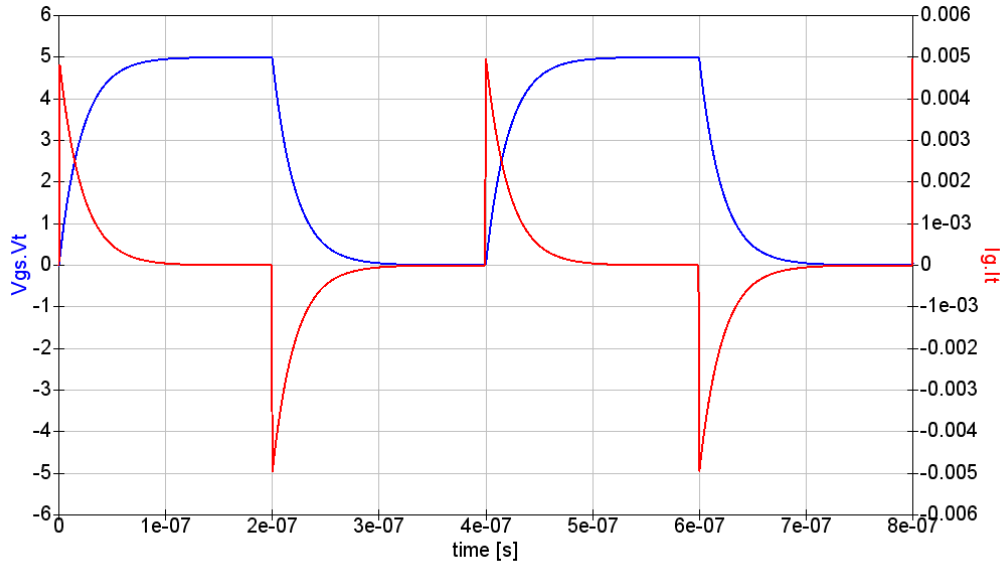


Figure 15

The capacitive response of the gate can clearly be seen from this graph. Of course gate behaves capacitor-like, since the gate plate and the bulk effectively forms a capacitor. Since the gate pretty much fully charges at about 100 ns, assuming this is roughly equal to 5τ, the approximate capacitance of the gate can be calculated.

$$\begin{aligned} 5\tau &\approx 100 \times 10^{-}9\mathtt{s} \\ \tau = RC &\approx 20\,\mathrm{ns}, \quad R = 1\,\mathrm{k}\Omega \\ \implies C &\approx 20\,\mathrm{pF} \end{aligned}$$

Therefore, the gate capacitance of this MOSFET should be around at the order of 20 pF's Another interesting observation is that during the transitions of the applied gate voltage, the gate momentarily draws around 5 mA of current![5] That's quite a lot of current to be drawn by something supposed to draw no current.

[5] At least this for this transistor.

2.4 Effect of Negative V_{GS}

What follows that is the case when a negative V_{GS} is applied to the gate. Then, the electric field between the gate plate and the body not only isn't sufficient to pull electrons into the channel region and create a channel, but it pushes the electrons away, not allowing any current to flow between drain and source. While it is not necessary for enhancement type NMOS' to apply a negative gate voltage, it can help discharging the gate more quickly and hence allow the transistor to fall into cut-off mode more abruptly.

Following is another test setup, where the same circuit as before is not first driven with 5 V positive pulse, and then with ±5 V symmetric pulse.

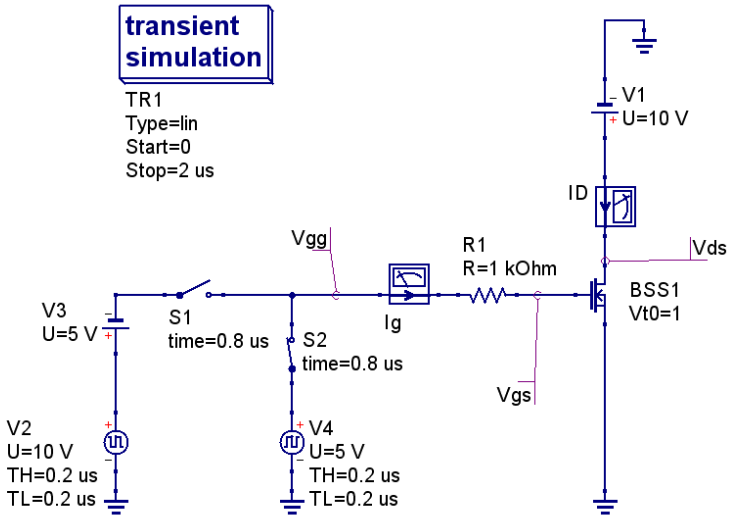


Figure 16

As expected, applying a negative voltage to a charged gate increased the speed of its discharge, thus decreasing the fall time of the drain current. However, now it takes proportionally longer to charge the gate above the threshold, thus delaying the rise of the drain current.

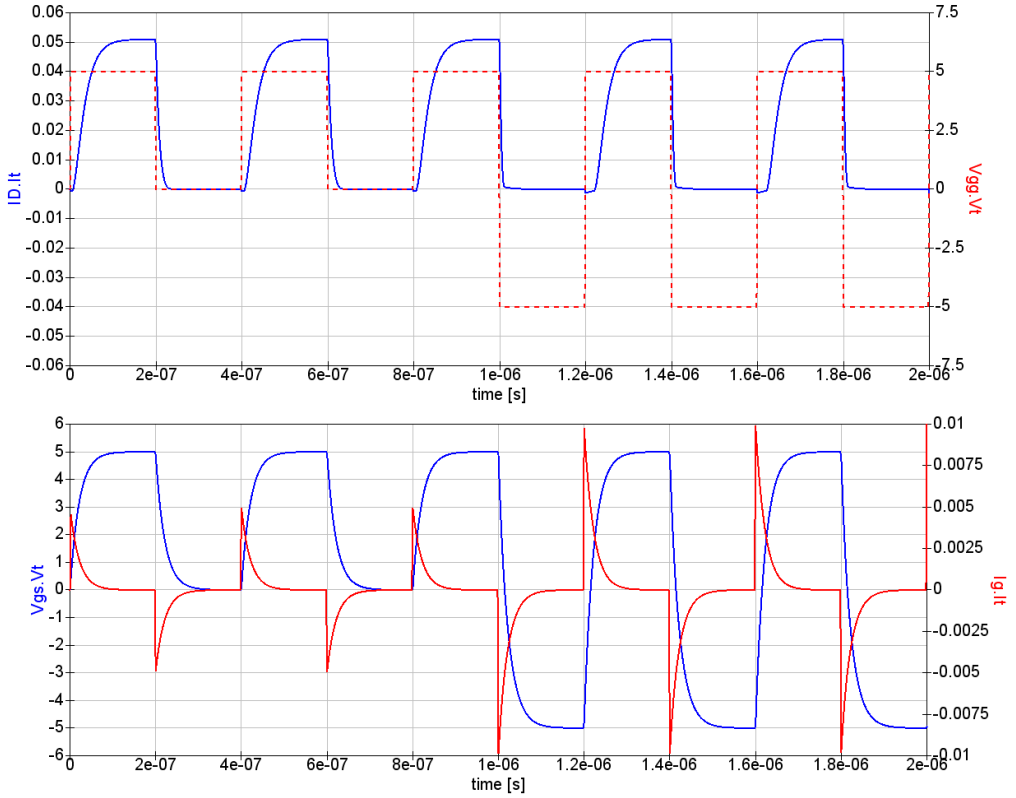


Figure 17:
Top: Drain current (left), applied gate voltage (right)
Bottom: Gate current (left), gate voltage (right)

3 Conclusion

In this experiment, characteristics of n-channel MOSFET are investigated.

In first stage, the the relation between gate voltage and the drain current is observed. It is seen that so long as the transistor remains in the saturation region, the drain current is a quadratic function of the gate voltage, where it remains at 0 until the gate voltage exceeds a certain level. That is, the zero bias threshold voltage, below which the electric field created by the gate voltage is not enough to form the inversion layer. As V_{GS} increases beyond this threshold, drain current starts to rise, following a parabola. Drain voltage has no effect in this operation, so long as it is kept higher that the $V_{GS} + V_{th}$, otherwise transistor falls out of the saturation and enters the triode region, where the drain current now is a linear function of the V_{GS}.

In the second stage, relation between drain voltage and the drain current is observed under various levels of gate voltage. It is seen that, for any gate voltage that doesn't put the MOSFET into cut-off, I_D rises almost linearly for relatively small V_{DS}. At this region, MOSFET behaves like a voltage controlled resistor whose value is inversly proportional to the gate voltage. This relation however, for increasing V_{DS}, starts to lose its linearity. As the V_{DS} exceeds $V_{GS} - V_{th}$, transistor enters the saturation region, where the drain current remains constant, independent of the V_{DS}. Clearly, both the drain voltage that puts the transistor into saturation $V_{DS_{(sat)}}$ and the drain current at the saturation $I_{D_{(sat)}}$ increases with increasing V_{GS}.

Lastly, a resistor in series with the gate is added into the circuit. It is seen that this resistor had no effect whatsoever on the results of the simulation. However, since the gate behaves like a small capacitor, when underwent transient simulation, it is seen that this resistor increases the the time it takes gate to fully reach its maximum, hence delaying the peak of the drain current. Approximate calculations estimated the value of the gate capacitance to be at the order of picofarads, hence quite small. However, at high frequencies, this capacitive behaviour can be very significant. Of course, the MOSFET used for this part was a discrete MOSFET, and the MOSFETs in integrated circuits may have drastically different values.

Effect of applying negative V_{GS} is also studied at this part, while it appears to be no different than applying any below-threshold voltage in DC analysis, it is seen that it can have a significant effect in trainsient analysis. Capacitive nature of the gate results in diminishing of fast edges, which consequently would deform any signal with high frequency components.