1 Application and Results

1.1 V_{GS}–I_D Characteristics of N-Channel MOSFET

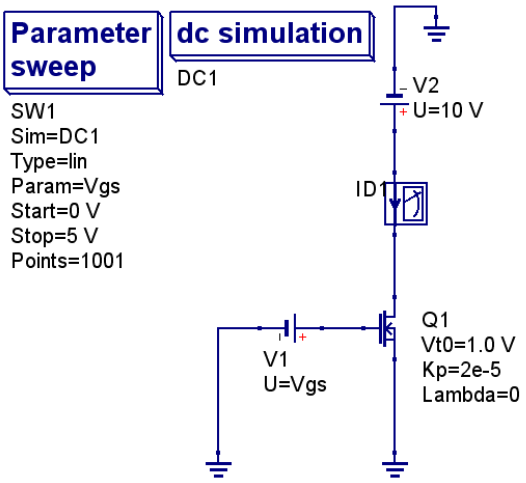

Figure 1: Experiment circuit for gate characteristic

To observe $V_{GS} - I_D$ characteristic of a n-channel MOSFET, the circuit as depicted above is constructed in QUCS. Under constant drain to source voltage $V_{DS} = 10\,\mathrm{V}$, gate to source voltage V_{GS} is swept from $0\,\mathrm{V}$ to $5\,\mathrm{V}$. During which the drain current I_D is measured. The following graph is created by plotting I_D against V_{GS}.

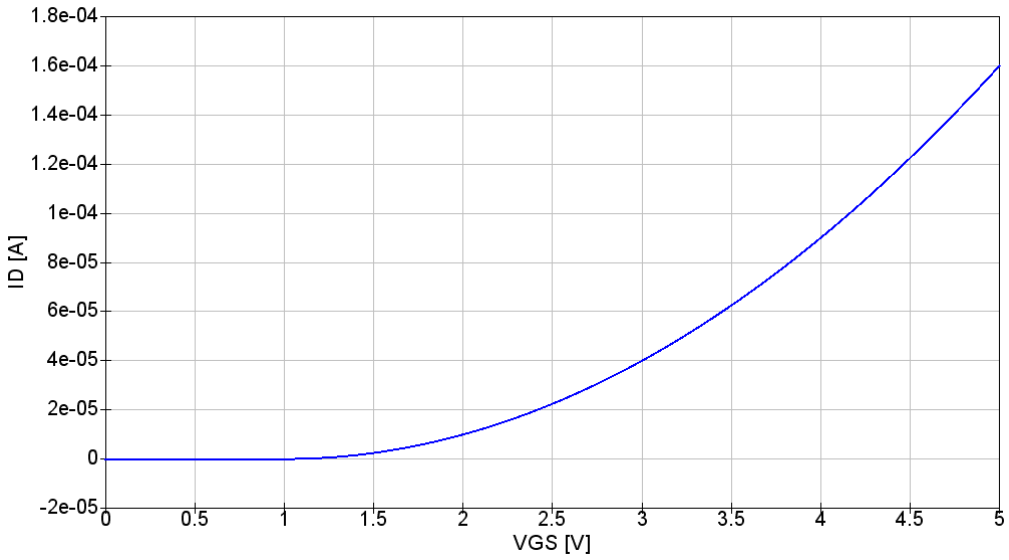

Figure 2: $V_{GS} - I_D$ characteristic graph

Notice that the simulation settings ensure that $V_D \geq V_{GS} - V_t$, so that the transistor remains saturated during the entire sweep. Since the expression for the drain current in this mode of operation is

$$I_D = \begin{cases} 0 & V_{GS} < V_{th} \\ \frac{1}{2}\kappa(V_{GS} - V_{th})^2 & V_{GS} \geq V_{th} \end{cases} \qquad \kappa \triangleq \mu_n C_{ox} \frac{W}{L_{eff}}$$

the graph is expected to be half of a parabola. Which is the case. It also can be seen from the graph that the drain current remains effectively 0 until the gate voltage surpasses the threshold voltage, in this case, 1 V.

V_{GS} [V]	Calculated [µA]	Simulation [µA]
1	0	3.97e-12
2	10	10
3	40	40
3	90	90
5	160	160

Table 1: Comparison of calculated values and simulation results

Simulation results agreed with calculations to 7 significant digits.

1.2 V_{DS}–I_D Characteristics of N-Channel MOSFET

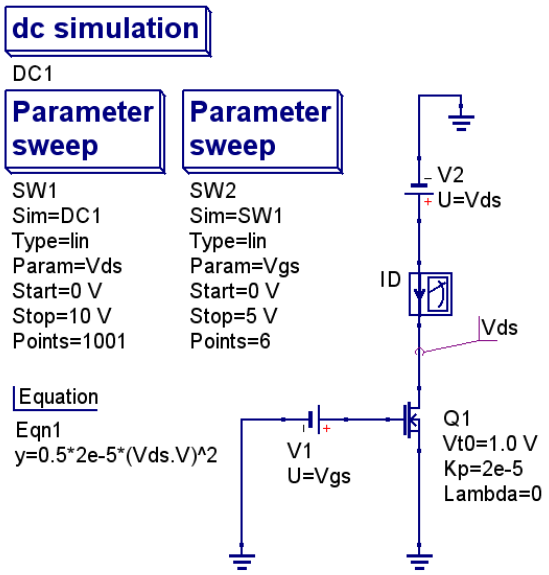

Figure 3: Circuit

To observe the $V_{DS} - I_D$ characteristics, experiment setup is changed by adding another parameter sweep for sweeping the drain voltage. Gate voltage sweep discretised and varied between 0 and 5 V with 1 V increments. I_D current is measured.

Family of drain current curves are plotted against V_{DS} and each one labelled.[1] The parabola $i = \frac{1}{2}\kappa(V_{DS})^2$ is also plotted with dashed black curve.

Simulation results again agree with theoratical calculations to 7 significant digits.

[1] Apart from V_{GS}={0,1} V since the plot doesn't allow to mark them seperately.

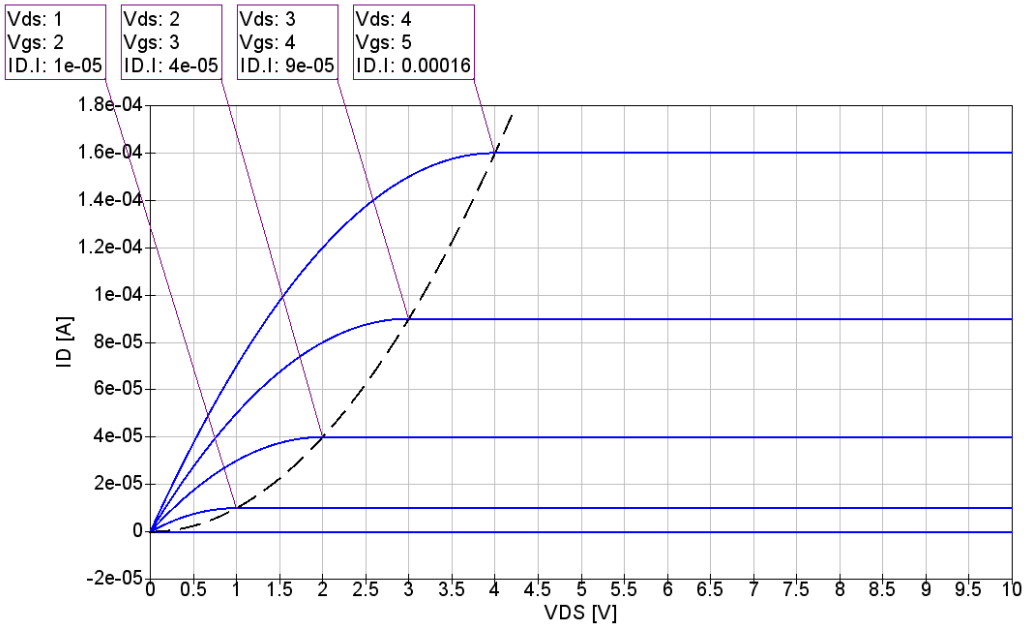

Figure 4: graph

As expected, for any gate voltage that doesn't put the transistor in cut-off, as V_{DS} increases, drain current starts more or less linear, eventually bending to form a downward looking parabola, and finally at the point $V_{DS} = (V_{GS} - V_{th})$, transistor saturates and I_D remains constant, independent of the V_{DS}. Increase in V_{GS} increases both the V_{DS} that saturates the transistor, and the I_D that flows when it saturates.

For $V_{GS} = 0\,\mathrm{V}$ and $V_{GS} = 1\,\mathrm{V}$, the drain current remains 0. Transistor is in cut-off region, since the electric field at the gate is lacking or not sufficient enough to form an inversion layer on the channel region. Since the structure of the MOSFET is so that there are two P-N junctions between drain and source with opposite directions, if a channel is not formed, there is a reverse biased P-N junction between drain and source for either polarity of the V_{DS}, hence no current can flow between drain and source.

1.3 Effect of Series Gate Resistor

In this part, a 1 kΩ resistor is introduced in series with the gate, to observe its effect on the $V_{DS} - I_D$ plot of the previous stage. Since gate of a MOSFET *draws no current*, this resistor appears completely irrelevant. And indeed, $V_{DS} - I_D$ plot in this setting is completely identical to that of previous stage. To avoid duplicating the entire stage, this barely modified schematic and the identical plot are not given seperately.

This gate resistor, however, starts doing interesting things, if looked correcty. By correctly, we mean, in time domain. Here, the circuit is carried into a transient simulation, with a relatively high frequency square wave of magnitude 5 V applied to the gate, with the 1 kΩ series resistor. However, since default parameters for the MOSFETs in QUCS apparently choosen so that the transistor is quite close to ideal[2], MOSFET is replaced by a real small signal discrete MOSFET, BSS123, that happens to be in QUCS library.

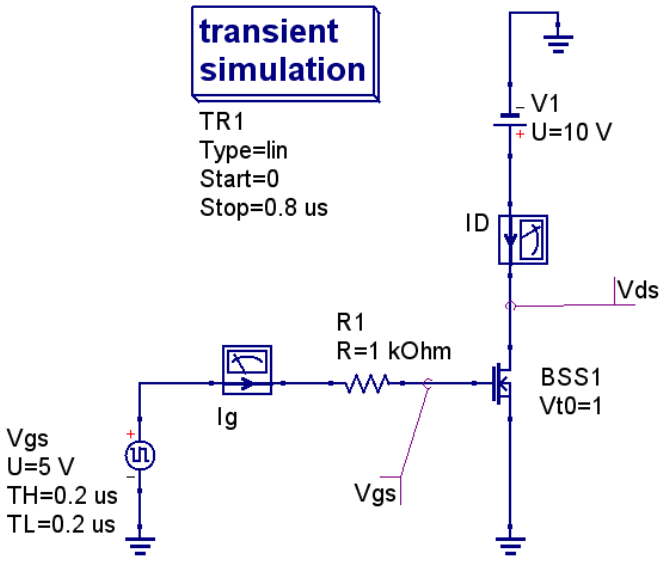

Figure 5: Transient simulation to see effect of series gate resistor.

[2]And there are way too many different capacitance parameters, and I wasn't sure what a realistic value would be anyway.

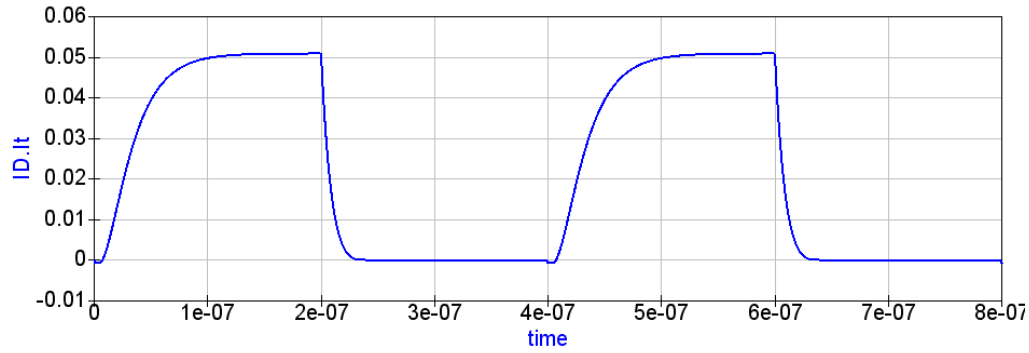

Figure 6

As a result, the drain current starts to behave awkwardly. Values, of course are different since the transistor is different, but what matters is the shape of the waveform, it looks *almost like capacitor charge-discharge pattern*. Indeed, if the voltage and the current at the gate were to be measured, we see the following graph.

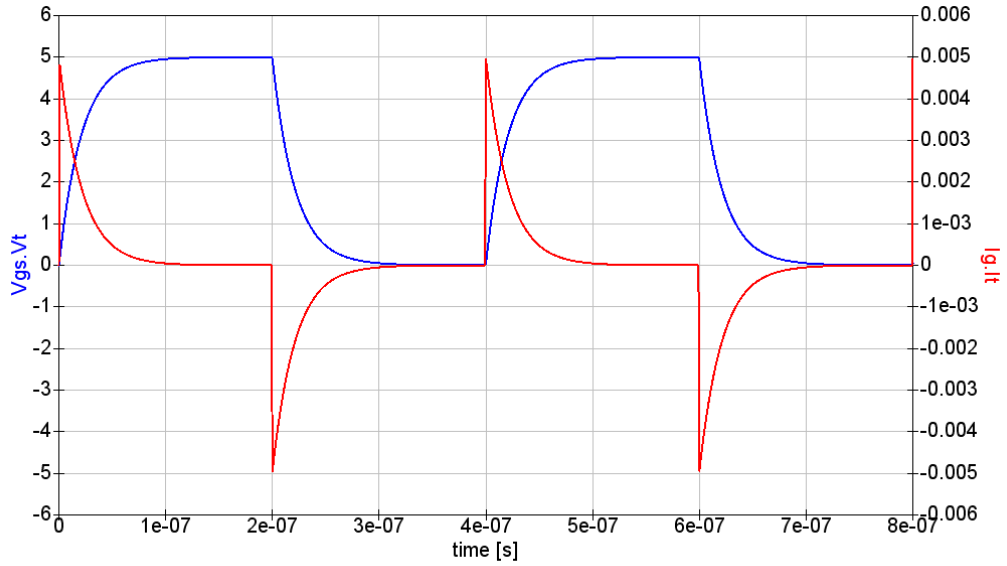

Figure 7

The capacitive response of the gate can clearly be seen from this graph. Of course gate behaves capacitor-like, since the gate plate and the bulk effectively forms a capacitor. Since the gate pretty much fully charges at about 100 ns, assuming this is roughly equal to 5τ, the approximate capacitance of the gate can be calculated.

$$\begin{aligned} 5\tau &\approx 100 \times 10^{-}9\mathtt{s} \\ \tau = RC &\approx 20\,\mathrm{ns}, \quad R = 1\,\mathrm{k}\Omega \\ \implies C &\approx 20\,\mathrm{pF} \end{aligned}$$

Therefore, the gate capacitance of this MOSFET should be around at the order of 20 pF's Another interesting observation is that during the transitions of the applied gate voltage, the gate momentarily draws around 5 mA of current![3] That's quite a lot of current to be drawn by something supposed to draw no current.

[3] At least this for this transistor.

1.4 Effect of Negative V_{GS}

What follows that is the case when a negative V_{GS} is applied to the gate. Then, the electric field between the gate plate and the body not only isn't sufficient to pull electrons into the channel region and create a channel, but it pushes the electrons away, not allowing any current to flow between drain and source. While it is not necessary for enhancement type NMOS' to apply a negative gate voltage, it can help discharging the gate more quickly and hence allow the transistor to fall into cut-off mode more abruptly.

Following is another test setup, where the same circuit as before is not first driven with 5 V positive pulse, and then with ±5 V symmetric pulse.

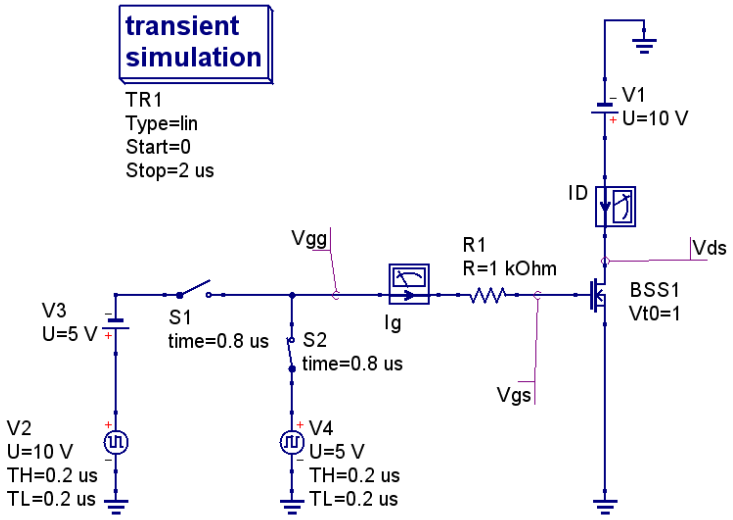

Figure 8

As expected, applying a negative voltage to a charged gate increased the speed of its discharge, thus decreasing the fall time of the drain current. However, now it takes proportionally longer to charge the gate above the threshold, thus delaying the rise of the drain current.

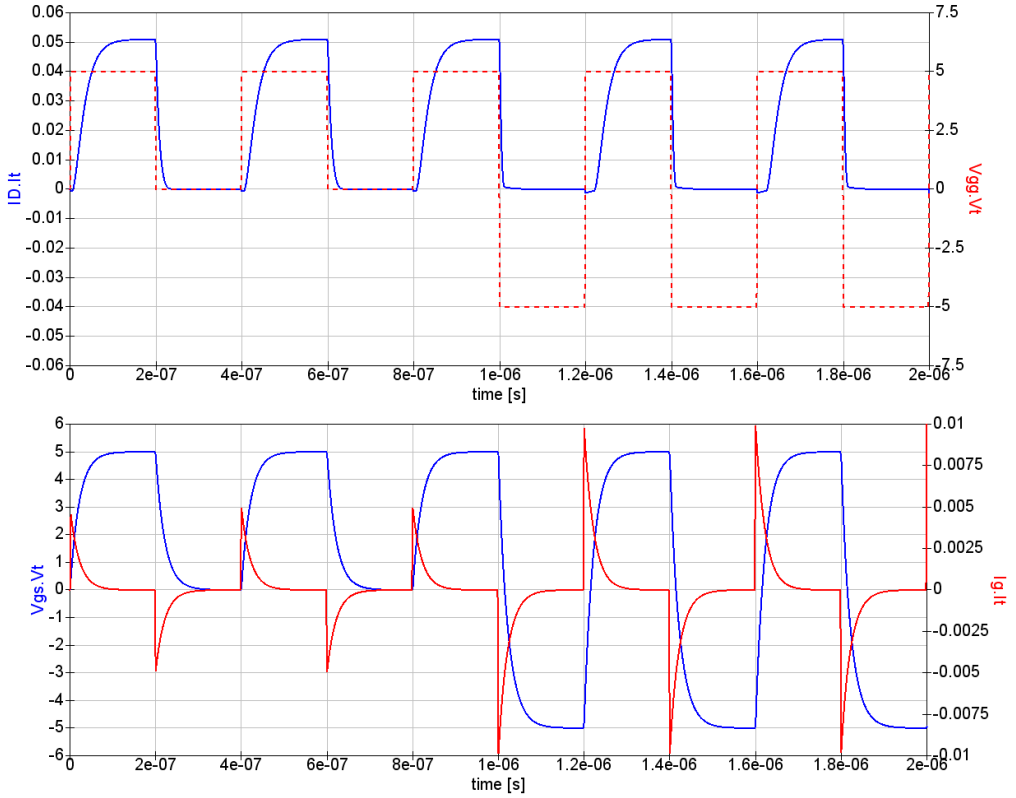

Figure 9:
Top: Drain current (left), applied gate voltage (right)
Bottom: Gate current (left), gate voltage (right)