Abenezer Wudenhe

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EDUCATION

University of California, Riverside (UCR) — PhD (Computer Science)
- SMART Fellow
- Chancellor's Distinguished Fellow
- GAANN Fellow

September 2024

University of Maryland, Baltimore County (UMBC) — BS (Computer Engineering)
- Meyerhoff Scholar
- NSA Scholar

May 2018 (Cum Laude)

PROFESSIONAL EXPERIENCE

Extreme Storage and Computer Architecture Lab (ESCAL) — **Aug 2018 – Sep 2024**

Graduate research assistant to Dr. Hung-Wei Tseng.

Accel-Bench: A Benchmark Suite toward the Future of Accelerator-Intensive Programming
- Designed and developed a benchmark suite optimization for accelerators.
- Integrate over 10 applications in fields including genomics, web mining, image processing.
- Integrate GPU simulator, Accel-Sim, for evaluation of micro architecture.

Optimizing memory hierarchy for mixed precision computing
- Developed an GPGPU-sim extension to enable more accurate simulation of NVIDIA's half-precision computation and evaluation of the overhead.
- Accelerate the performance of GPU kernels with reasonable accuracy using CUDA.

TPUPoint: Profiler and optimizer for TPU cloud
- Designed and developed an automatic profiling and optimization tool for Google's TPU-based.
- Achieved up to 1.12x speedup for programmer's optimizations using TensorFlow.

Google Software Engineering Intern — **June 2023 – Sep 2023**

SWE Intern under Dr. Jaswanth Sreeram (XLA Compiler Team)
- Developed Low Level Instruction analysis tool to identify performance gaps in compiler heuristics.
- Create visual analysis tool of compiler generated TPU & CPU instruction execution and Utilization.

Google Software Engineering Intern — **June 2022 – Sep 2022**

SWE Intern under Dr. Ayub Gubran (Pixel gChip Team)
- Developed System Verilog based tools for architects to utilize in debugging/analysis of SoCs files.
- Participated in Google Intern Mentorship Program during weeks 5 - 12.

Intel OneAPI Graduate Student Software Internship — **Oct 2021 – Feb 2022**

SWE Research Intern
- Extend compiler infrastructure to produce Data Parallel C++ device code for CPU, GPU, and FPGA.
- Present Temporal to Spatial Programming (T2SP) at the 10th IWOCL Conference.

PUBLICATION

A. Wudenhe, Hung-Wei Tseng. "TPUPoint: Automatically Characterizing Hardware Accelerated Data Center Machine Learning Program Behavior". In IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS 2021), 2021.

TECHNICAL SKILLS

- Experience programming in **C, C++, python**, **CUDA**, Bazel, Makefile, CMake, html, MPI, php, Arduino, OpenMP, Open MPI, TensorFlow, Skilearn, Javascript, NodeJS
- Experience writing technical documents using LaTex, BibTex, Word
- Experience with Xilinx Design Tool, MATLAB, Cadence's Allegro Design Entry CIS, Atmel Studio