Abenezer Wudenhe

Mawude001@ucr.com | Ahttps://abe157.github.io/ | ☐ (240) 418-4302 (mobile) | Google Scholar

EDUCATION

University of California, Riverside (UCR)	PhD (Computer Science)
---	------------------------

SMART Fellow Expected: May 2024

Chancellor's Distinguished Fellow

GAANN Fellow

University of Maryland, Baltimore County (UMBC) BS (Computer Engineering)

Meyerhoff Scholar May 2018 (Cum Laude)

NSA Scholar

PROFESSIONAL EXPERIENCE

ARMY CYBER DWD Internship

2019 May – Aug 2019

Software Engineering Intern.

Assess new technologies for ARMY Big Data Platform. Determine potential and cost of machine learning application Explore Amazon Kinesis tool for reduction of database overhead.

Extreme Storage and Computer Architecture Lab (ESCAL) 2018 Aug – Present Graduate research assistant to Dr. Hung-Wei Tseng.

Conduct research with a focus on memory acceleration and hardware software co-design. Investigate new accelerator for domain specific application.

University of Michigan Lab 4PROGRESS REU

2017 May - Aug 2017

Undergraduate research assistant to Dr. Chad Jenkins

Applied cluster computing methods to robotic visualization techniques and object recognition. Utilized computer networking and Message Passing Interface (OpenMPI) for applicationsDeveloped GPU accelerated image rendering using Nvidia drivers and CUDA programing.

PUBLICATION

A. Wudenhe, Hung-Wei Tseng. TPUPoint: Automatically Characterizing Hardware Accelerated Data Center Machine Learning Program Behavior. In IEEE International Symposium on Performance Analysis of Systems and Software, ISPASS 2021, 2021.

A. Wudenhe, F. S. Choa, Q. Meng. Three-dimensional EEG signal tracking for reproducible brain activity monitoring. IEEE Xplore Digital Library 2017. 7846869.

TECHNICAL SKILLS

- Experience programming in C, C++, python, CUDA, html, MPI, php, Arduino, OpenMP, Open MPI, TensorFlow, Skilearn, Javascript, NodeJS
- Experience writing technical documents using LaTex, BibTex, Word
- Experience with Xilinx Design Tool, MATLAB, Cadence's Allegro Design Entry CIS, Atmel Studio