Abenezer Wudenhe

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PROFESSIONAL SUMMARY

Accomplished Computer Science PhD Researcher with 6+ years of specialized experience in accelerator devices, focusing on GPGPUs, TPUs, with exposure to FPGAs. With an undergraduate degree focusing in VLSI and Computer Security. Industry experiences working in large-scale infrastructure, along with a large exposure to algorithms, architecture, programming languages, and operating systems, proven track record of delivering results shown by several publications and scholarships.

EDUCATION

University of California, Riverside (UCR)
Ph.D., Computer Science Sep. 2024
Areas of Expertise: GPU Performance Analysis, Program Language Design

University of Maryland, Baltimore County (UMBC)
B.S., Computer Engineering (Cum Laude) May 2018
Areas of Focus: VLSI and Cyber Security

TECHNICAL SKILLS

Programming: C, C++, CUDA, Python, Verilog, Bazel, Tensorflow, Matplot, NodeJS, Makefile, Clang, OpenMP, NodeJS, JavaScript, SYCL, Intel OneAPI, SQL
Software: Github, Matlab, Cadence's Allegro Design Entry CIS, Atmel Studio, Xilinx Design Tool

SOFTWARE ENGINEERING EXPERIENCE

Extreme Storage and Computer Architecture Lab (ESCAL), UCR May 2018 – Sep. 2024
Graduate Researcher

Accel-Bench: A Benchmark Suite toward the Future of Accelerator-Intensive Programming

- Designed and developed a benchmark suite optimization for accelerators.
- Integrate over 10 applications in fields including genomics, data mining, image processing, and security.
- Integrate GPU simulator, Accel-Sim, for evaluation of micro architecture.

Optimizing memory hierarchy for mixed precision computing

- Developed an GPGPU-sim extension to enable more accurate simulation of NVIDIA's half-precision computation and evaluation of the overhead.
- Developed a set of Rodinia benchmarks to utilize the half-precision support.
- Accelerate the performance of GPU kernels with reasonable accuracy using CUDA, RTL Design.

TPUPoint: Profiler and optimizer for TPU cloud

- Designed and developed an automatic profiling and optimization tool for Google's TPU-based ML Cloud Platform.
- Achieved up to 1.12x speedup for programmer's optimizations using TensorFlow along with power efficiency analysis.
- Adapt subset of MLPerf applications to Google's TPU Cloud Platform.

Google, Sunnyvale, CA
Software Engineering Intern June 2023 – Aug. 2023

- Developed Low Level Instruction analysis tool to identify performance gaps in compiler heuristics.
- Create visual analysis tool of compiler generated TPU & CPU instruction execution and Utilization.

Google, Mountain View, CA
Software Engineering Intern Sep. 2020 – May 2022

- Developed System Verilog based tools for architects to utilize in debugging/analysis of SoCs files.
- Participated in Google Intern Mentorship Program during weeks 5 - 12.

Intel OneAPI Labs, Irvine, CA Oct. 2021 – Feb. 2022
Software Engineering Research Intern

- Extend compiler infrastructure to produce Data Parallel C++ device code for CPU, GPU, and FPGA.
- Construct Clang source-to-source code translation feature on Intel Dev-Cloud platform.
- Present Temporal to Spatial Programming (T2SP) at the 10th IWOCL Conference.

ARMY CYBER COMMAND Internship May 2019 – Aug. 2019
Software Engineering Intern

- Assessed new technologies for ARMY big data platform for distributed computing applications to drive large data insight for threat intelligence analysts.
- Evaluated the potential and deliver cost analysis of ML application on current infrastructure and potential benefits future roadmap objectives.

PROFESSIONAL TRAINNING

Google Computer Science Research Mentorship Program (CSRMP) Sep. 2021 – Dec. 2021

- Collaborate one-on-one with research faculty at Google to structure and explore research topics.
- Identified roadblocks and possible solutions to producing novel computing research at Google.

Facebook (Meta) 2021 Amplified: Above & Beyond Computer Science (ABCS) June 2021 - Aug. 2021

- Actively participated in a three-part virtual workshop hosted by Facebook over the course of six weeks.
- Review technical concepts important to the interviewing process.

PROFESSIONAL MEMBERSHIPS

Member, Institute of Electrical and Electronics Engineers (IEEE) Oct. 2017– Present
Member, Association for Computing Machinery (ACM) Sep. 2019 – Present

PUBLICATIONS (1 of 3) & PRESENTATION (1 of 7)

A. Wudenhe. "Accel-Bench: Exploring the Potential of Programming using Hardware-Accelerated Functions". (In submission)

A. Wudenhe, Hongbo Rong. "Embedding a DSL in SYCL for Productive and Performant Tensor Computing on Heterogeneous Devices". Poster presentation delivered at the 10th International Workshop on OpenCL (IWOCL) and SYCL, Remotely, May 11, 2022.

OTHER SKILLS

Computer: Microsoft Word, PowerPoint, Excel, LaTeX
Languages: English, Amharic