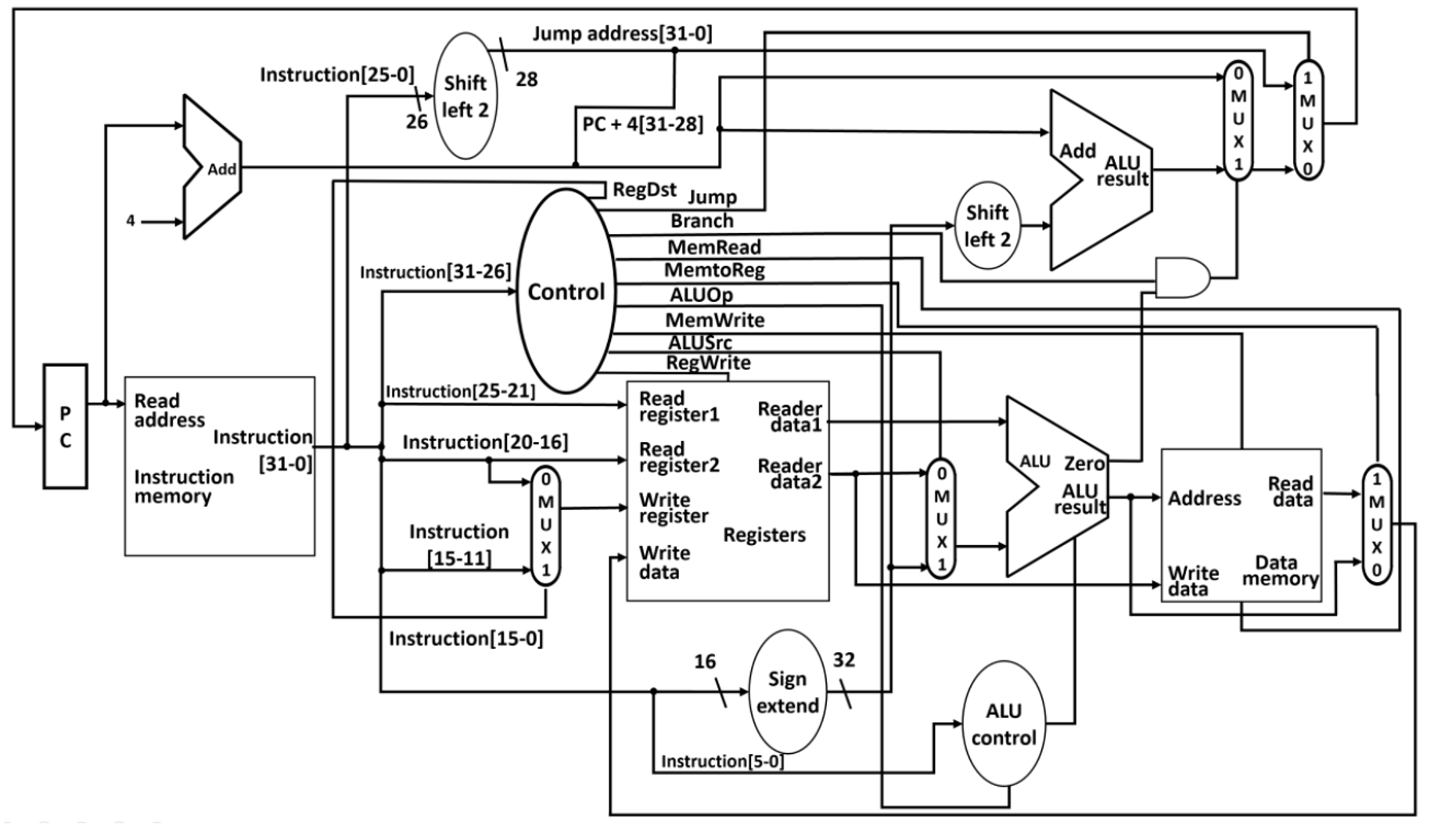
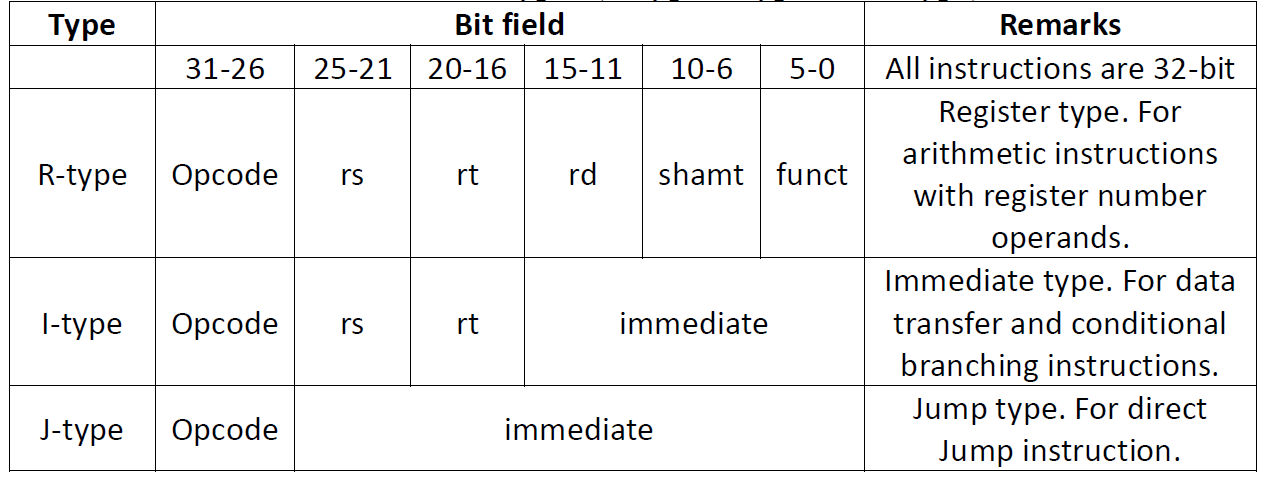
**Exercise: CPU**

1.

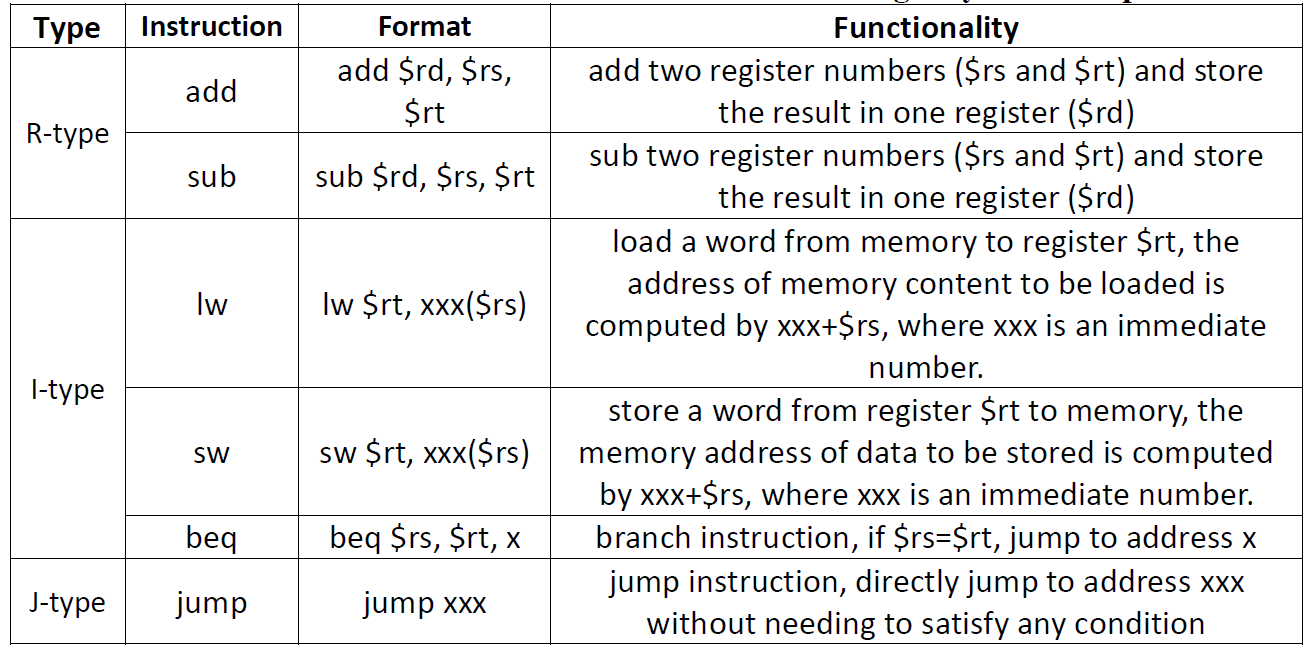
Given a 32-bit single-cycle processor with 32 registers and separated instruction and data memory. The processor structure is shown in the following picture:



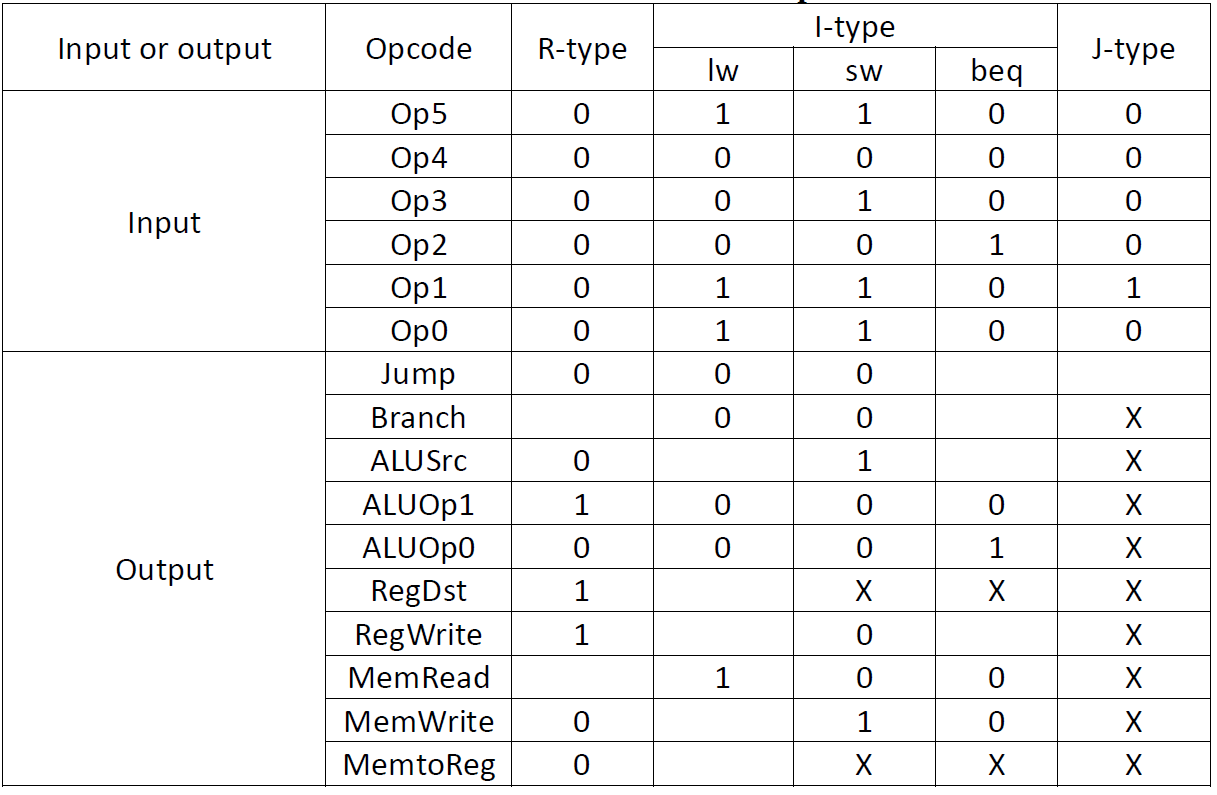
The processor has three types of instructions (R-type, I-type and J-type), the format of which are shown in the following table:



The processor supports the instructions in the following table.



1.Please complete the following table 2 with the corresponding control signals of the different type of instructions. The content with X indicates “don’t care”. Please draw the output part of this table on your answer sheet and fill the blanks (you don’t need to write the output values that are already given to you in the table, but **only** need to answer those are blank).



2. Suppose we will execute the following assembly program on this processor

*sub $3,$4,$5*

*lw $1,20($2)*

*sw $9,20($10)*

*beq $11,$12,20*

*jump 10*

Assume the “shamt” and “funct” fields for instruction “sub” are 00000 and 000001. Please write the machine codes of the above instructions (in hexadecimal numbers).

3. Now, suppose we change the processor to a 5-stage pipeline structure. The 5 stages are:

• IF: instruction fetch

• ID: instruction decode and register file read

• EX: execution or address calculation

• MEM: data memory access

• WB: write data back to register

Moreover, the processor supports ***forwarding*** to directly send the result of the ALU to the register file and directly send the memory data to the register file within one cycle. Now we will execute the MIPS assembly program on this processor:

*lw $5, 10($6)*

*add $7, $8, $9*

*sub $10, $5, $7*

*lw $11, 10($10)*

*sw $11,10($12)*

Please complete the following table showing how the above instructions will proceed through pipeline (draw the table on the answer sheet and fill in your answer).

