



COEN 6501 Project Report

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1 Introduction

The objective of this project is to design an arithmetic logic unit (ALU) that is capable of computing $Z = \frac{A*B}{4} + 1$. The components needed to calculate that output should be designed and chosen properly in order to enhance the efficiency and optimize the design as much as possible. It is important to raise the efficiency by either reducing the area, delay, and the power consumption of the ALU. The component that will affect the performance of the ALU in this case would be the multiplier. Therefore, we will be comparing three multiplier designs to show how our main design is the most efficient in this case. After that, we have expanded the design to 16 bits which was initially 8 bits. We've also implemented pipelining and we've also added an accumulator at the end of the experiment.

2 Design of the ALU

First, a multiplier is needed to compute the product $A*B$. An incrementer is also needed in order to add 1 to the product. Three registers are also required: Register A, Register B, and Register Z. The input operands A and B are latched to registers A and B, respectively, when the load signal transitions from 1 to 0. The final output will also be latched to register Z. The registers are also cleared through a clear signal. Since the operands A and B are unsigned and the output is signed, then, 2 two's complement generators are needed to convert the input operands to signed numbers. A control unit is also needed in order to generate the enable signals for the registers and the end flag that indicates the end of the ALU operation.

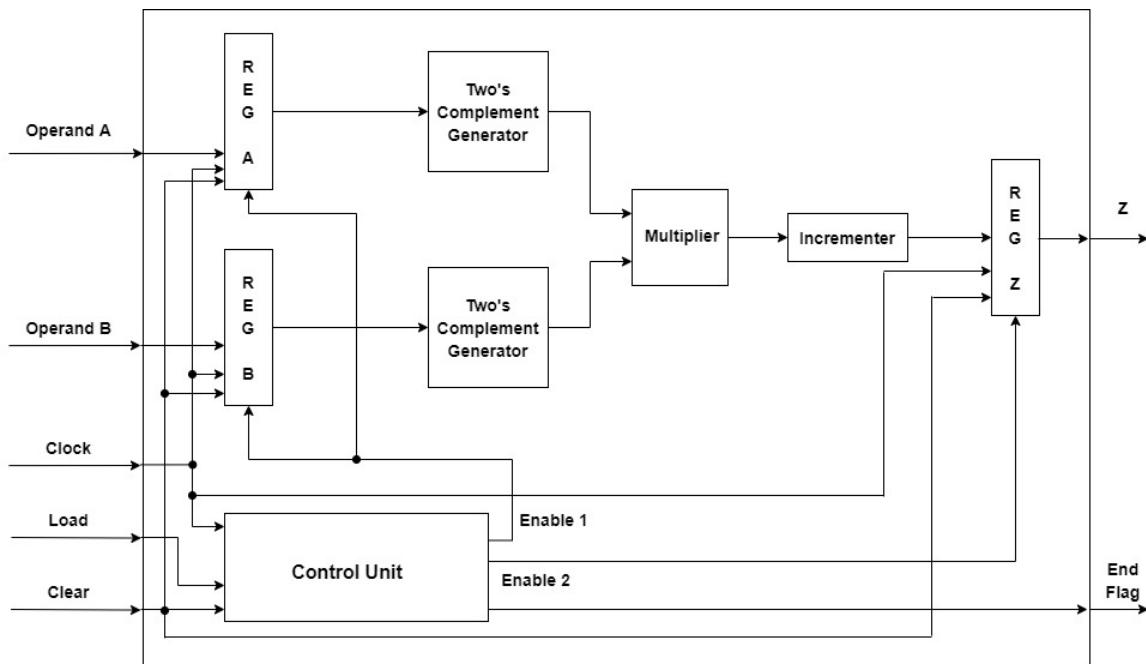


Figure 1 ALU Block Diagram

2.1 Conversion of The Input Operands

Since the input operands are unsigned and the output is signed, then, the operands need to be converted to signed using 2 two's complement generators. The operand bits will all be inverted and then they will be incremented by 1 with the help of an 8-bit incrementer that is made up of eight half-adders that will add the operand bits with the carry bits.

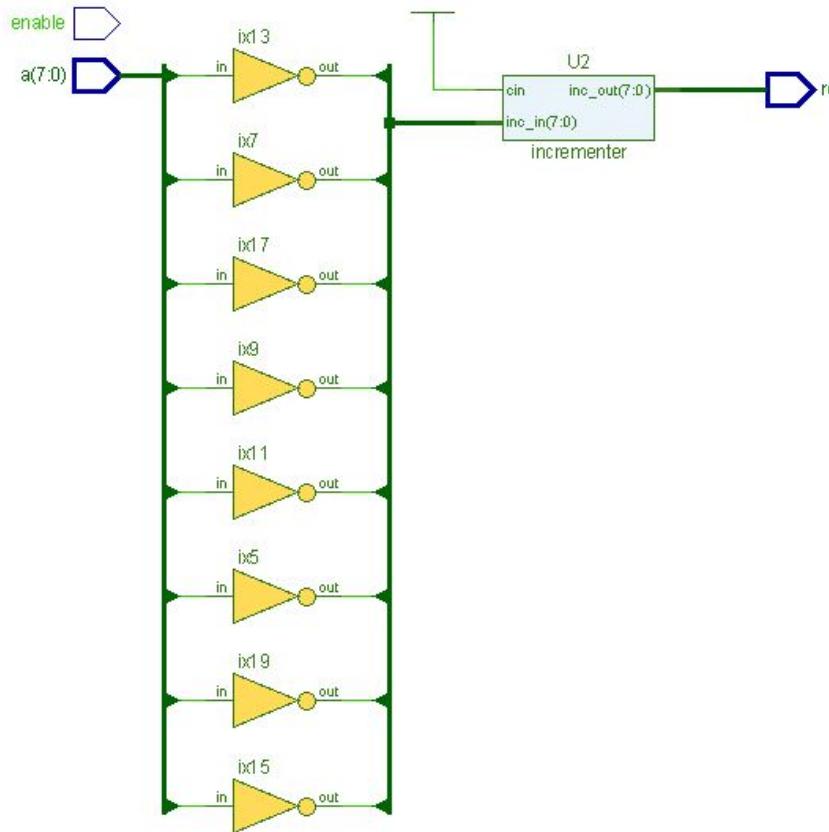


Figure 2 RTL of Two's Complement Generator

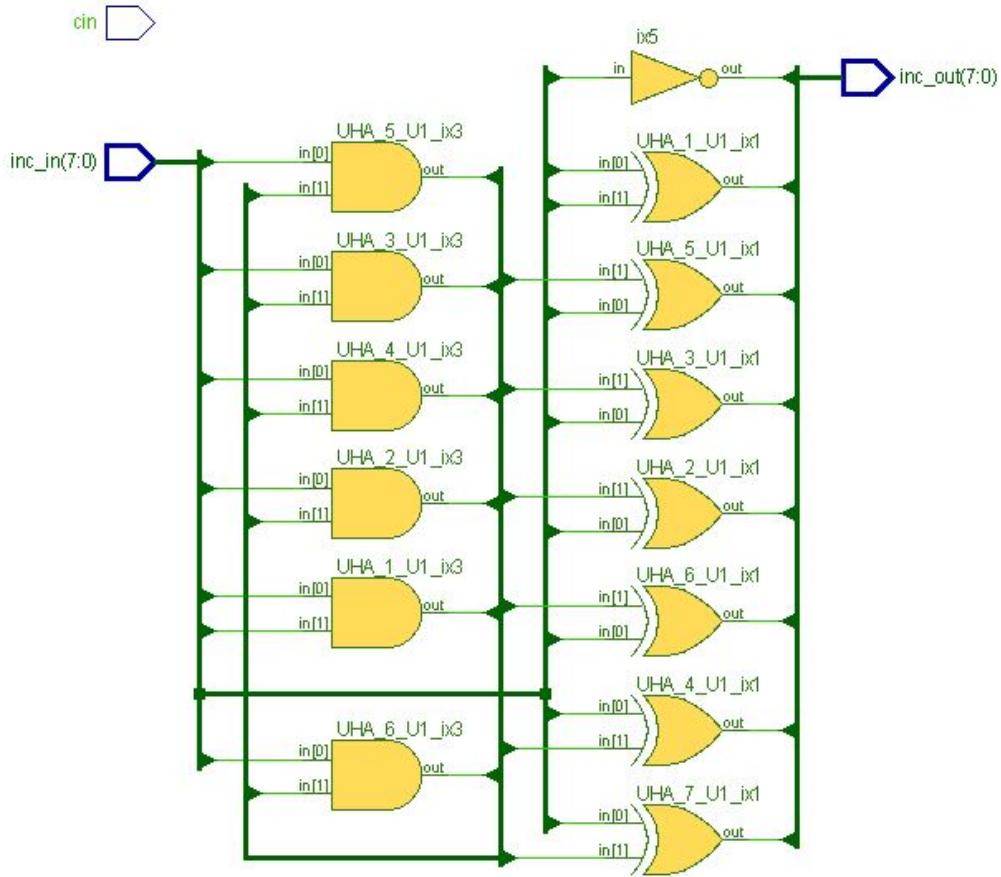


Figure 3 RTL of 8-bit Incrementer

2.2 Multiplier

The multiplier that will be used for the ALU is the radix-4 booth multiplier [1]. This multiplier will basically reduce the number of partial products by half since it doesn't shift and add for every column of the multiplier operand. Instead, the multiplier will operate on four columns by taking every three bits of the multiplier operand. Depending on those three bits, the multiplier will either multiply the multiplicand by either 0, ± 1 , or ± 2 generating $N/2$ partial products where N is the number of bits. Each partial product is shifted by 2 bits. The multiplier will take two signed N -bit input operands and gives a $2N$ signed output resultant.

Table 1 Radix-4 Booth recoding table [1]

Multiplier Bits Block			Multiplier Value	Partial Product
X _{i+1}	X _i	X _{i-1}		
0	0	0	0	Mx0
0	0	1	1	Mx1
0	1	0	1	Mx1
0	1	1	2	Mx2
1	0	0	-2	Mx-2
1	0	1	-1	Mx-1
1	1	0	-1	Mx-1
1	1	1	0	Mx0

For example, consider that we want to multiply two 8-bit signed operands "11100010" (-30) and "01110010" (114). First, a zero is appended to the right side of the multiplier and 4 3-bits will be checked. Going from right to the left, the 4 3-bits are: 100, 001, 110, and 011. According to table 1, the operations will be -2xM, +1xM, -1xM, and +2xM, respectively. Sign extension should also be performed in order to maintain the value and the sign of the partial products. Therefore, the four partial products will be:

PP0: 0000000000111100

PP1: 1111111100010

PP2: 000000011110

PP3: 1111000100

Adding the four partial products will give a sum of “1111001010100100” (-3420) which is correct. The multiplier will be basically composed of partial product generators that will compute the partial products, and an adder in order to add the partial products.

011100100100

Figure 4 3-bit pairing in radix-4 booth recoding

PP0: 0000000000111100
PP1: 1111111100010
PP2: 000000011110
PP3: 1111000100

Sum: 1111001010100100

Figure 5 Addition of the partial products in a radix-4 booth multiplier

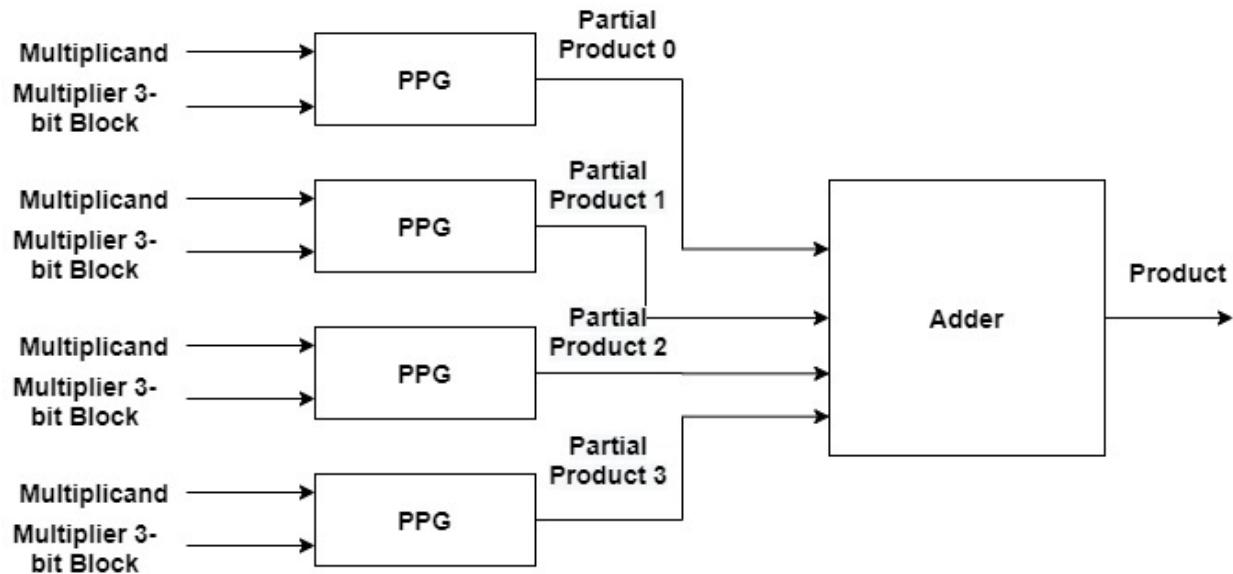


Figure 6 Radix-4 Booth Multiplier Block Diagram

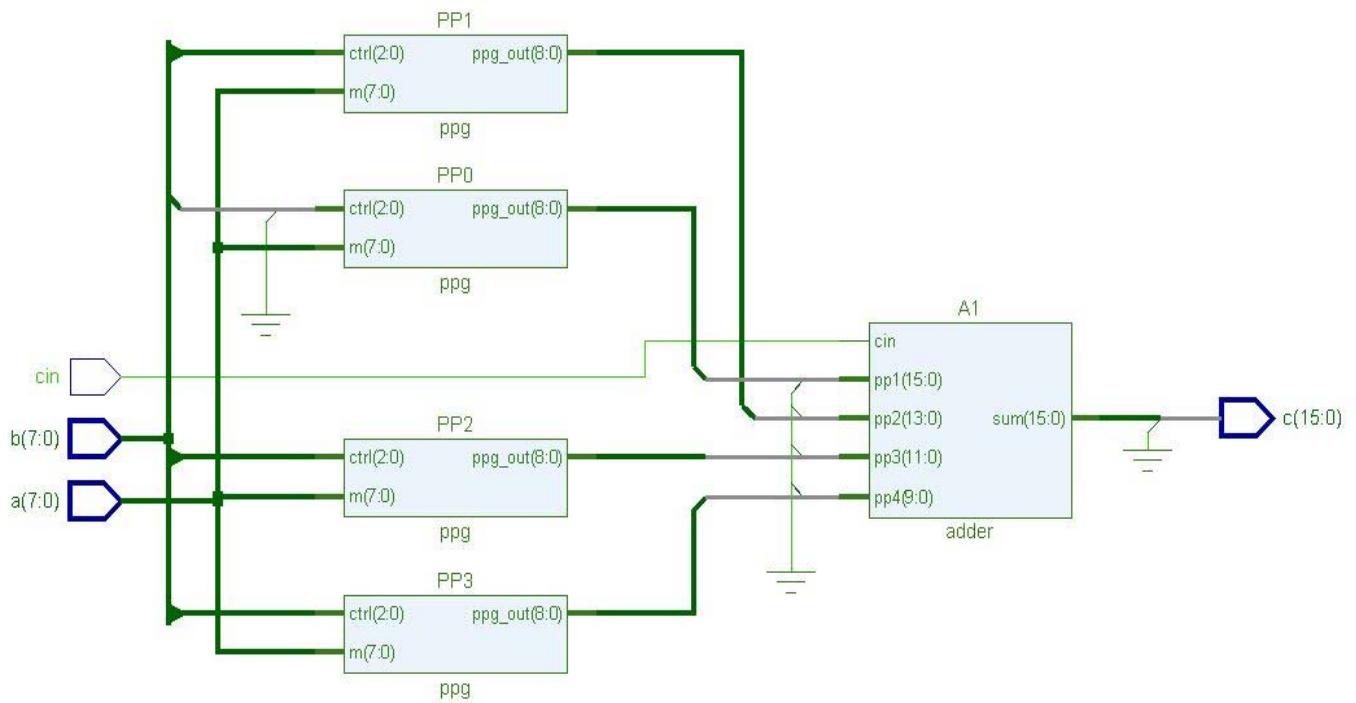


Figure 7 RTL of Radix-4 Booth Multiplier

2.2.1 Partial Product Generator (PPG)

Since an N-bit radix-4 booth multiplier generates $N/2$ partial products, then $N/2$ partial product generators (PPG) are needed. For example, if the multiplier is operating in 8 bits, then 4 PPG's are required. The PPG is made up of a decoder, a two's complement generator, and a shifter.

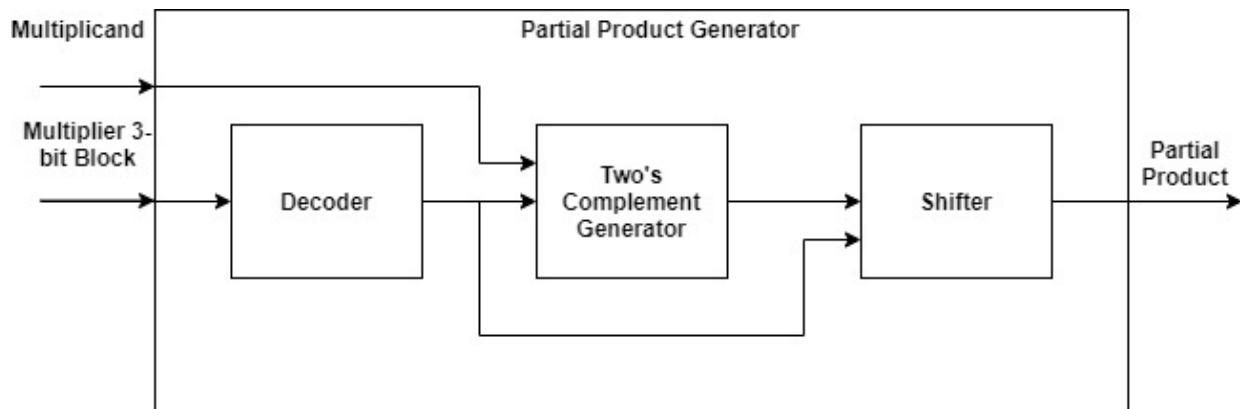


Figure 8 PPG Block Diagram

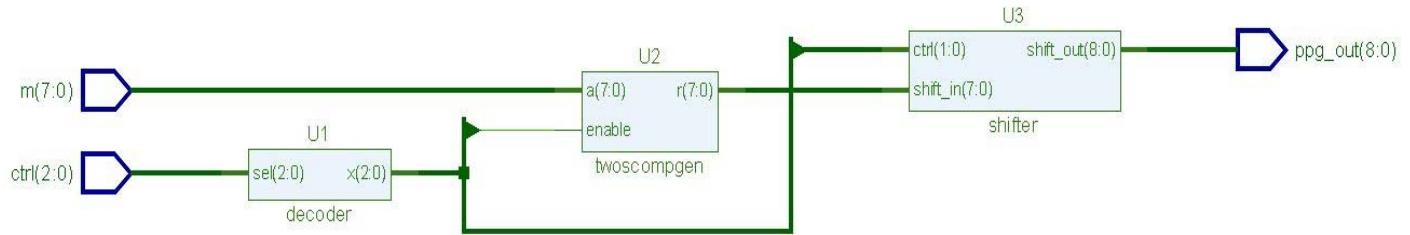


Figure 9 RTL of PPG

2.2.1.1 Decoder

The decoder will take the corresponding 3 bits of the multiplier as input and will give the corresponding 3-bit control signal as output. The LSB of the control signal will be used as the enable signal for the two's complement generator, and the two MSB's will be used as the control for the shifter.

Table 2 Decoder Truth Table

Multiplier Bits Block			Control Signal
X_{i+1}	X_i	X_{i-1}	
0	0	0	000
0	0	1	010
0	1	0	010
0	1	1	100
1	0	0	101
1	0	1	011
1	1	0	011
1	1	1	000

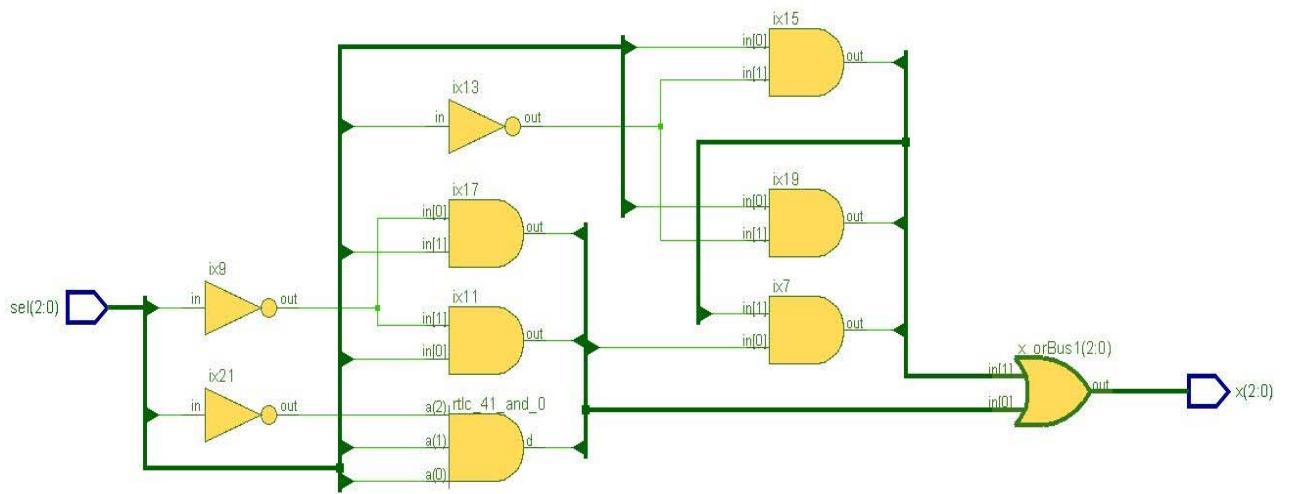


Figure 10 RTL of Decoder

2.2.1.2 Two's Complement Generator

This one here is a different than the one we're using to convert the input operands. This two's complement generator will take the multiplicand as an input. Then, the multiplicand bits are xored with the enable bit. If the enable bit is 0, then the multiplicand will stay the same, whereas, if the enable bit is 1, then all the multiplicand bits will be inverted. After that, an N-bit incrementer is used to add the output of the multiplexers with the enable bit. As you can see, if the enable bit is 0, then the output stays the same, but if it's 1, then two's complement is applied. You could say that the role of this component is to give $-1 \times M$ if needed.

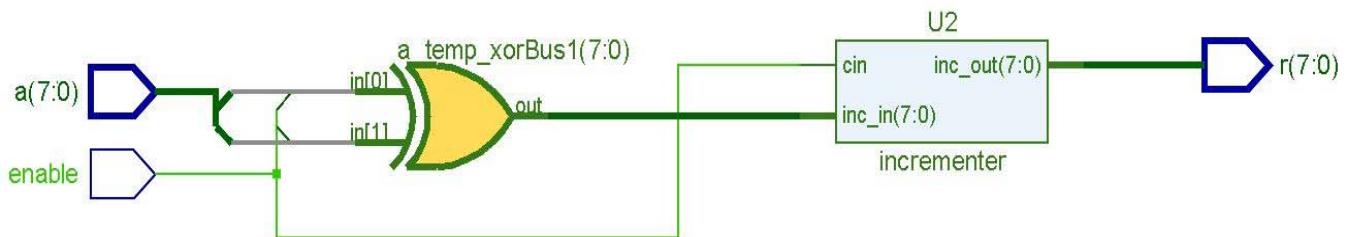


Figure 11 RTL of Two's Complement Generator of PPG

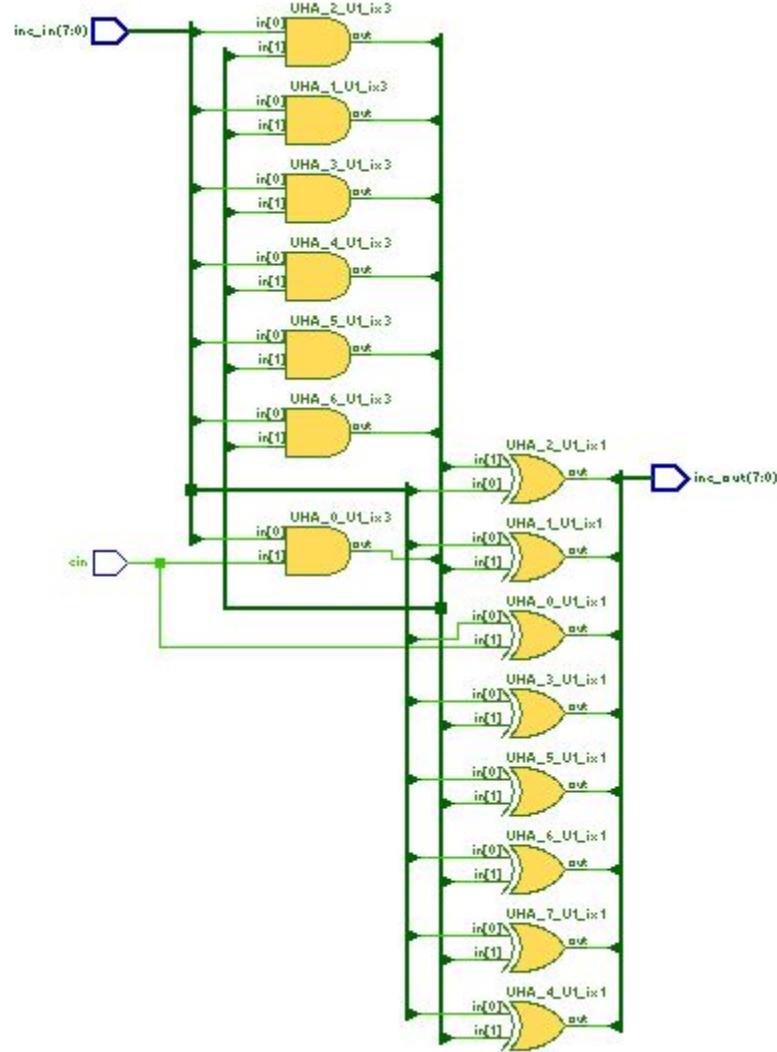


Figure 12 RTL of Incrementer in Two's Complement Generator of PPG

2.2.1.3 Shifter

The role of the shifter is to multiply the multiplicand by either 0, 1, or 2 depending on the 2-bit control signal from the decoder. Meaning, it will either give a zero output, the multiplicand itself, or shift it to the left by 1 bit ($x2$). The LSB of the control signal will be used with a set of $N+1$ multiplexers to choose between '0' (control LSB is 0) or the multiplicand bits (control LSB is 1). Whereas, the MSB of the control signal will be used with another set of $N+1$ multiplexers to choose between the output of the first set (control MSB is 0) or the shifted value of the multiplicand (control MSB is 1).

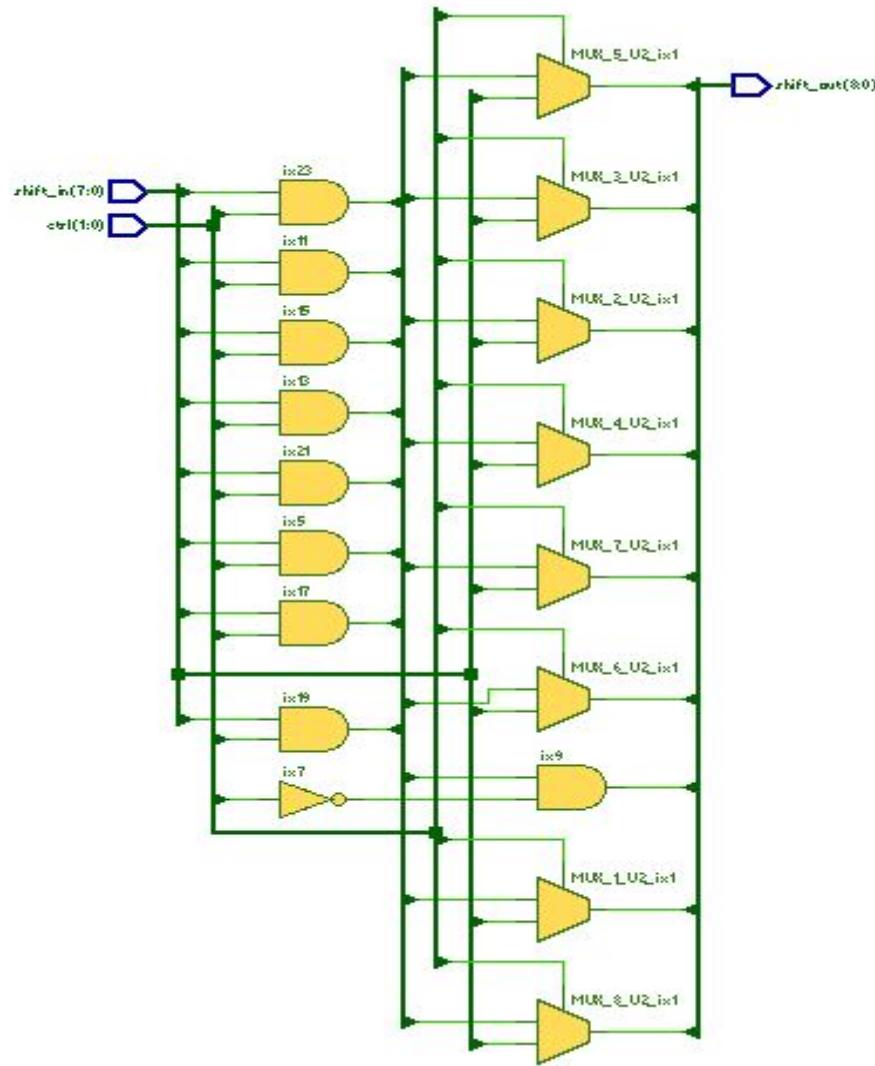


Figure 13 RTL of Shifter

2.2.2 Adder

An adder is needed in order to add the N/2 partial products generated by the PPG's. Since the PPG gives an output of 9 bits and the partial products are shifted by 2 bits each, the partial products will be sign extended to 16 bits, 14 bits, 12 bits, and 10 bits, respectively, when operating in 8 bits. The adder will be composed of three carry-lookahead adders (CLA). A 14-bit CLA will add the first and the second partial products, a 12-bit CLA will add the sum of the 14-bit CLA with the third partial product, and a 10-bit CLA will add the sum of the 12-bit CLA with the fourth partial product.

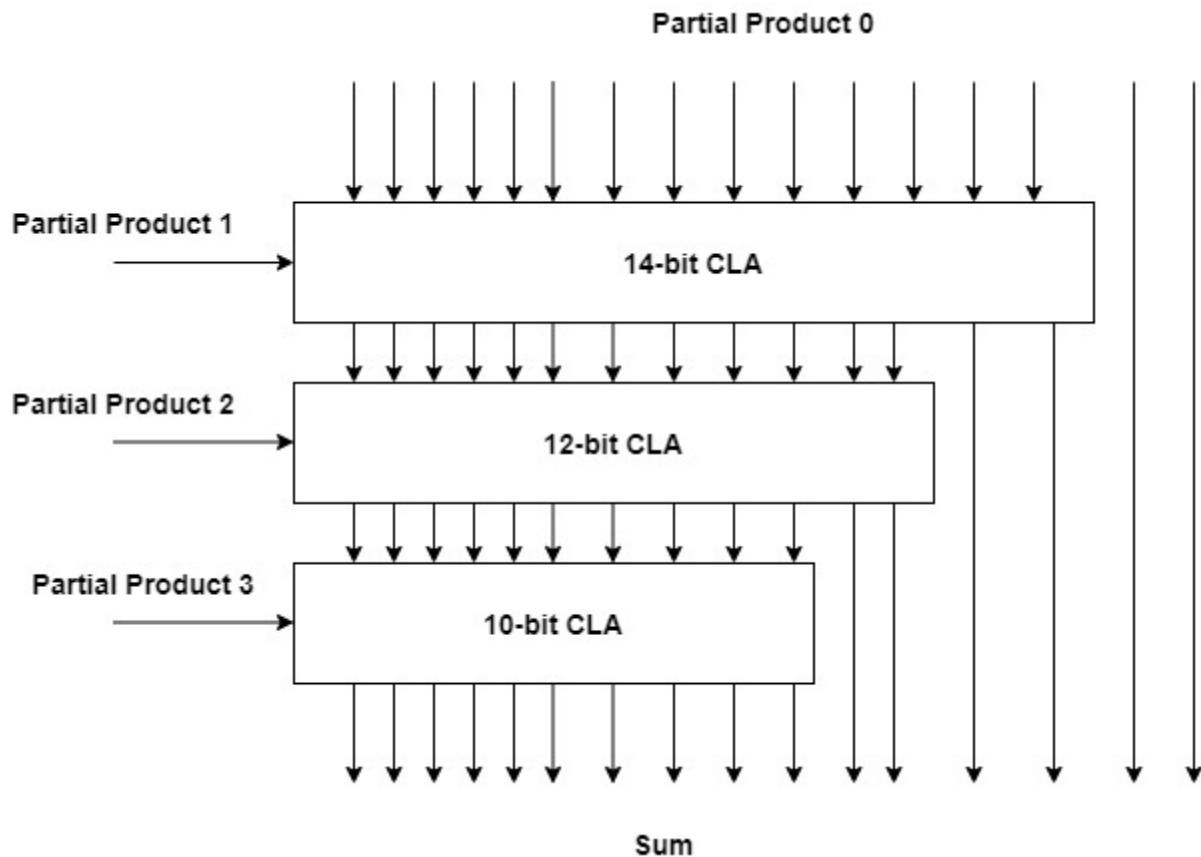


Figure 14 Adder Block Diagram

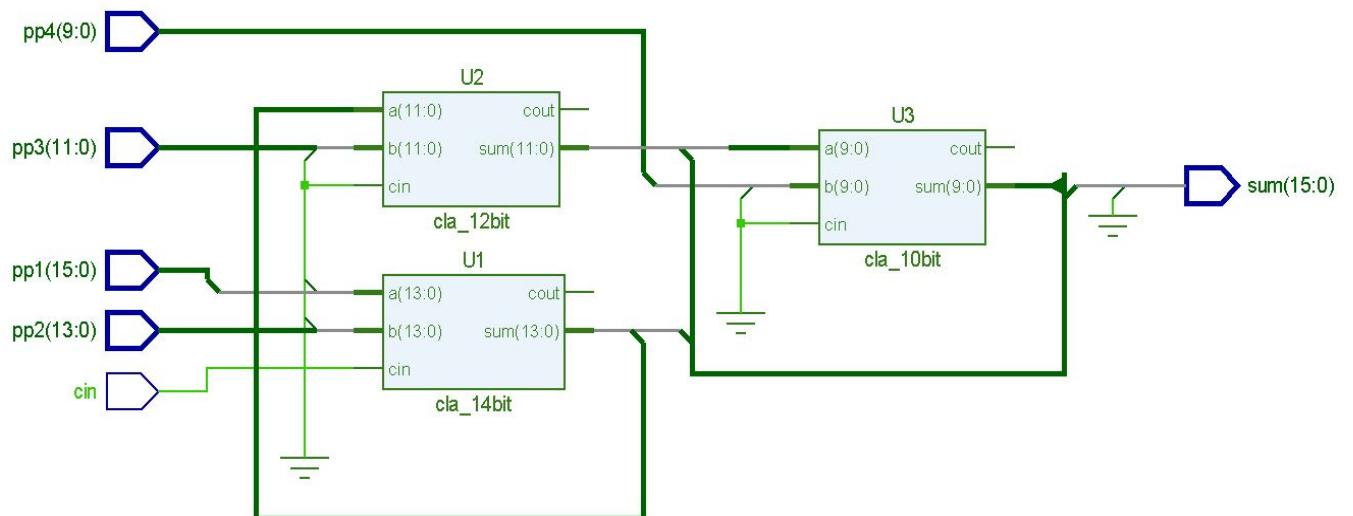


Figure 15 RTL of Adder

2.2.2.1 Carry Look-Ahead Adder

The carry look-ahead adder (CLA) [2] is a fast adder because it calculates the carry bits before the sum which reduces the propagation delay unlike the ripple carry adder that requires the carry bits to be calculated first in order to calculate the sum. The CLA is capable of calculating the carry bits by using two signals that are the generate signal (G) and the propagate signal (P) where $G(i) = A(i)B(i)$ and $P(i) = A(i) + B(i)$. Then, the carry bits are calculated: $C(i+1) = G(i) + (P(i)C(i))$. The CLA is also made up of full adders that add the operand bits with the carry bits.

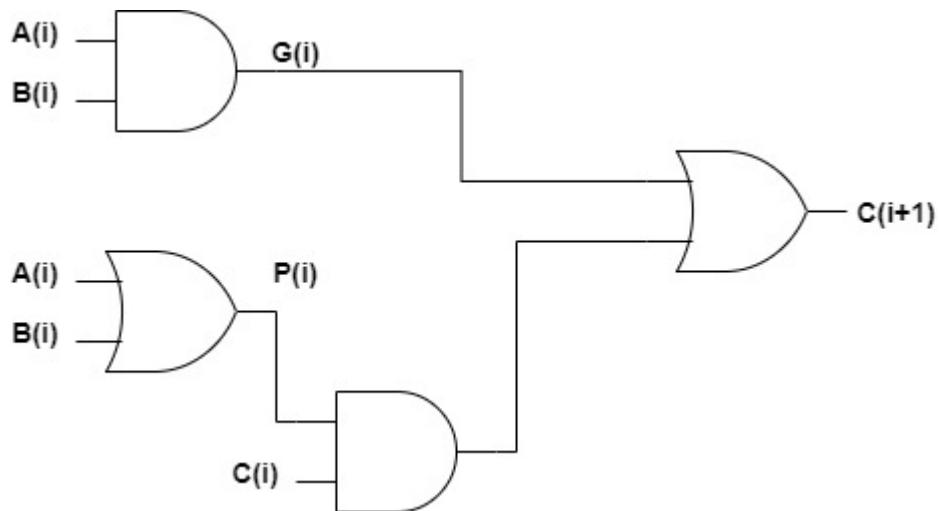


Figure 16 Carry Bit Generator Circuit

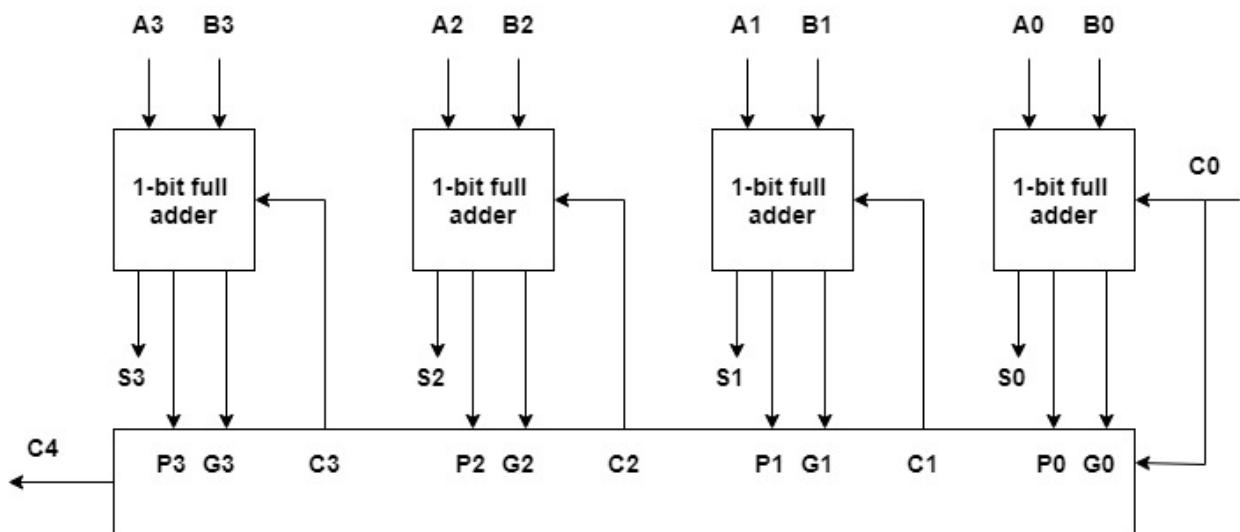


Figure 17 4-bit Carry Look-Ahead Adder Circuit [2]

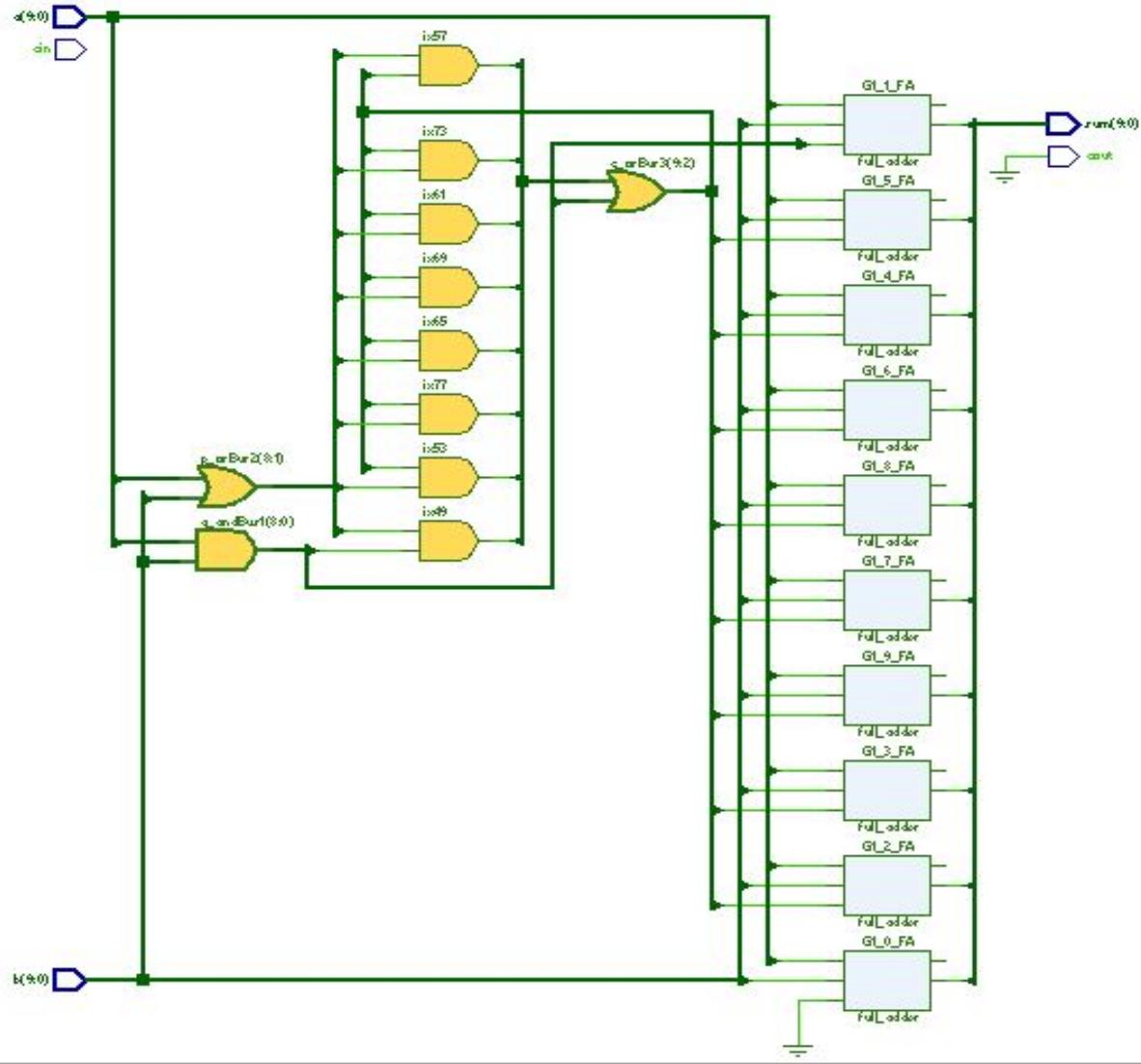


Figure 18 RTL of 10-bit CLA

2.3 Division by Four and Increment by One

In order to divide the product by 4, it should be shifted 2 bits to the right, and in order to increment it by 1, an incrementer is needed. However, instead of using another component, the multiplier could be modified. The output $Z = \frac{A \cdot B}{4} + 1$ can be written as $Z = \frac{A \cdot B + 4}{4}$, therefore, we can start the increment at the third bit of the product. Since the first two bits of the first partial product are not added with the bits of the other partial products, then, they can be neglected and we can add an input carry to the 14-bit CLA of the multiplier adder.

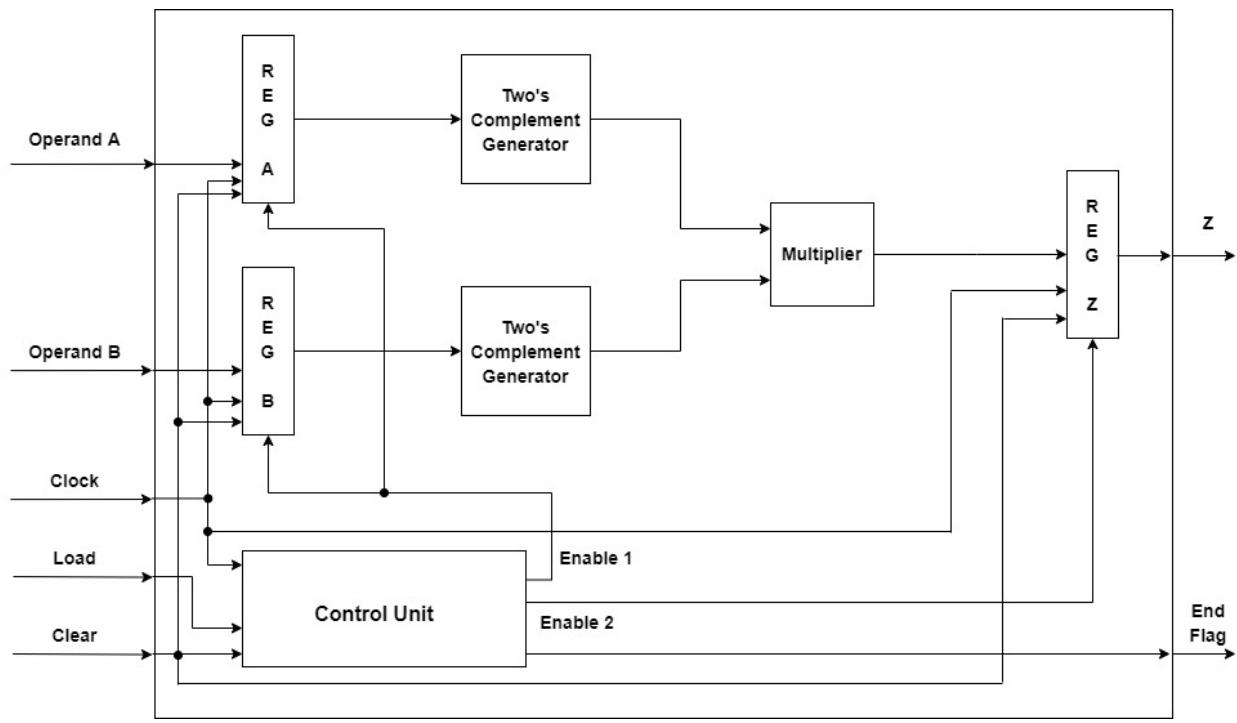


Figure 19 ALU Block Diagram after removing incrementer

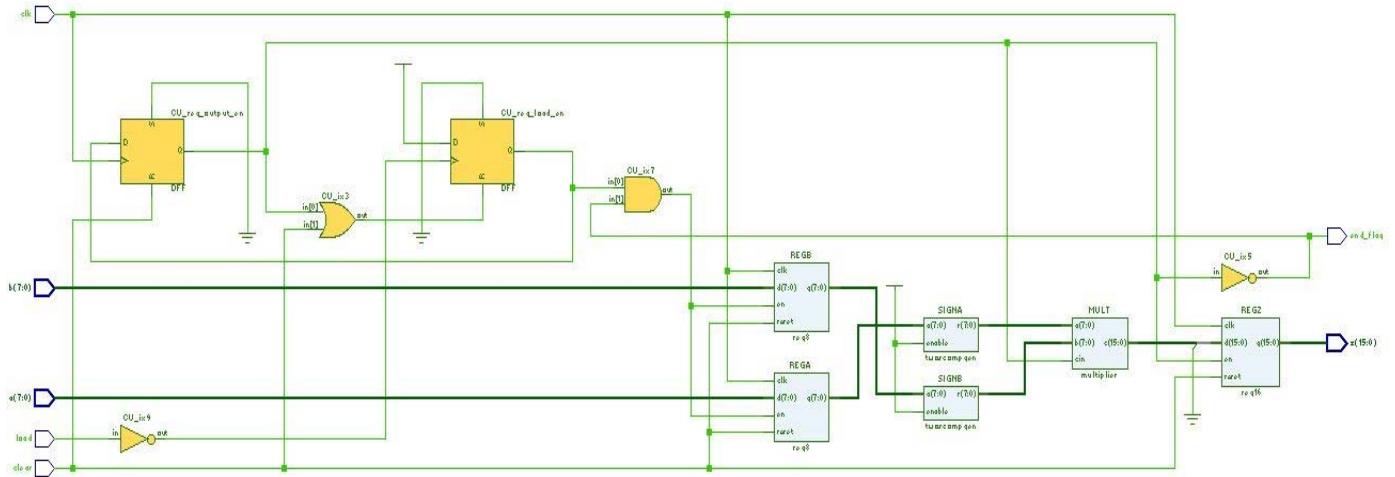


Figure 20 RTL of 8-bit ALU

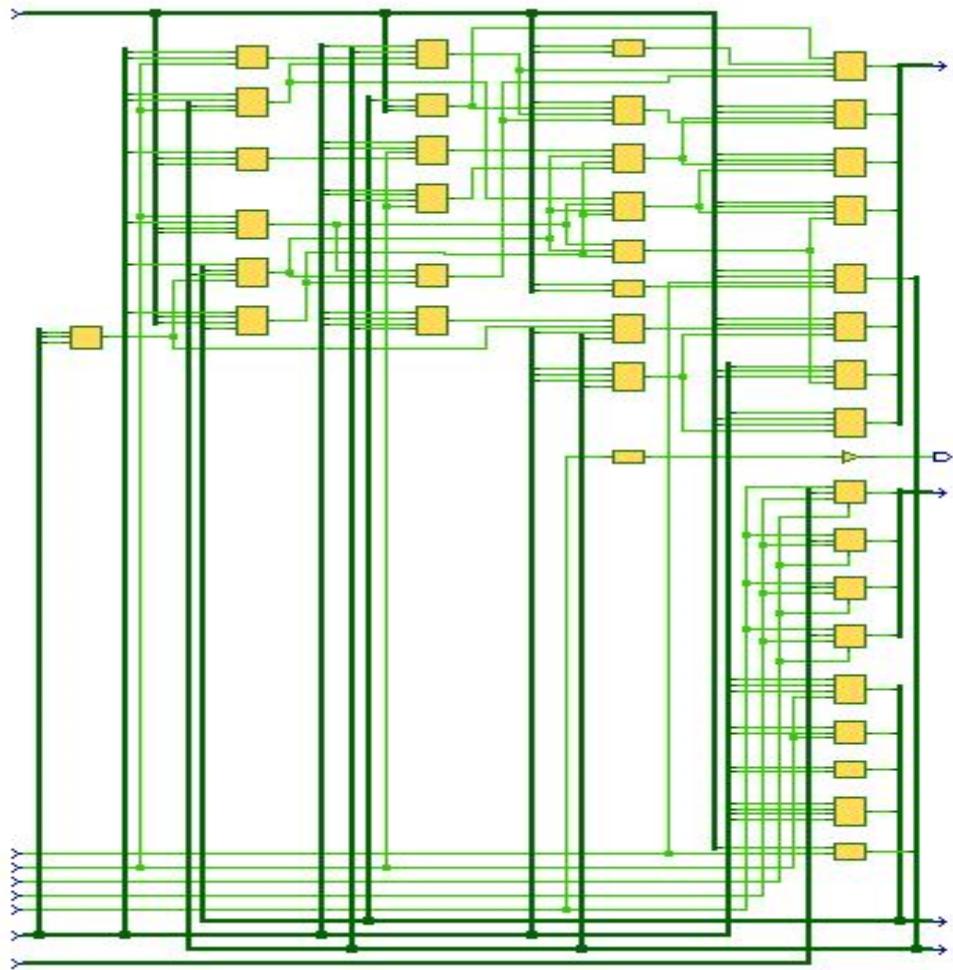


Figure 21 Tech Schematic of 8-bit ALU

2.4 Control Unit

A control unit is needed for the ALU in order to generate the enable signals for the registers and the end flag that indicates the end of each operation. First, when the load signal transitions from 1 to 0, the first enable signal becomes 1. The first enable signal will allow the first to registers A and B to latch the input operands A and B at the first rising edge of the clock. After that, the first enable signal will become 0 but the second enable signal will become 1 at the first rising edge of the clock. The second enable signal will allow the output register Z to latch the output Z at the second rising edge of the clock. At the second rising edge of the clock, the second enable signal will become 0 and the end flag becomes 1. The whole operation takes two clock cycles after the load signal transitions from 1 to 0. In the first clock cycle, the input operands are latched to registers A and B and the product is computed, while, in the second clock cycle, the output is latched to register Z and the end flag becomes 1.

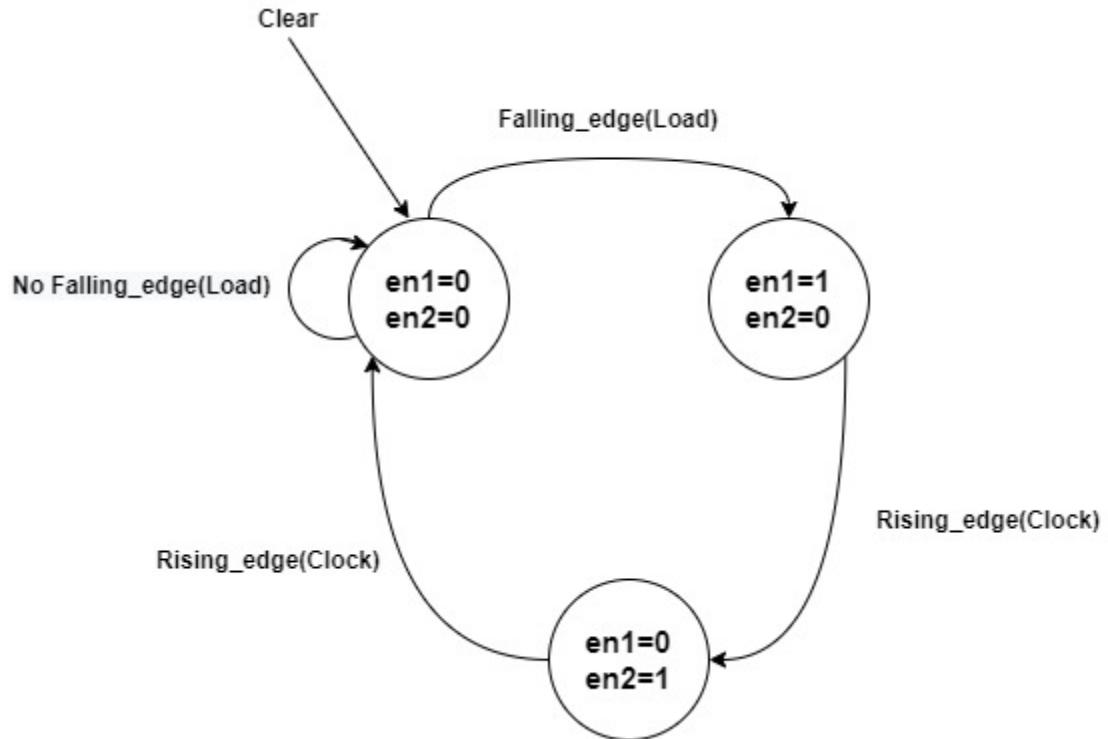


Figure 22 ALU State Diagram

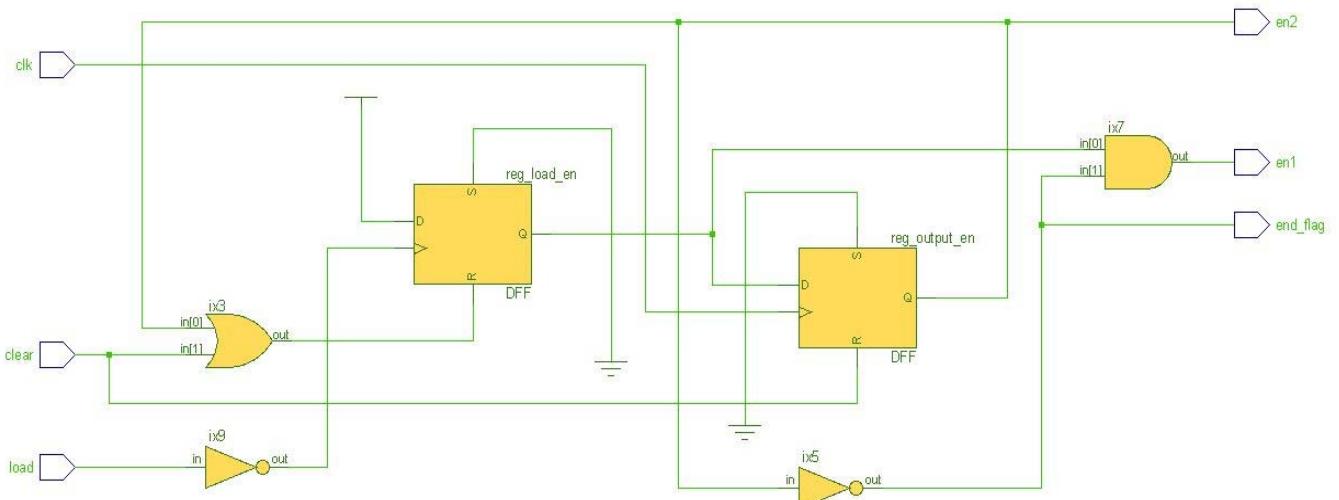


Figure 23 RTL of Control Unit

2.5 Registers

The ALU consists of three registers: two 8-bit registers and one 16-bit register. The two 8-bit registers will latch the input operands when “enable 1” signal is 1. Whereas, the 16-bit register will latch the output result of the ALU when “enable 2” signal is 1.

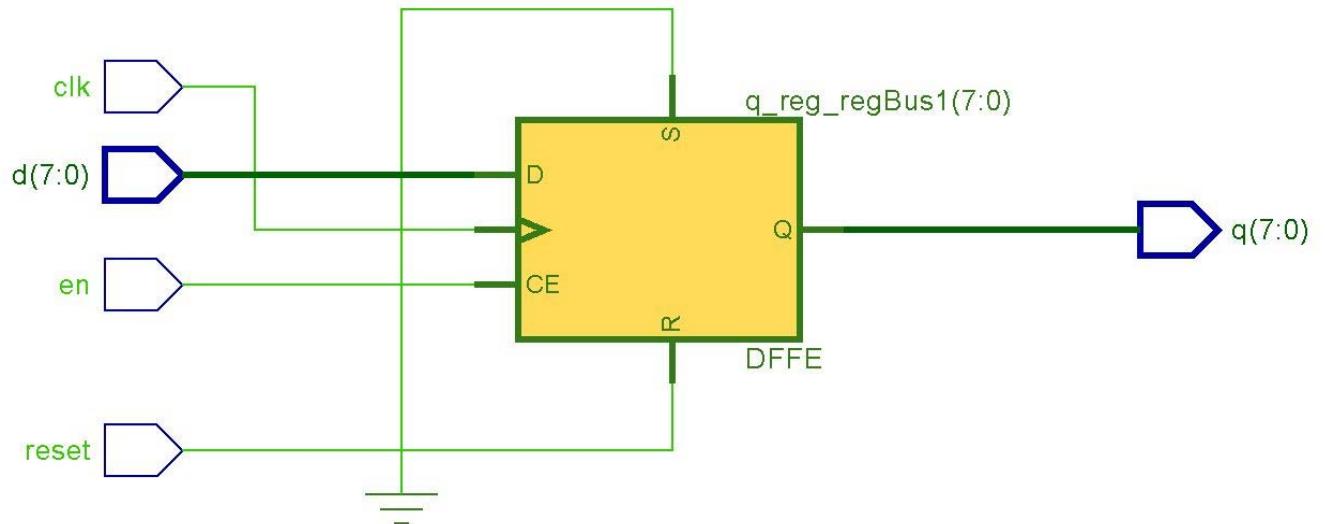


Figure 24 RTL of 8-bit Register

2.6 Test Results and Analysis

The 8-bit ALU design was simulated using Modelsim. We have tried with 10 pairs of input operands (A and B). The signals a and b are unsigned and signals rega_out and regb_out are also unsigned (registers A and B). The remaining signal are signed. As you can see from the simulation results below, when the load signal transitions from 1 to 0, en1 will be 1. After that, the operands will be latched at the first rising edge of the clock and en2 will be 1. During this time, A and B will be converted to signed numbers, multiplied, added by 4, and divided by 4. At the second rising edge, the output is latched to register Z and the end_flag becomes 1.

Set 1: A=142 and B=13

A will be converted to 114 and B to -13. Z at this operation is -370 which is correct since $\frac{114*-13}{4} + 1 = -369.5$

Set 2: A=255 and B=255

A will be converted to 1 and B to 1. Z at this operation is 1 which is correct since $\frac{1*1}{4} + 1 = 1.25$

Set 3: A=73 and B=229

A will be converted to -73 and B to 27. Z at this operation is -492 which is correct since $\frac{-73*27}{4} + 1 = -491.75$

Set 4: A=13 and B=21

A will be converted to -13 and B to -21. Z at this operation is 69 which is correct since $\frac{-13*-21}{4} + 1 = 69.25$

Set 5: A=242 and B=168

A will be converted to 14 and B to 88. Z at this operation is 309 which is correct since $\frac{14*88}{4} + 1 = 309$

Set 6: A=5 and B=227

A will be converted to -5 and B to 29. Z at this operation is -36 which is correct since $\frac{-5*29}{4} + 1 = -35.25$

Set 7: A=163 and B=59

A will be converted to 93 and B to -59. Z at this operation is -1371 which is correct since $\frac{93*-59}{4} + 1 = -1370.75$

Set 8: A=252 and B=0

A will be converted to 4 and B to 0. Z at this operation is 1 which is correct since $\frac{4*0}{4} + 1 = 1$

Set 9: A=71 and B=81

A will be converted to -71 and B to -81. Z at this operation is 1438 which is correct since $\frac{-71*-81}{4} + 1 = 1438.75$

Set 10: A=93 and B=171

A will be converted to -93 and B to 85. Z at this operation is -1976 which is correct since $\frac{-93*85}{4} + 1 = -1975.25$

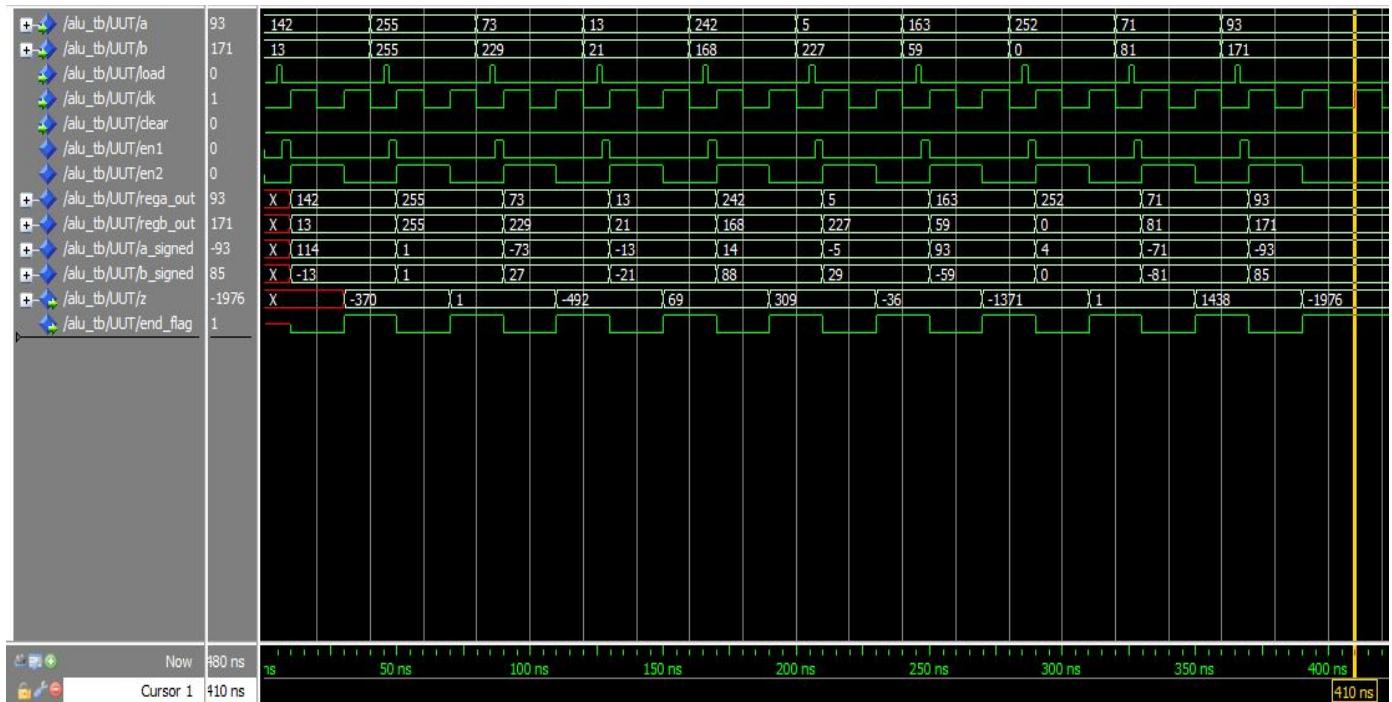


Figure 25 Simulation Waveforms of 8-bit ALU

As you can see in the following figure, the clear signal was able to clear all the registers and also set the end_flag to 1 once it became 1. The ALU will remain in this state until another operation begins.

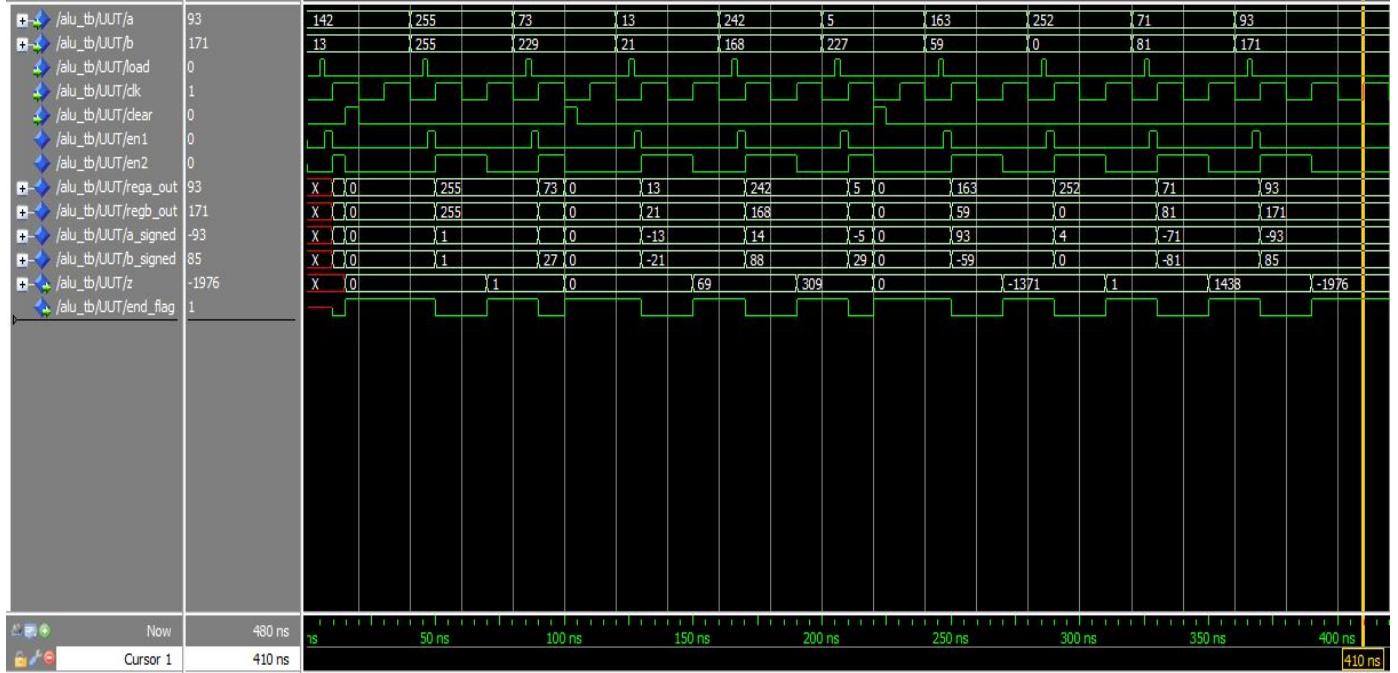


Figure 26 Simulation Waveforms of 8-bit ALU with clear

We were also able to synthesize another 2 ALU designs in order to compare them with our design. The first design uses a regular multiplier that uses basic binary multiplication (shifting and adding) with ripple carry adders (RCA). The second design is similar to our design but uses radix-2 booth multiplier that uses two bits from the multiplier term instead of three which gives N partial products instead of N/2. After that, we were able to obtain the areas and the delays of the three design. The results show that our design had the least area: 32 % less slices than design 1 and 41 % less slices than design 2. Our design also had the least delay: 36.6 % less time than design 1 and 32.5 % less time than design 2.

Table 3 Area of Each ALU Design

	LUTs	CLB Slices	Dffs or Latches
ALU with regular multiplier	301	151	32
ALU with radix-2 booth multiplier	348	174	32
ALU with radix-4 booth multiplier	204	102	32

Table 4 Delay of Each ALU Design

	Delay
ALU with regular multiplier	16.786 ns
ALU with radix-2 booth multiplier	15.774 ns
ALU with radix-4 booth multiplier	10.642 ns

3 Expansion to 16 Bits

3.1 Concept

In order to expand the design for 16-bit operands, more components are needed and the main components also need to be expanded to 16 bits. The Two's complement generators, incrementer, shifter, ppg's are expanded to 16-bits. Registers A and B are expanded to 16 bits while register Z is expanded to 32 bits. Since the number of bits is 16, then, there will be 8 partial products which means that 8 ppg's and 7 CLA's (30-bit CLA, 28-bit CLA, 26-bit CLA, 24-bit CLA, 22-bit CLA, 20-bit CLA, 18-bit CLA). That's the main difference from the 8-bit design, however, they both have the same logic. The decoder and the control unit will remain the same.

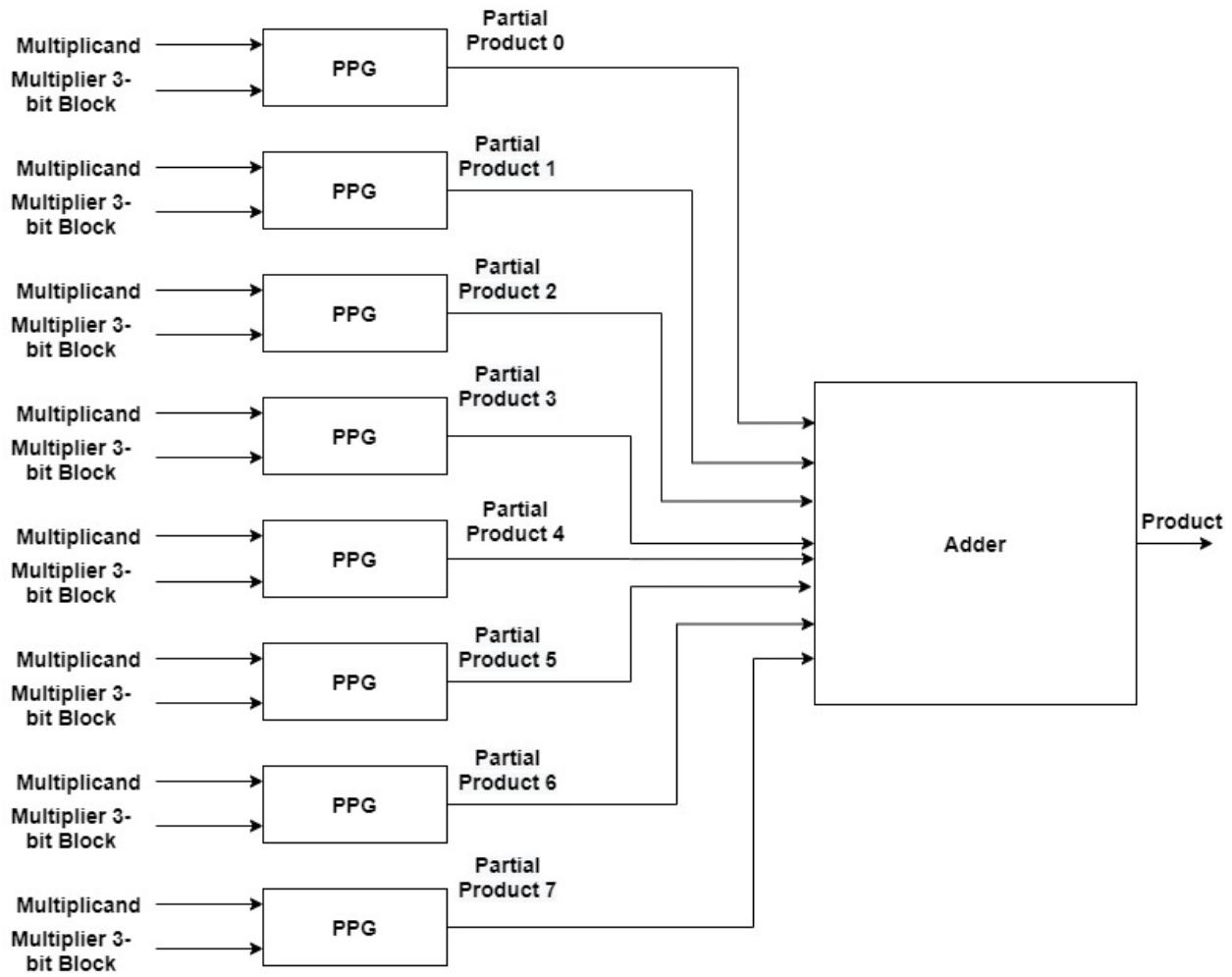


Figure 27 16-bit Radix-4 Booth Multiplier Block Diagram

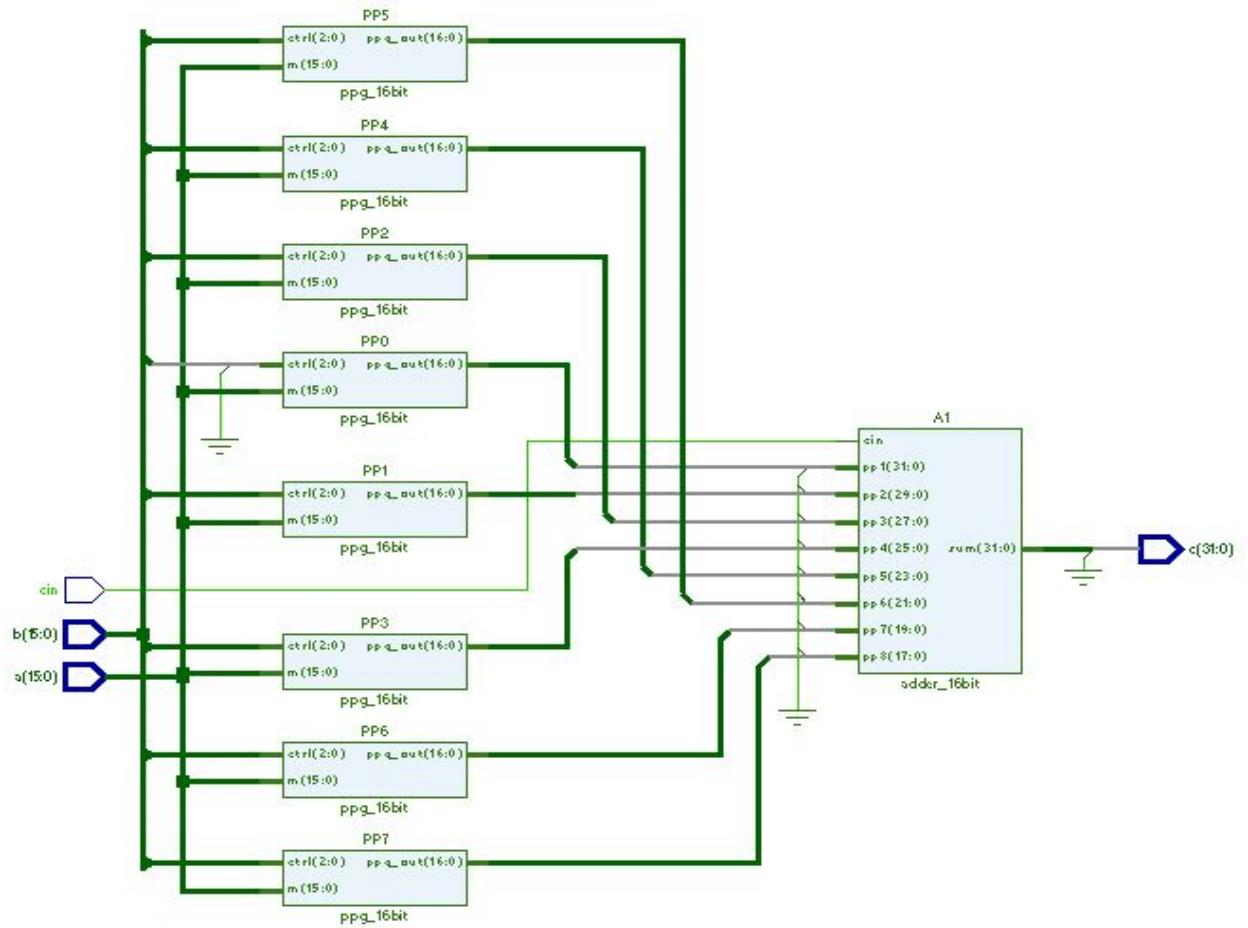


Figure 28 RTL of 16-bit Radix-4 Booth Multiplier

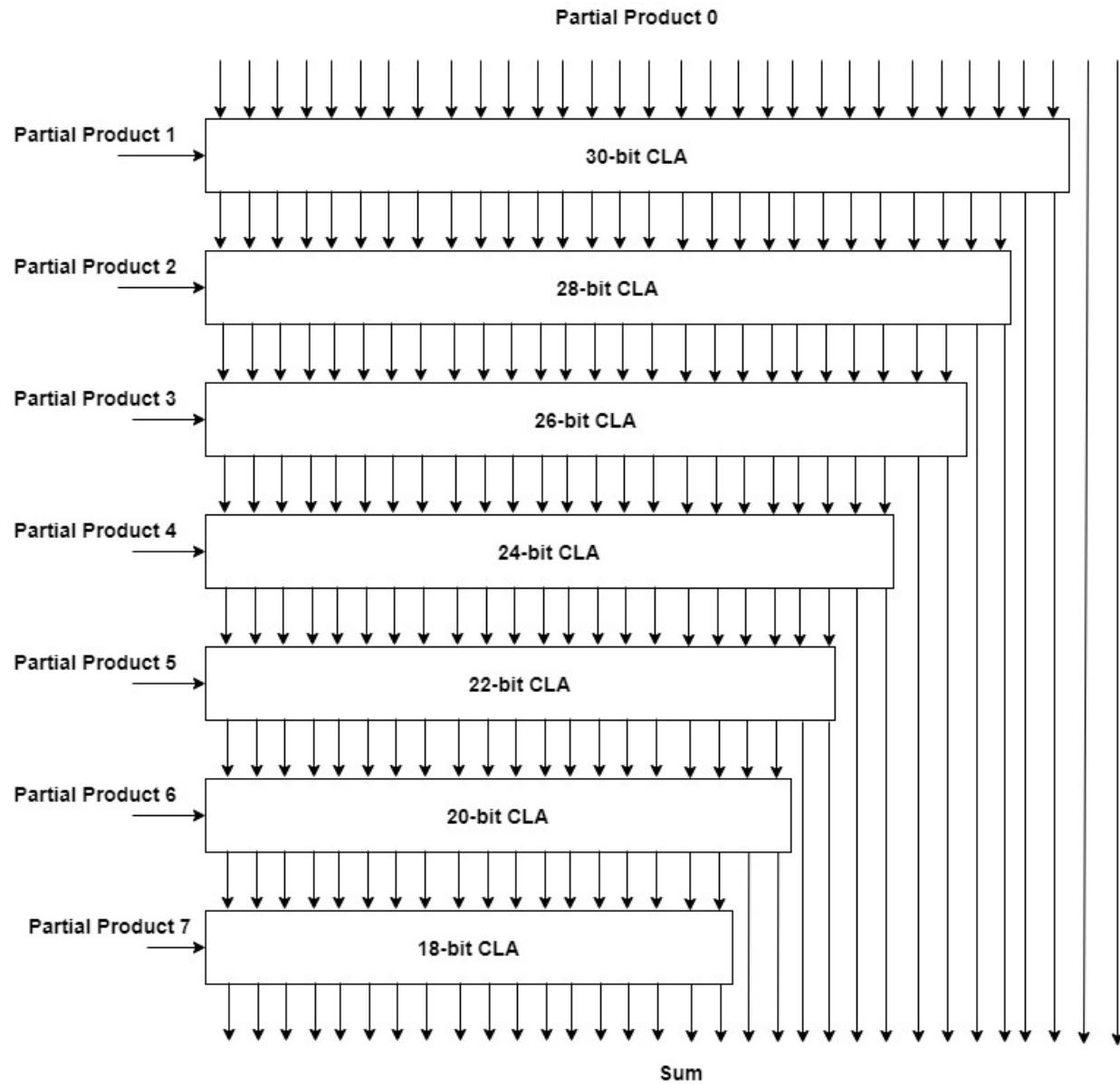


Figure 29 16-bit Adder Block Diagram

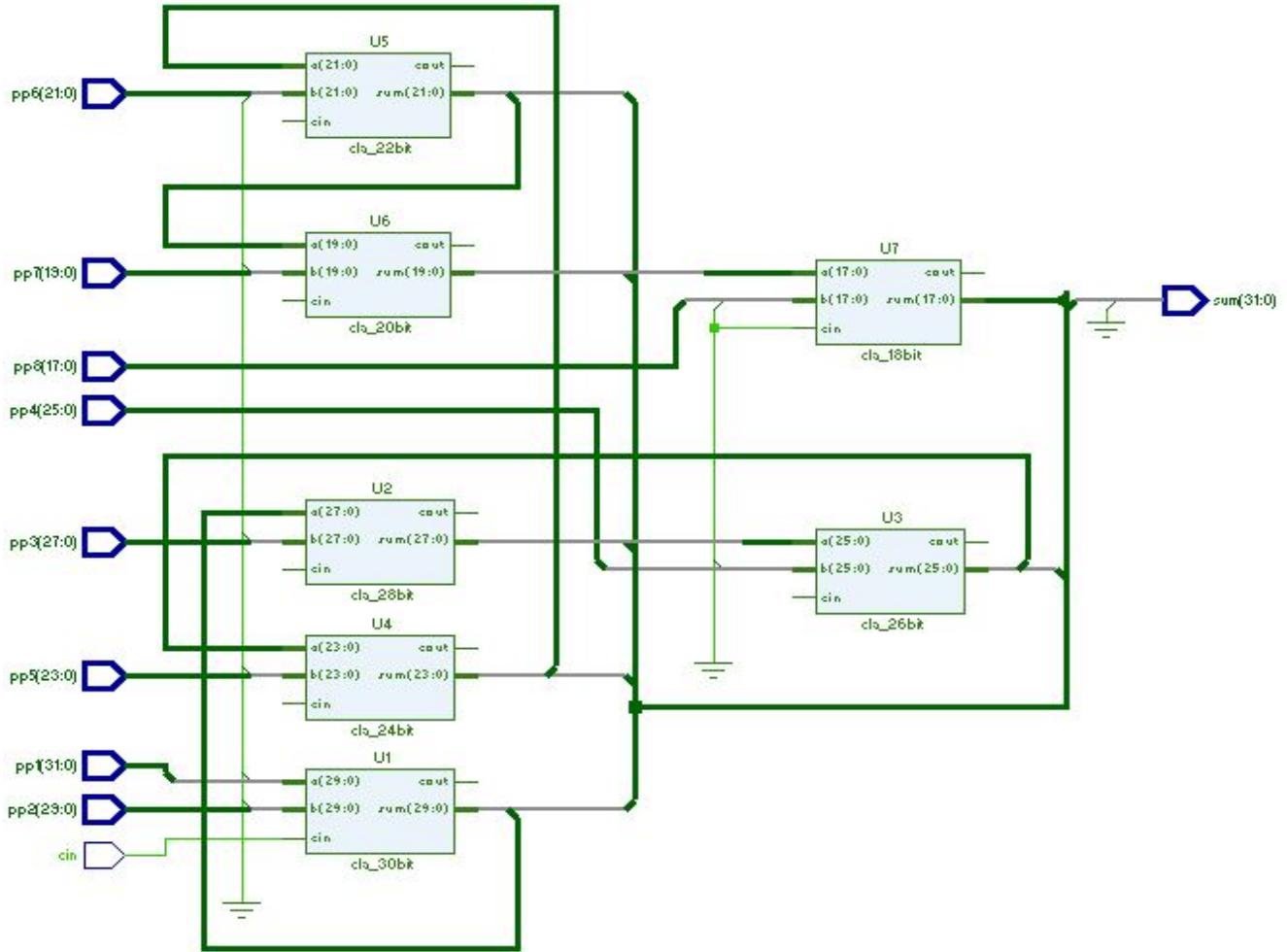


Figure 30 RTL of 16-bit Adder

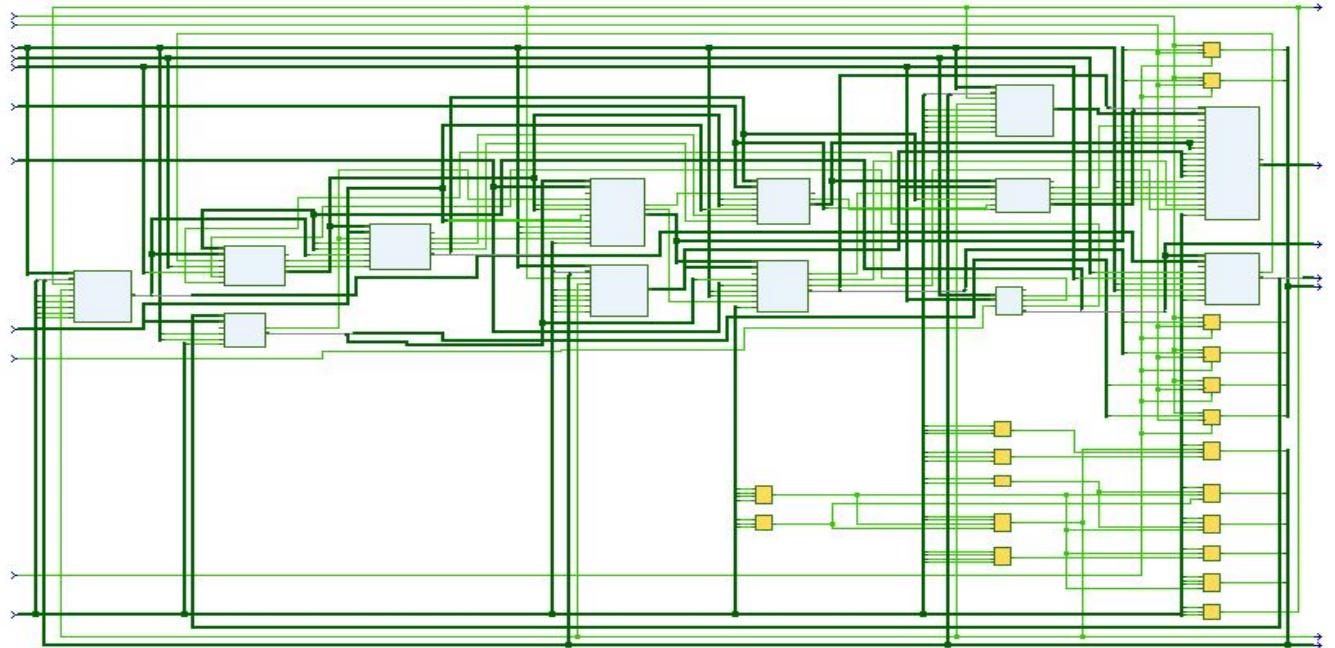


Figure 31 Tech Schematic of 16-bit ALU

3.2 Test Results and Analysis

You can notice here that the simulation waveforms are similar as the ones of the 8-bit version but the input operands are in 16 bits and the output is 32 bits. We also used 10 pairs of input operands.

Set 1: A=45291 and B=30220

A will be converted to 20245 and B to -30220. Z at this operation is -152950974 which is correct since

$$\frac{20245 * -30220}{4} + 1 = -152950974$$

Set 2: A=42573 and B=40497

A will be converted to 22963 and B to 25039. Z at this operation is 143742640 which is correct since

$$\frac{22963 * 25039}{4} + 1 = 143742640.3$$

Set 3: A=18853 and B=17442

A will be converted to -18853 and B to -17442. Z at this operation is 82208507 which is correct since

$$\frac{-18853 * -17442}{4} + 1 = 82208507.5$$

Set 4: A=9938 and B=58403

A will be converted to -9938 and B to 7133. Z at this operation is -17721938 which is correct since

$$\frac{-9938 * 7133}{4} + 1 = -17721937.5$$

Set 5: A=61770 and B=61770

A will be converted to 3766 and B to 3766. Z at this operation is 3545690 which is correct since $\frac{3766*3766}{4} + 1 = 3545690$

Set 6: A=1269 and B=20976

A will be converted to -1269 and B to -20976. Z at this operation is 6654637 which is correct since

$$\frac{-1269 * -20976}{4} + 1 = 6654637$$

Set 7: A=45635 and B=41226

A will be converted to 19901 and B to 24310. Z at this operation is 120948328 which is correct since

$$\frac{93*59}{4} + 1 = 120948328.5$$

Set 8: A=63628 and B=61845

A will be converted to 1908 and B to 3691. Z at this operation is 1760608 which is correct since $\frac{1908*3691}{4} + 1 = 1760608$

Set 9: A=65535 and B=65283

A will be converted to 1 and B to 253. Z at this operation is 64 which is correct since $\frac{1*253}{4} + 1 = 64.25$

Set 10: A=0 and B=7372

A will be converted to 0 and B to -7372. Z at this operation is 0 which is correct since $\frac{0*-7372}{4} + 1 = 1$

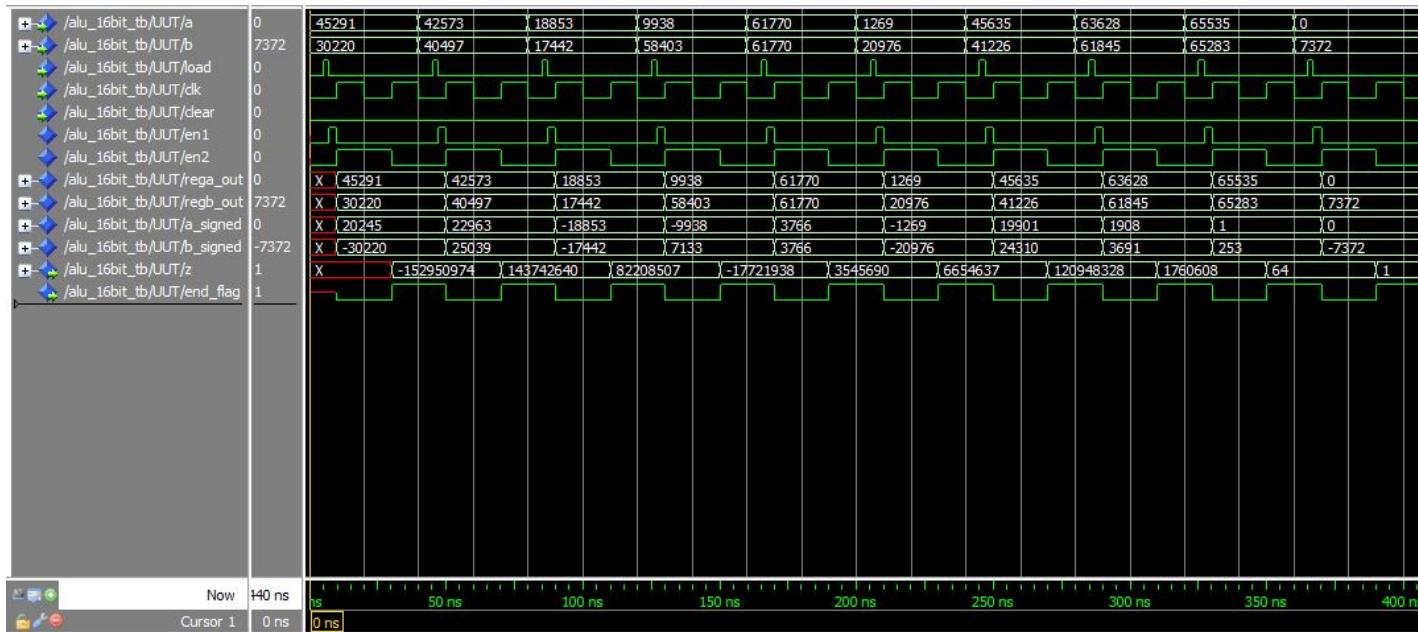


Figure 32 Simulation Waveforms of 16-bit ALU

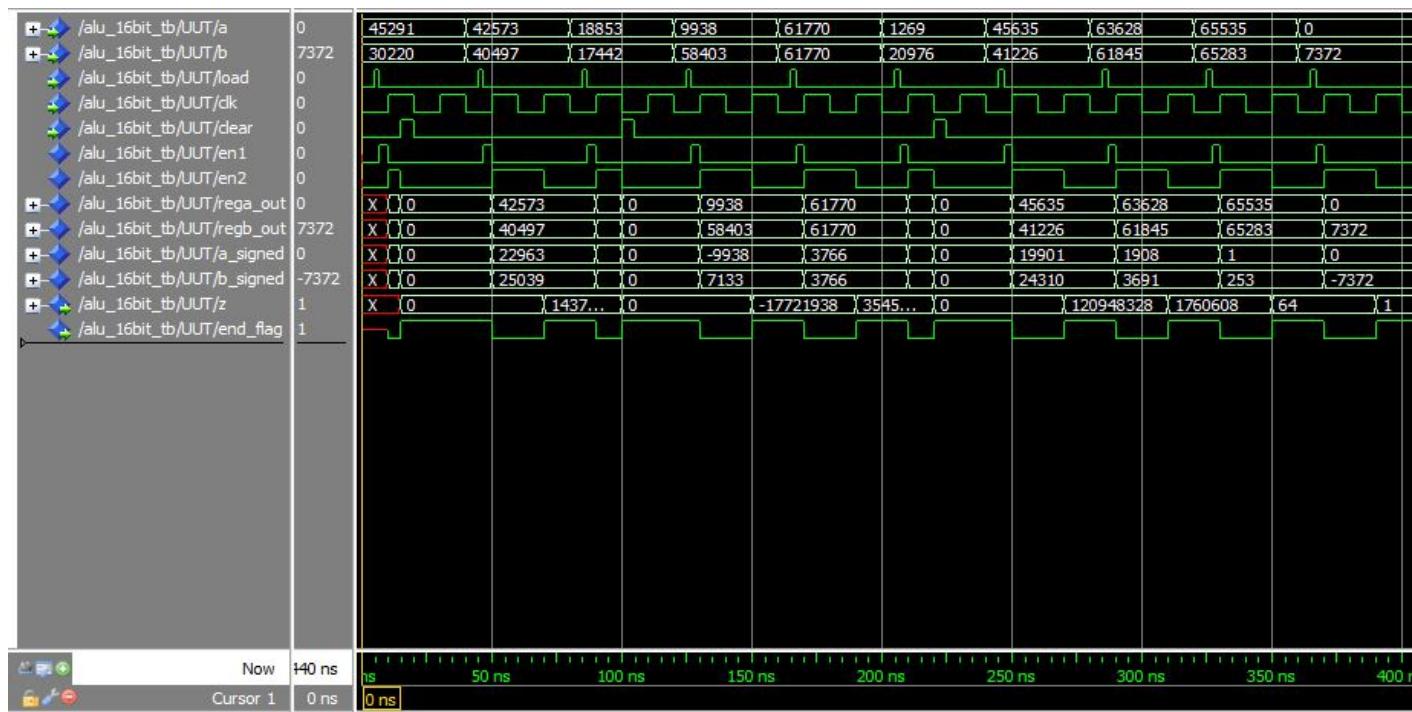


Figure 33 Simulation Waveforms of 16-bit ALU with clear

The 16-bit version has a larger area: 334.31 % increase in slices. It also has a larger delay: 121.92 % increase in delay.

Table 5 Area of 8-bit and 16-bit ALU

	LUTs	CLB Slices	Dffs or Latches
8-bit ALU	204	102	32
16-bit ALU	886	443	64

Table 6 Delay of 8-bit and 16-bit ALU

	Delay
8-bit ALU	10.642 ns
16-bit ALU	23.617 ns

4 Pipelining of The Design

4.1 Concept

Since the operation is taking 2 clock cycles, pipelining can be used to reduce the total number of clock cycles. For example, let's say we have 5 operations, then, it will take 10 clock cycles, but with pipelining, this will take 6 clock cycles. In order to implement pipelining, we need to modify the control unit and add a counter. Let's say we have 10 sets of inputs. When the load signal transitions from 1 to 0, en1 will become 1. After the first rising edge of the clock, en2 will become 1. Both en1 and en2 will remain 1 until the max is reached which is 10. The end flag will also become 1 after the max is reached.

Operation	1		2		3		4		5	
Stage 1	Red		Blue		Yellow		Green		Orange	
Stage 2		Red		Blue		Yellow		Green		Orange
Clock	1	2	3	4	5	6	7	8	9	10

Figure 34 Time Diagram without Pipelining

Operation	1	2	3	4	5	
Stage 1	Red	Blue	Yellow	Green	Orange	
Stage 2		Red	Blue	Yellow	Green	Orange
Clock	1	2	3	4	5	6

Figure 35 Time Diagram with Pipelining

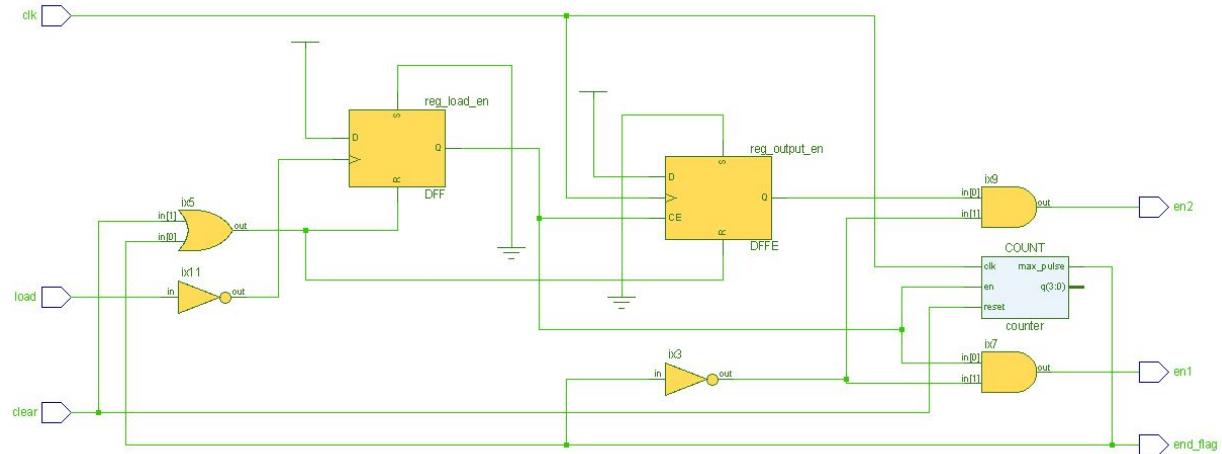


Figure 36 RTL of Control Unit with Pipelining

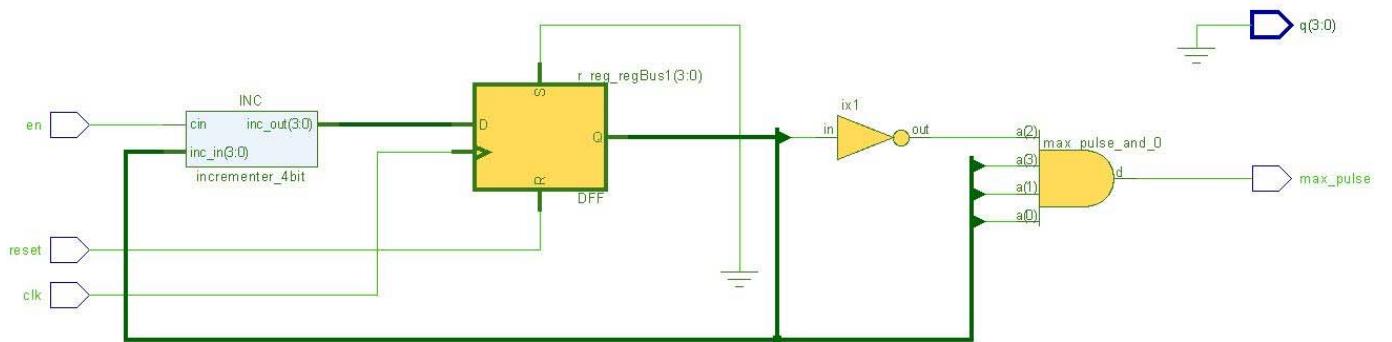


Figure 37 RTL of Counter

4.2 Test Results and Analysis

We can see here that the total number of clock cycles has decreases from 20 to 11.

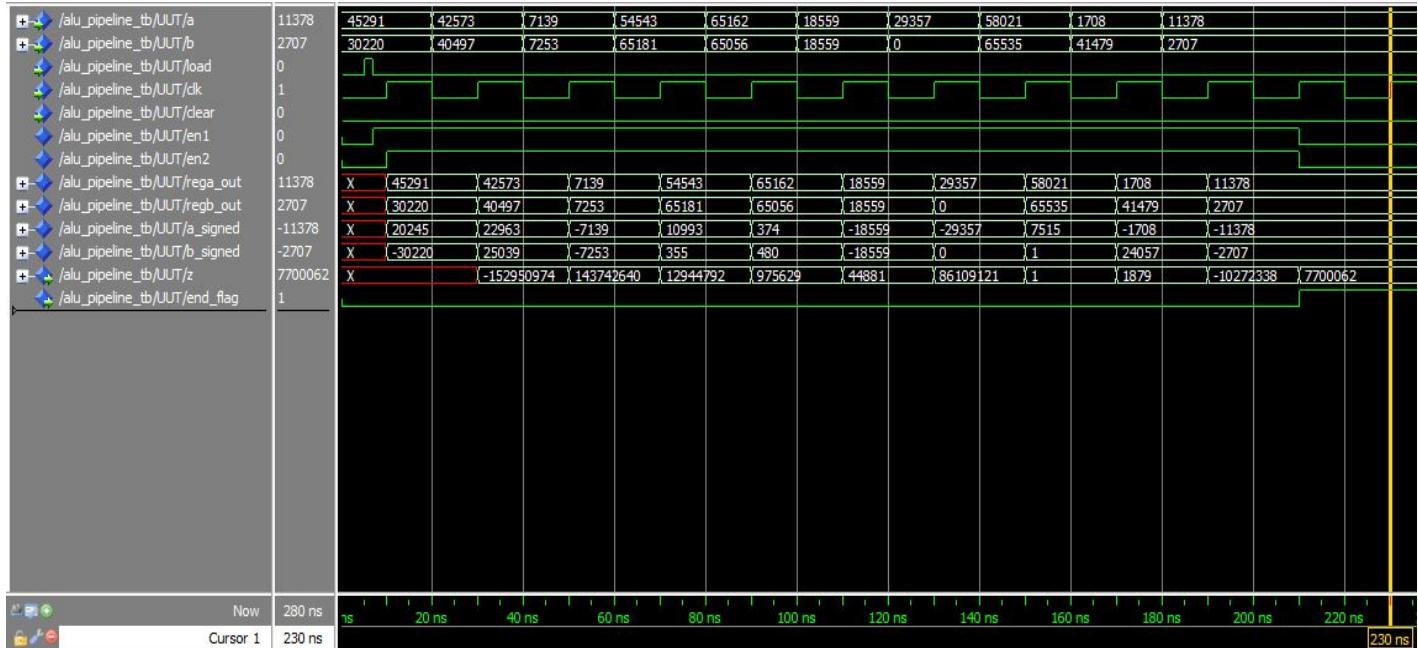


Figure 38 Simulation Waveforms of 16-bit ALU pipelined

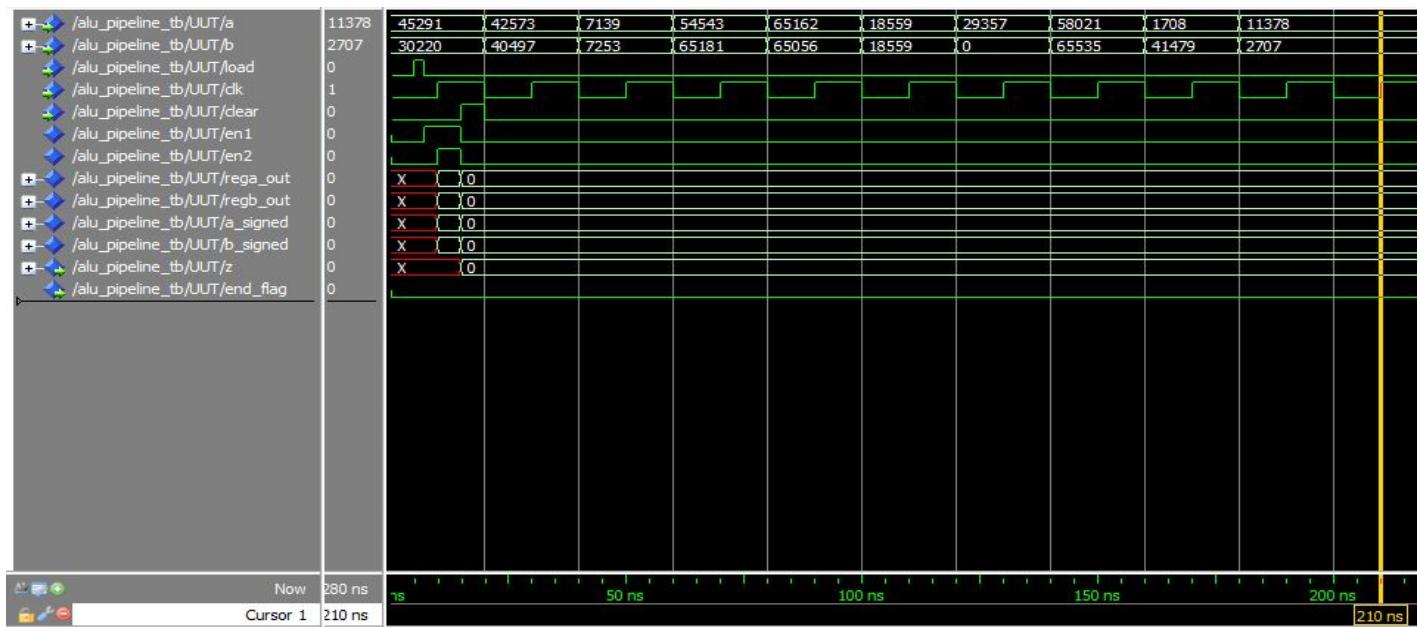


Figure 39 Simulation Waveforms of 16-bit ALU pipelined with clear 1

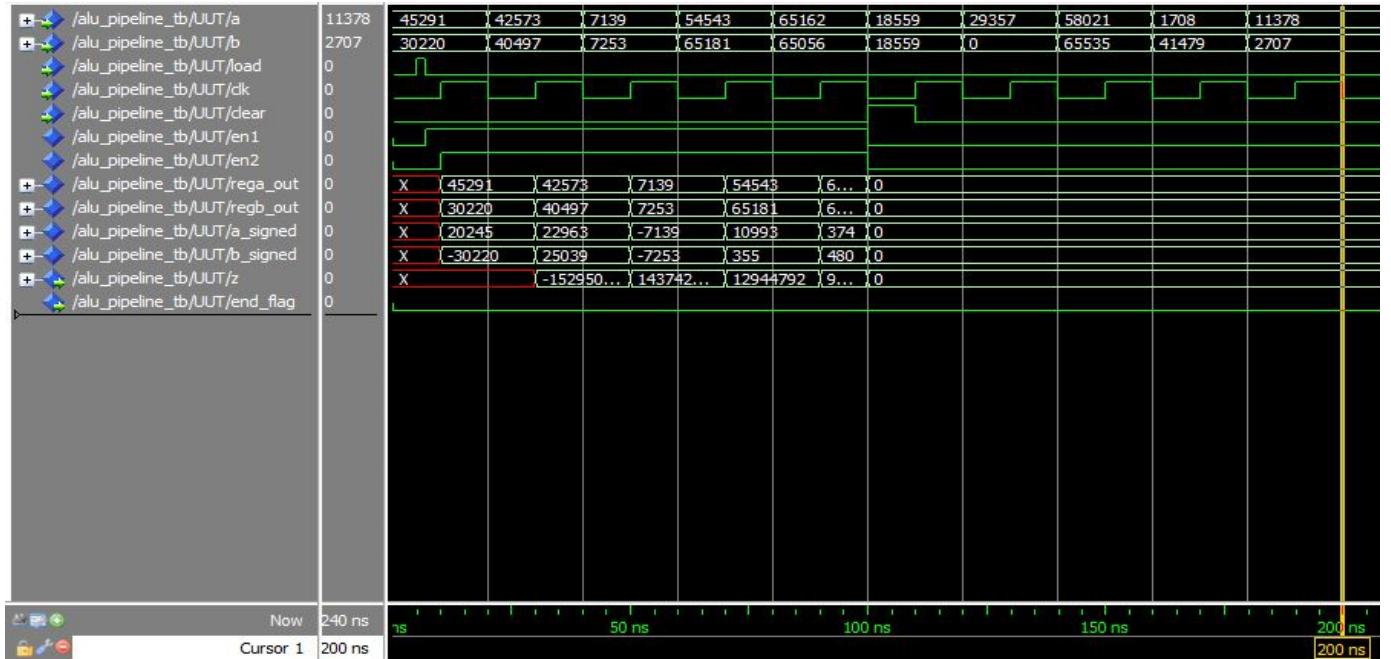


Figure 40 Figure 38 Simulation Waveforms of 16-bit ALU pipelined with clear 2

The pipelined version only increases the area by 0.9 % slices. Whereas the delay remains the same.

Table 7 Area of the normal and the pipelined version

	LUTs	CLB Slices	Dffs or Latches
16-bit ALU	886	443	64
16-bit ALU pipelined	893	447	68

Table 8 Delay of the normal and the pipelined version

	Delay
16-bit ALU	23.617 ns
16-bit ALU pipelined	23.617 ns

5 Multiply Accumulate for Additional operands

5.1 Concept

In this version, we will be using the 16-bit pipelined version along with a few additions and modifications. This design will basically compute the product in each operation and add it to the previous product and latch it to register C. Once the maximum number of operations is reached, the total sum will be shifted by two bits to the right (division by 4) and then incremented by 1. When the maximum is reached, the control unit will set “enable 3” to 1 and the final result is latched to register Z. Both registers C and Z are 36-bits.

The ALU will perform the following operation: $Z = \frac{\sum_{i=1}^n A_i * B_i}{4} + 1$.

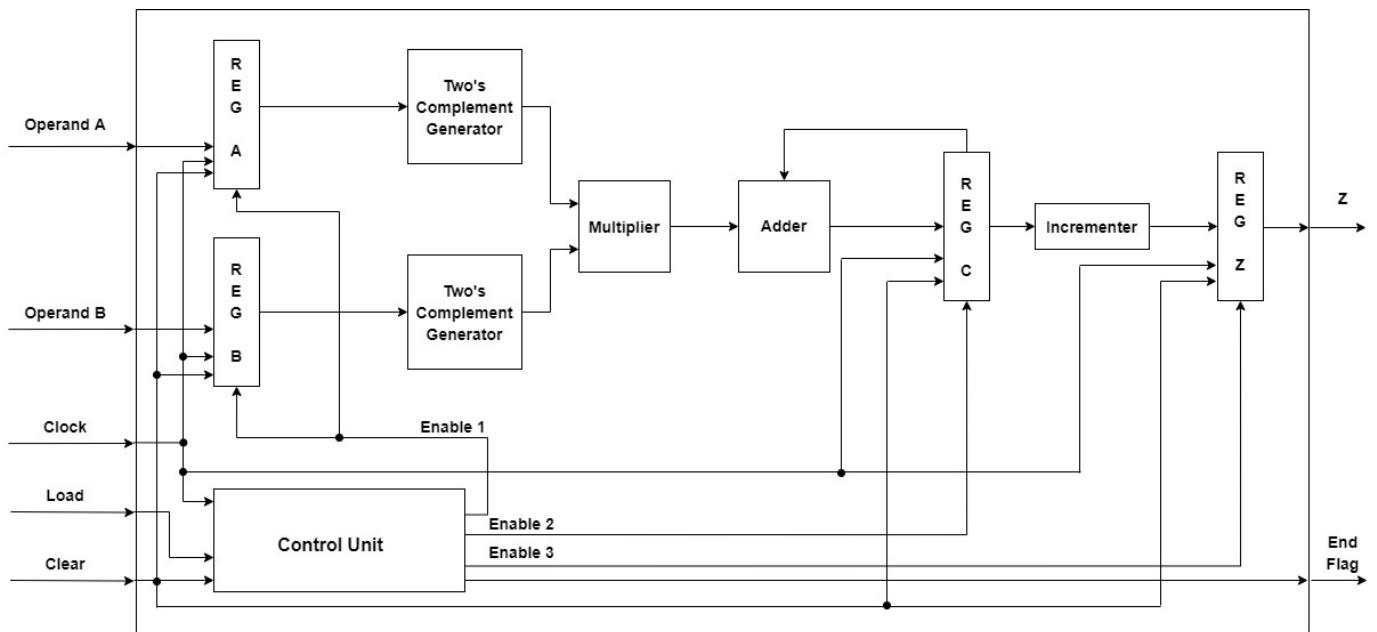


Figure 41 16-bit ALU with Accumulator Block Diagram

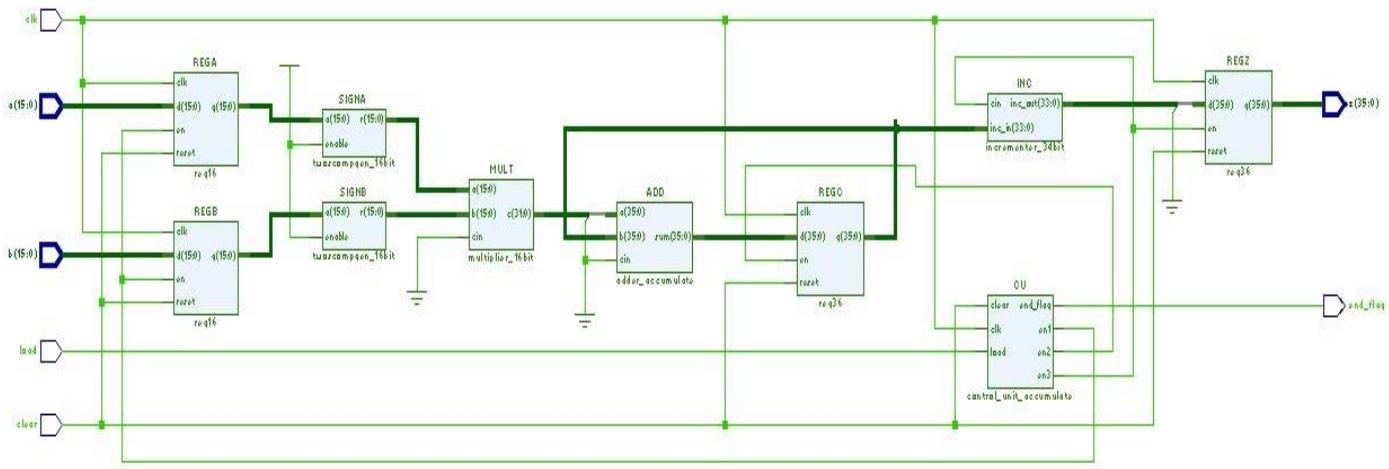


Figure 42 RTL of 16-bit ALU with Accumulator

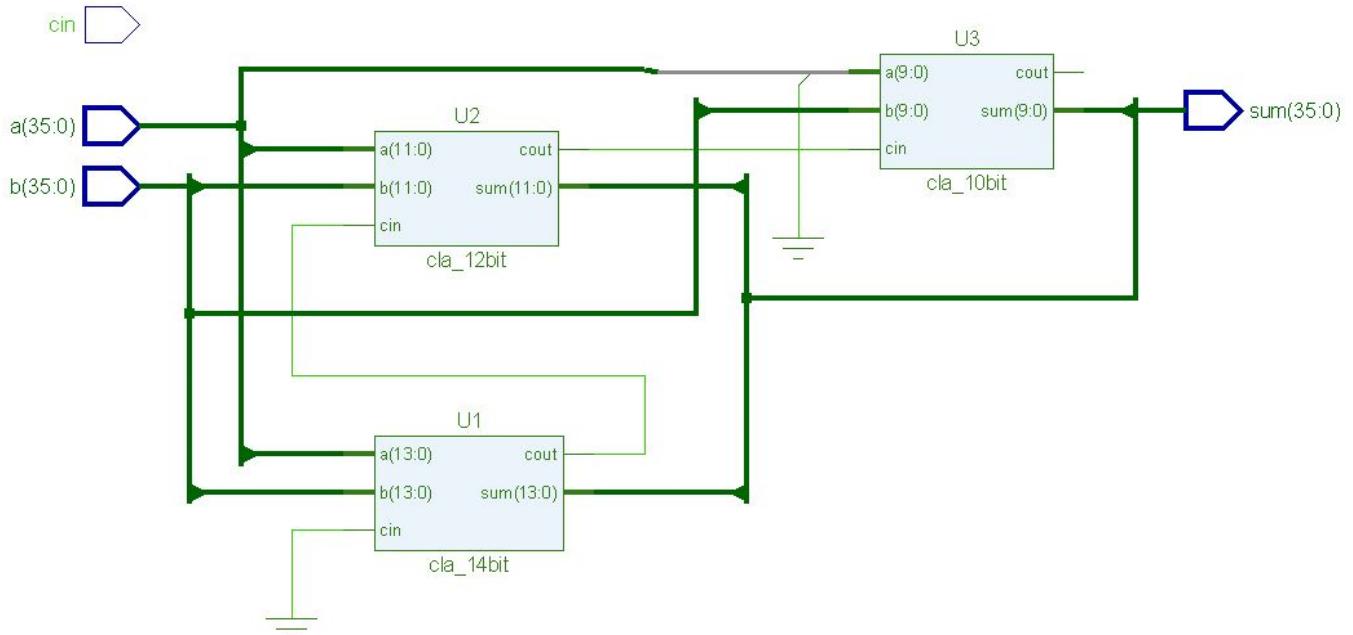


Figure 43 RTL of Accumulate Adder

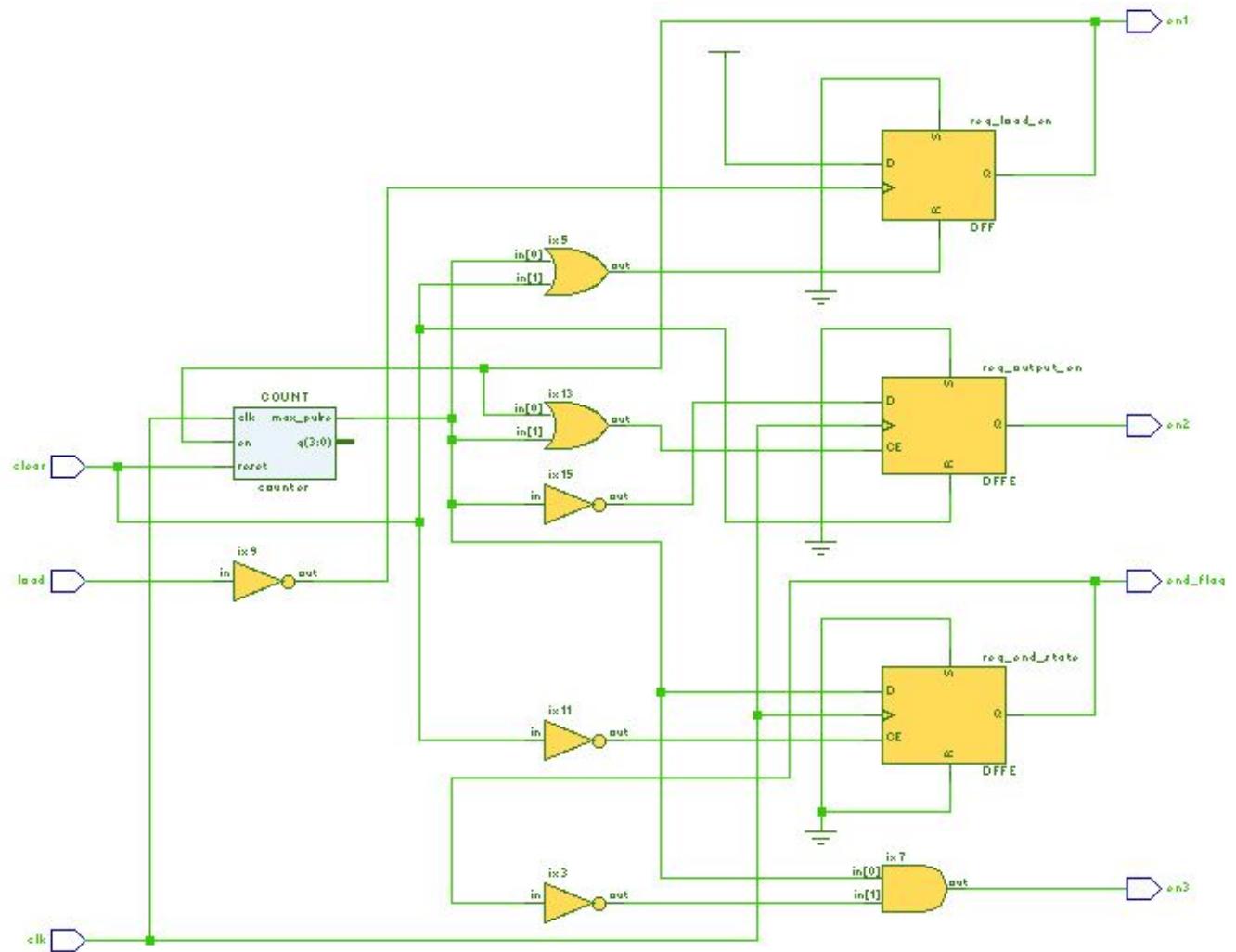


Figure 44 RTL of Control Unit for 16-bit ALU with Accumulator

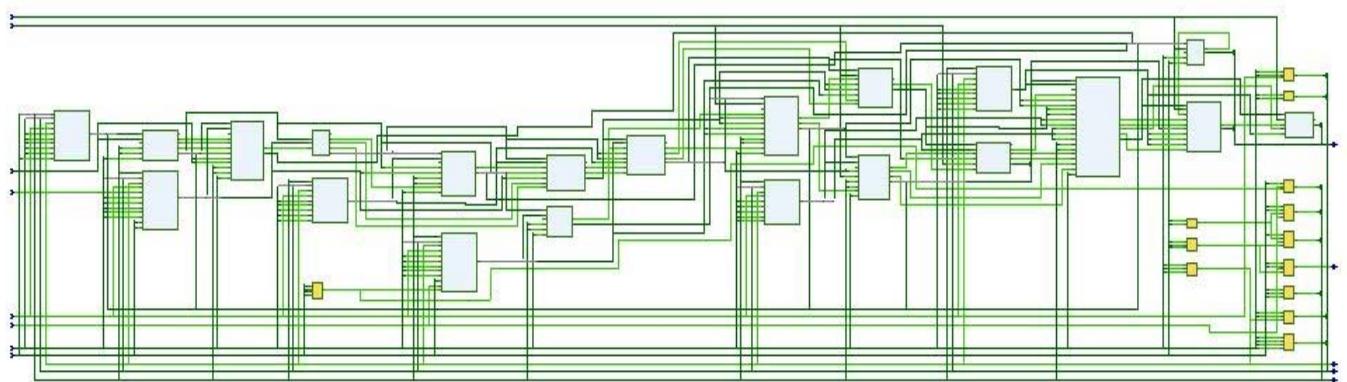


Figure 45 Tech schematic of 16-bit ALU with Accumulator

5.2 Test Results and Analysis

We simulated this version using 10 pairs of input operands. Therefore, the ALU will first add the products together at each clock cycle: $20245*-30220 + 22963*25039 + -7139*-7253 + 10993*355 + 374*480 + -18559*-18559 + -29357*0 + 7515*1 + -1708*24057 + -11378*-2707 = 353182745$. When max is reached, this value will be divide by 4 and incremented by 1: $353182745/4 + 1 = 88295687.25$. Therefore, the ALU gives the correct output of 88295687.



Figure 46 Simulation Waveforms of 16-bit ALU with Accumulator



Figure 47 Simulation Waveforms of 16-bit ALU with Accumulator with clear 1

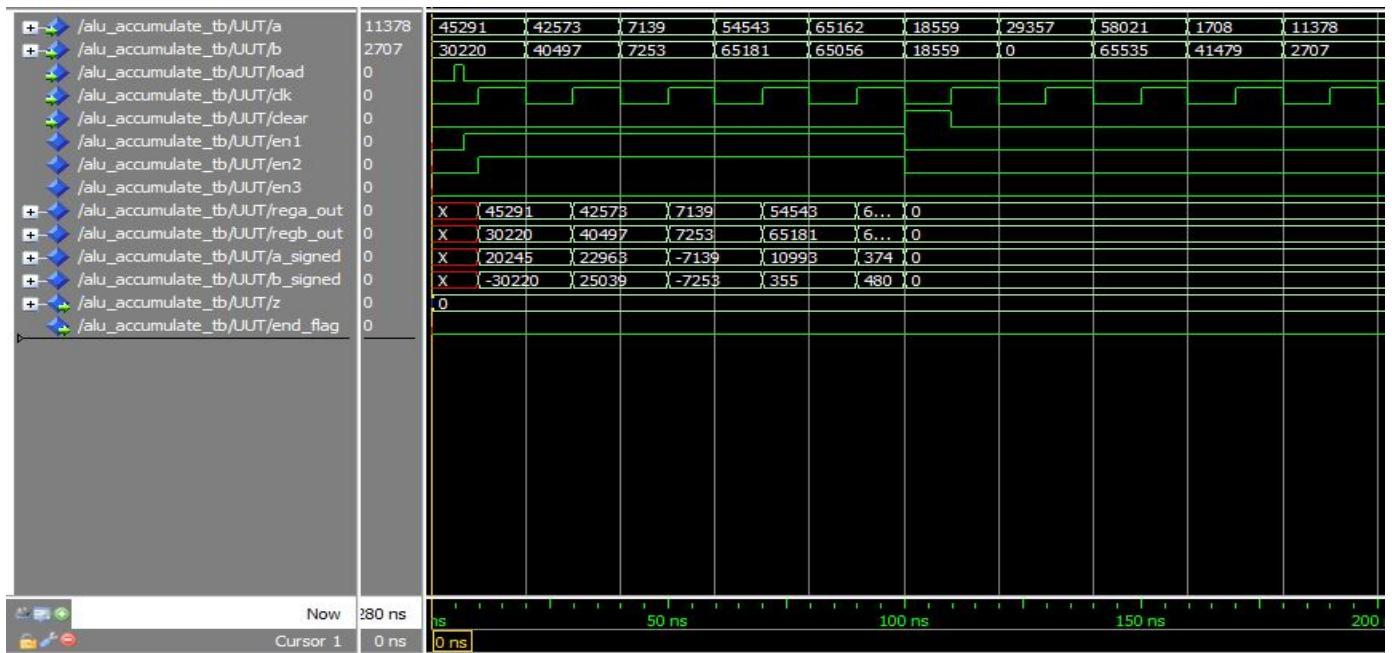


Figure 48 Simulation Waveforms of 16-bit ALU with Accumulator with clear 2

This version increases the area by 17.8 % in slices and increases the delay by 9.3 %.

Table 9 Area of the 16-bit ALU with and without Accumulator

	LUTs	CLB Slices	Dffs or Latches
16-bit ALU	886	443	64
16-bit ALU with Accumulator	1043	522	109

Table 10 Delay of the 16-bit ALU with and without Accumulator

	Delay
16-bit ALU	23.617 ns
16-bit ALU with Accumulator	25.823 ns

6 Conclusion

The ALU has proven to be the best and the most efficient when using the radix-4 booth multiplier along with CLA's. We've seen how it was able to enhance the performance by decreasing both the area and the delay. When expanding the design to 16 bits, both the area and the delay will increase significantly. Implementing pipelining will help in decreasing the total number of clock cycles of the operations. An accumulator can be added to the ALU in order to add the products of all the operations together.

References

- [1] Kaur and M. Manna, "Implementation of modified booth algorithm(radix 4) and its comparison with booth algorithm (radix-2),"Advance in Electronic and Electric Engineering ISSN 2231-1297, vol. 3, pp. 683–690, 09 2013.
- [2] "Fast Addition -- Carry Lookahead", *Fourier.eng.hmc.edu*, 2020. [Online]. Available: http://fourier.eng.hmc.edu/e85_old/lectures/arithmetic_html/node7.html.
- [3] P. Chu, *Register transfer level (RTL) hardware design using VHDL*. Hoboken, NJ: J. Wiley & Sons, 2006.

Appendix

ALU 8-bit (Radix-4 Booth Multiplier with CLA) Area Report

```
*****
Device Utilization for 2VP2fg256
*****
Resource           Used   Avail   Utilization
-----
IOs                  36    140    25.71%
Global Buffers       2     16    12.50%
LUTs                 204   2816    7.24%
CLB Slices           102   1408    7.24%
Dffs or Latches      32    3236    0.99%
Block RAMs            0     12    0.00%
Block Multipliers     0     12    0.00%
Block Multiplier Dffs 0     432    0.00%
GT_CUSTOM             0      4    0.00%
-----
```

```
*****
```

Library: work Cell: alu View: alu_arch

```
*****
```

Cell	Library	References	Total Area
BUFGP	xcv2p	2 x	
FDC	xcv2p	1 x	1 Dffs or Latches
FDCE	xcv2p	30 x	30 Dffs or Latches
FDC_1	xcv2p	1 x	1 Dffs or Latches
IBUF	xcv2p	17 x	
LUT1	xcv2p	1 x	1 LUTs
LUT2	xcv2p	9 x	9 LUTs
LUT3	xcv2p	10 x	10 LUTs
LUT4	xcv2p	28 x	28 LUTs
OBUF	xcv2p	17 x	
VCC	xcv2p	1 x	
cla_10bit	work	1 x	21 gates 21 LUTs
cla_12bit	work	1 x	28 gates 28 LUTs
cla_14bit	work	1 x	27 gates 27 LUTs 1 MUXF5
ppg	work	1 x	27 gates 27 LUTs
ppg_unfolded0	work	1 x	27 gates 27 LUTs

```
ppg_unfolded1      work      1 x      27      27 gates
                    27          27 LUTs
```

```
Number of ports :                      36
Number of nets :                       198
Number of instances :                  123
Number of references to this view :   0
```

```
Total accumulated area :
Number of Dffs or Latches :           32
Number of LUTs :                      204
Number of MUXF5 :                     1
Number of gates :                     206
Number of accumulated instances :     275
```

```
*****
```

IO Register Mapping Report

```
*****
```

```
Design: work.alu.alu_arch
```

Port	Direction	INFF	OUTFF	TRIFF
a(7)	Input			
a(6)	Input			
a(5)	Input			
a(4)	Input			
a(3)	Input			
a(2)	Input			
a(1)	Input			
a(0)	Input			
b(7)	Input			
b(6)	Input			
b(5)	Input			
b(4)	Input			
b(3)	Input			
b(2)	Input			

b(1)	Input				
b(0)	Input				
load	Input				
clk	Input				
clear	Input				
end_flag	Output				
z(15)	Output				
z(14)	Output				
z(13)	Output				
z(12)	Output				
z(11)	Output				
z(10)	Output				
z(9)	Output				
z(8)	Output				
z(7)	Output				
z(6)	Output				
z(5)	Output				
z(4)	Output				
z(3)	Output				
z(2)	Output				
z(1)	Output				
z(0)	Output				

Total registers mapped: 0

ALU 8-bit (Radix-4 Booth Multiplier with CLA) Timing Report

=====

=====

Clock Frequency Report

Domain Period (Freq)	Clock Name Required Period (Freq)	Min
-----	-----	---
-----	-----	-----
ClockDomain0 10.642 (93.967 MHz)	clk 20.000 (50.000 MHz)	
-- Device: Xilinx - VIRTEX-II Pro : 2VP2fg256 : 7		
-- CTE report summary..		
	CTE Report Summary	

End CTE Report Summary CPU Time Used: 0 sec.

-- POST-SYNTHESIS TIMING REPORTS ARE ESTIMATES AND SHOULD NOT BE RELIED ON TO MAKE QoR DECISIONS. For accurate timing information, please run place-and-route (P&R) and review P&R generated timing reports.

Setup Slack Path Summary

Data							
Data	Setup	Path	Source	Dest.			
End							
Index	Slack	Delay	Clock	Clock	Data Start	Pin	Data
End Pin		Edge					
-----	-----	-----	-----	-----	-----	-----	-----
1	9.358	10.468	clk	clk	REGA_reg_q_reg(0)/C		
REGZ_reg_q_reg(13)/D		Rise					
2	9.538	10.288	clk	clk	REGA_reg_q_reg(1)/C		
REGZ_reg_q_reg(13)/D		Rise					
3	9.628	10.198	clk	clk	REGB_reg_q_reg(0)/C		
REGZ_reg_q_reg(13)/D		Rise					
4	9.628	10.198	clk	clk	REGB_reg_q_reg(1)/C		
REGZ_reg_q_reg(13)/D		Rise					
5	9.638	10.188	clk	clk	REGA_reg_q_reg(2)/C		
REGZ_reg_q_reg(13)/D		Rise					
6	9.658	10.168	clk	clk	REGA_reg_q_reg(3)/C		
REGZ_reg_q_reg(13)/D		Rise					
7	10.162	9.664	clk	clk	REGB_reg_q_reg(2)/C		
REGZ_reg_q_reg(13)/D		Rise					
8	10.172	9.654	clk	clk	REGB_reg_q_reg(3)/C		
REGZ_reg_q_reg(13)/D		Rise					
9	10.222	9.604	clk	clk	REGA_reg_q_reg(4)/C		
REGZ_reg_q_reg(13)/D		Rise					
10	10.332	9.494	clk	clk	REGA_reg_q_reg(5)/C		
REGZ_reg_q_reg(13)/D		Rise					
-- Device: Xilinx - VIRTEX-II Pro : 2VP2fg256 : 7							
-- CTE report summary..							
	CTE Report Summary						

Analyzing setup constraint violations
End CTE Report Summary CPU Time Used: 0 sec.
-- POST-SYNTHESIS TIMING REPORTS ARE ESTIMATES AND SHOULD NOT BE
RELIED ON TO MAKE QoR DECISIONS. For accurate timing information,
please run place-and-route (P&R) and review P&R generated timing
reports.
-- Device: Xilinx - VIRTEX-II Pro : 2VP2fg256 : 7
-- CTE report timing..
CTE Path Report

Critical path #1, (path slack = 9.358):

SOURCE CLOCK: name: clk period: 20.000000
Times are relative to the 1st rising edge
DEST CLOCK: name: clk period: 20.000000
Times are relative to the 2nd rising edge

NAME	GATE	DELAY	ARRIVAL	DIR	FANOUT
REGA_reg_q_reg(0)/C	FDCE		0.000	up	
REGA_reg_q_reg(0)/Q	FDCE	0.370	0.370	up	
rega_out(0)	(net)	0.600			31
ix49392z1315/I3	LUT4		0.970	up	
ix49392z1315/O	LUT4	0.264	1.234	up	
NOT_SIGNAL_U2_cout_temp(4)	(net)	0.420			16
ix49392z28355/I0	LUT4		1.654	up	
ix49392z28355/O	LUT4	0.264	1.918	up	
MULT_PP0_U2_a_temp(4)	(net)	0.290			3
ix49392z1509/I0	LUT3		2.208	up	
ix49392z1509/O	LUT3	0.264	2.472	up	
MULT_PP0_twoscompgen_out(4)	(net)	0.280			2
ix49392z64837/I3	LUT4		2.752	up	
ix49392z64837/O	LUT4	0.264	3.016	up	
MULT_ppg0_out(4)	(net)	0.290			3
MULT_A1_U1/ix61094z1335/I0	LUT2		3.306	up	
MULT_A1_U1/ix61094z1335/O	LUT2	0.264	3.570	up	
MULT_A1_U1/nx61094z4	(net)	0.280			1
MULT_A1_U1/ix61094z60711/I3	LUT4		3.850	up	
MULT_A1_U1/ix61094z60711/O	LUT4	0.264	4.114	up	
MULT_A1_U1/nx61094z3	(net)	0.280			2
MULT_A1_U1/ix61094z62478/I2	LUT4		4.394	up	
MULT_A1_U1/ix61094z62478/O	LUT4	0.264	4.658	up	
MULT_A1_U1/c(4)	(net)	0.290			3
MULT_A1_U1/ix61094z1549/I2	LUT3		4.948	up	
MULT_A1_U1/ix61094z1549/O	LUT3	0.264	5.212	up	
MULT_A1_U1/c(5)	(net)	0.300			5
MULT_A1_U2/ix63088z61671/I1	LUT4		5.512	up	
MULT_A1_U2/ix63088z61671/O	LUT4	0.264	5.776	up	
MULT_A1_U2/nx63088z3	(net)	0.280			1
MULT_A1_U2/ix63088z60711/I3	LUT4		6.056	up	
MULT_A1_U2/ix63088z60711/O	LUT4	0.264	6.320	up	
MULT_A1_U2/nx63088z2	(net)	0.280			2

MULT_A1_U2/ix63088z62478/I2	LUT4		6.600	up
MULT_A1_U2/ix63088z62478/O	LUT4	0.264	6.864	up
MULT_A1_U2/c(5)	(net)	0.300		5
MULT_A1_U2/ix63088z60709/I2	LUT4		7.164	up
MULT_A1_U2/ix63088z60709/O	LUT4	0.264	7.428	up
MULT_A1_U2/nx63088z1	(net)	0.280		2
MULT_A1_U2/ix63088z62476/I2	LUT4		7.708	up
MULT_A1_U2/ix63088z62476/O	LUT4	0.264	7.972	up
MULT_A1_U2/c(8)	(net)	0.320		6
MULT_A1_U3/ix17797z61672/I1	LUT4		8.292	up
MULT_A1_U3/ix17797z61672/O	LUT4	0.264	8.556	up
MULT_A1_U3/nx17797z5	(net)	0.280		1
MULT_A1_U3/ix17797z60708/I3	LUT4		8.836	up
MULT_A1_U3/ix17797z60708/O	LUT4	0.264	9.100	up
MULT_A1_U3/nx17797z1	(net)	0.280		2
MULT_A1_U3/ix17797z62475/I2	LUT4		9.380	up
MULT_A1_U3/ix17797z62475/O	LUT4	0.264	9.644	up
MULT_A1_U3/c(8)	(net)	0.280		2
MULT_A1_U3/ix17797z43964/I3	LUT4		9.924	up
MULT_A1_U3/ix17797z43964/O	LUT4	0.264	10.188	up
MULT_A1_U3/sum(9)	(net)	0.280		1
REGZ_reg_q_reg(13)/D	FDCE		10.468	up
 Initial edge separation: 20.000				
Source clock delay: - 1.359				
Dest clock delay: + 1.359				

Edge separation: 20.000				
Setup constraint: - 0.174				

Data required time: 19.826				
Data arrival time: - 10.468 (46.41% cell delay,				
53.59% net delay)				

Slack: 9.358				

End CTE Analysis CPU Time Used: 0 sec.

ALU 8-bit (Radix-2 Booth Multiplier with CLA) Area Report

```
*****
Device Utilization for 2VP2fg256
*****
Resource          Used      Avail   Utilization
-----
IOs                36       140    25.71%
Global Buffers     2        16     12.50%
```

LUTs	348	2816	12.36%
CLB Slices	174	1408	12.36%
Dffs or Latches	32	3236	0.99%
Block RAMs	0	12	0.00%
Block Multipliers	0	12	0.00%
Block Multiplier Dffs	0	432	0.00%
GT_CUSTOM	0	4	0.00%

Library: work Cell: alu_radix2 View: alu_radix2_arch

Cell	Library	References	Total Area
BUFGP	xcv2p	2 x	
FDC	xcv2p	1 x	1 Dffs or Latches
FDCE	xcv2p	30 x	30 Dffs or Latches
FDC_1	xcv2p	1 x	1 Dffs or Latches
IBUF	xcv2p	17 x	
LUT1	xcv2p	1 x	1 LUTs
LUT2	xcv2p	8 x	8 LUTs
LUT3	xcv2p	8 x	8 LUTs
LUT4	xcv2p	26 x	26 LUTs
OBUF	xcv2p	17 x	
VCC	xcv2p	1 x	
multiplier_radix2	work	1 x	5 MUXF5 306 LUTs 309 gates

Number of ports :	36
Number of nets :	154
Number of instances :	113
Number of references to this view :	0

Total accumulated area :	
Number of Dffs or Latches :	32
Number of LUTs :	348
Number of MUXF5 :	5
Number of gates :	354
Number of accumulated instances :	423

IO Register Mapping Report

Design: work.alu_radix2.alu_radix2_arch

Port	Direction	INFF	OUTFF	TRIFF
------	-----------	------	-------	-------

a(7)	Input			
a(6)	Input			
a(5)	Input			
a(4)	Input			
a(3)	Input			
a(2)	Input			
a(1)	Input			
a(0)	Input			
b(7)	Input			
b(6)	Input			
b(5)	Input			
b(4)	Input			
b(3)	Input			
b(2)	Input			
b(1)	Input			
b(0)	Input			
load	Input			
clk	Input			
clear	Input			
end_flag	Output			
z(15)	Output			
z(14)	Output			
z(13)	Output			
z(12)	Output			
z(11)	Output			
z(10)	Output			

z(9)	Output			
z(8)	Output			
z(7)	Output			
z(6)	Output			
z(5)	Output			
z(4)	Output			
z(3)	Output			
z(2)	Output			
z(1)	Output			
z(0)	Output			

Total registers mapped: 0

ALU 8-bit (Radix-2 Booth Multiplier with CLA) Timing Report

```
=====
=====
          Clock Frequency Report
```

Domain Period (Freq)	Clock Name Required Period (Freq)	Min
-----	-----	---
ClockDomain0 15.774 (63.395 MHz)	clk 20.000 (50.000 MHz)	

```
=====
=====
      Setup Timing Analysis of clk
```

Setup Slack Path Summary

Data End Index Pin	Data						Data End
	Setup	Path	Source	Dest.	Clock	Clock	
	Slack	Delay			Data Start	Pin	
	Edge						

1	4.226	15.600	clk	clk	REGA_reg_q_reg(0)/C
REGZ_reg_q_reg(13)/D		Rise			
2	4.486	15.340	clk	clk	REGA_reg_q_reg(1)/C
REGZ_reg_q_reg(13)/D		Rise			
3	4.586	15.240	clk	clk	REGA_reg_q_reg(2)/C
REGZ_reg_q_reg(13)/D		Rise			
4	4.626	15.200	clk	clk	REGA_reg_q_reg(3)/C
REGZ_reg_q_reg(13)/D		Rise			
5	4.660	15.166	clk	clk	REGB_reg_q_reg(0)/C
REGZ_reg_q_reg(13)/D		Rise			
6	5.030	14.796	clk	clk	REGB_reg_q_reg(1)/C
REGZ_reg_q_reg(13)/D		Rise			
7	5.334	14.492	clk	clk	REGA_reg_q_reg(4)/C
REGZ_reg_q_reg(13)/D		Rise			
8	5.504	14.322	clk	clk	REGA_reg_q_reg(5)/C
REGZ_reg_q_reg(13)/D		Rise			
9	6.028	13.798	clk	clk	REGA_reg_q_reg(6)/C
REGZ_reg_q_reg(13)/D		Rise			
10	6.248	13.578	clk	clk	REGB_reg_q_reg(2)/C
REGZ_reg_q_reg(13)/D		Rise			

CTE Path Report

Critical path #1, (path slack = 4.226):

```
SOURCE CLOCK: name: clk period: 20.000000
    Times are relative to the 1st rising edge
DEST CLOCK: name: clk period: 20.000000
    Times are relative to the 2nd rising edge
```

NAME	GATE	DELAY	ARRIVAL	DIR	FANOUT
REGA_reg_q_reg(0)/C	FDCE		0.000	up	
REGA_reg_q_reg(0)/Q	FDCE	0.370	0.370	up	
rega_out(0)	(net)	0.680			41
ix33258z23166/I3	LUT4		1.050	up	
ix33258z23166/O	LUT4	0.264	1.314	up	
a_signed(3)	(net)	0.420			16
MULT/ix12673z1344/I0	LUT2		1.734	up	
MULT/ix12673z1344/O	LUT2	0.264	1.998	up	
MULT/PP1_U2_a_temp(3)	(net)	0.280			1
MULT/ix12673z36190/I1	LUT4		2.278	up	
MULT/ix12673z36190/O	LUT4	0.264	2.542	up	
MULT/nx12673z13	(net)	0.290			3
MULT/A1_U1/ix60097z50129/I0	LUT4		2.832	up	
MULT/A1_U1/ix60097z50129/O	LUT4	0.264	3.096	up	
MULT/A1_U1/nx60097z2	(net)	0.280			1
MULT/A1_U1/ix60097z60709/I3	LUT4		3.376	up	
MULT/A1_U1/ix60097z60709/O	LUT4	0.264	3.640	up	
MULT/A1_U1/nx60097z1	(net)	0.280			2

MULT/A1_U1/ix60097z62476/I2	LUT4		3.920	up	
MULT/A1_U1/ix60097z62476/O	LUT4	0.264	4.184	up	
MULT/A1_U1/c(5)	(net)	0.290			3
MULT/A1_U1/ix60097z1547/I2	LUT3		4.474	up	
MULT/A1_U1/ix60097z1547/O	LUT3	0.264	4.738	up	
MULT/A1_U1/c(6)	(net)	0.290			3
MULT/A1_U1/ix19791z41448/I3	LUT4		5.028	up	
MULT/A1_U1/ix19791z41448/O	LUT4	0.264	5.292	up	
MULT/A1_U1/sum(7)	(net)	0.320			7
MULT/A1_U2/ix61094z1340/I0	LUT2		5.612	up	
MULT/A1_U2/ix61094z1340/O	LUT2	0.264	5.876	up	
MULT/A1_U2/nx61094z7	(net)	0.280			1
MULT/A1_U2/ix61094z60717/I3	LUT4		6.156	up	
MULT/A1_U2/ix61094z60717/O	LUT4	0.264	6.420	up	
MULT/A1_U2/nx61094z6	(net)	0.290			3
MULT/A1_U2/ix61094z1492/I1	LUT3		6.710	up	
MULT/A1_U2/ix61094z1492/O	LUT3	0.264	6.974	up	
MULT/A1_U2/nx61094z5	(net)	0.290			3
MULT/A1_U2/ix64085z1187/I3	LUT4		7.264	up	
MULT/A1_U2/ix64085z1187/O	LUT4	0.264	7.528	up	
MULT/A1_U2/c(9)	(net)	0.290			3
MULT/A1_U2/ix64085z43964/I3	LUT4		7.818	up	
MULT/A1_U2/ix64085z43964/O	LUT4	0.264	8.082	up	
MULT/A1_U2/sum(10)	(net)	0.290			4
MULT/A1_U3/ix62091z1052/I0	LUT4		8.372	up	
MULT/A1_U3/ix62091z1052/O	LUT4	0.264	8.636	up	
MULT/A1_U3/nx62091z7	(net)	0.280			2
MULT/A1_U3/ix63088z1485/I2	LUT3		8.916	up	
MULT/A1_U3/ix63088z1485/O	LUT3	0.264	9.180	up	
MULT/A1_U3/nx63088z1	(net)	0.280			2
MULT/A1_U3/ix63088z1187/I3	LUT4		9.460	up	
MULT/A1_U3/ix63088z1187/O	LUT4	0.264	9.724	up	
MULT/A1_U3/c(10)	(net)	0.280			1
MULT/A1_U3/ix63088z43964/I3	LUT4		10.004	up	
MULT/A1_U3/ix63088z43964/O	LUT4	0.264	10.268	up	
MULT/A1_U3/sum(11)	(net)	0.290			3
MULT/A1_U4/ix63088z1340/I0	LUT2		10.558	up	
MULT/A1_U4/ix63088z1340/O	LUT2	0.264	10.822	up	
MULT/A1_U4/nx63088z7	(net)	0.280			1
MULT/A1_U4/ix63088z45012/I3	LUT4		11.102	up	
MULT/A1_U4/ix63088z45012/O	LUT4	0.264	11.366	up	
MULT/A1_U4/nx63088z4	(net)	0.280			1
MULT/A1_U4/ix63088z55178/I1	MUXF5		11.646	up	
MULT/A1_U4/ix63088z55178/O	MUXF5	0.337	11.983	up	
MULT/A1_U4/sum(11)	(net)	0.280			2
MULT/A1_U5/ix64085z28621/I0	LUT4		12.263	up	
MULT/A1_U5/ix64085z28621/O	LUT4	0.264	12.527	up	
MULT/A1_U5/nx64085z1	(net)	0.280			1
MULT/A1_U5/ix64085z55178/I0	MUXF5		12.807	up	
MULT/A1_U5/ix64085z55178/O	MUXF5	0.337	13.144	up	
MULT/A1_U5/sum(10)	(net)	0.280			1
MULT/A1_U6/ix17797z1328/I0	LUT2		13.424	up	

MULT/A1_U6/ix17797z1328/O	LUT2	0.264	13.688	up	
MULT/A1_U6/nx17797z5	(net)	0.280			1
MULT/A1_U6/ix17797z15198/I1	LUT4		13.968	up	
MULT/A1_U6/ix17797z15198/O	LUT4	0.264	14.232	up	
MULT/A1_U6/sum(9)	(net)	0.280			1
MULT/ix7382z29163/I1	LUT4		14.512	up	
MULT/ix7382z29163/O	LUT4	0.264	14.776	up	
MULT/c(15)	(net)	0.280			1
ix63131z45003/I0	LUT4		15.056	up	
ix63131z45003/O	LUT4	0.264	15.320	up	
z_temp(15)	(net)	0.280			1
REGZ_reg_q_reg(13)/D	FDCE		15.600	up	
Initial edge separation: 20.000					
Source clock delay: - 1.359					
Dest clock delay: + 1.359					

Edge separation: 20.000					
Setup constraint: - 0.174					

Data required time: 19.826					
Data arrival time: - 15.600 (47.31% cell delay,					
52.69% net delay)					

Slack: 4.226					

=====

=====

Input Delay Report

Input Slack (ns)	Clock Name	
-----	-----	-----
-----	-----	-----

No input delay constraints.

=====

=====

Output Delay Report

Output Slack (ns)	Clock Name	
-----	-----	-----
-----	-----	-----

No output delay constraints.

ALU 8-bit (Regular Multiplier with RCA) Area Report

```
*****
Device Utilization for 2VP2fg256
*****
Resource           Used   Avail   Utilization
-----
IOS                36     140    25.71%
Global Buffers      2      16    12.50%
LUTs               301    2816   10.69%
CLB Slices          151    1408   10.72%
Dffs or Latches     32     3236   0.99%
Block RAMs          0      12    0.00%
Block Multipliers    0      12    0.00%
Block Multiplier Dffs 0      432    0.00%
GT_CUSTOM           0      4     0.00%
-----
```

```
*****
Library: work      Cell: alu_regular      View: alu_regular_arch
*****
```

Cell	Library	References	Total Area
BUFGP	xcv2p	2 x	
FDC	xcv2p	1 x	1 Dffs or Latches
FDCE	xcv2p	30 x	30 Dffs or Latches
FDC_1	xcv2p	1 x	1 Dffs or Latches
IBUF	xcv2p	17 x	
LUT1	xcv2p	1 x	1 LUTs
LUT2	xcv2p	8 x	8 LUTs
LUT3	xcv2p	11 x	11 LUTs
LUT4	xcv2p	23 x	23 LUTs
OBUF	xcv2p	17 x	
VCC	xcv2p	1 x	
multiplier_regular	work	1 x	265 gates 259 LUTs 1 MUXF5

Number of ports :	36
Number of nets :	149
Number of instances :	113
Number of references to this view :	0

Total accumulated area :	
Number of Dffs or Latches :	32
Number of LUTs :	301
Number of MUXF5 :	1
Number of gates :	310
Number of accumulated instances :	372

```
*****
IO Register Mapping Report
*****
Design: work.alu_regular.alu_regular_arch
```

Port	Direction	INFF	OUTFF	TRIFF
a(7)	Input			
a(6)	Input			
a(5)	Input			
a(4)	Input			
a(3)	Input			
a(2)	Input			
a(1)	Input			
a(0)	Input			
b(7)	Input			
b(6)	Input			
b(5)	Input			
b(4)	Input			
b(3)	Input			
b(2)	Input			
b(1)	Input			
b(0)	Input			
load	Input			
clk	Input			
clear	Input			
end_flag	Output			
z(15)	Output			

z(14)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(13)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(12)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(11)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(10)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(9)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(8)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(7)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(6)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(5)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(4)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(3)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(2)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(1)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(0)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+

Total registers mapped: 0

ALU 8-bit (Regular Multiplier with RCA) Timing Report

```
=====
=====
          Clock Frequency Report
```

Domain Period (Freq)	Clock Name Required Period (Freq)	Min
----------------------	-----------------------------------	-----

```

-----
----- -----
ClockDomain0      clk
16.786 (59.573 MHz) 20.000 (50.000 MHz)

```

```

=====
=====
Setup Timing Analysis of clk
```

Setup Slack Path Summary

Data							
Data	Setup	Path	Source	Dest.			
End							
Index	Slack	Delay	Clock	Clock	Data Start Pin		Data End
Pin	Edge						
1	3.214	16.612	clk	clk	REGA_reg_q_reg(0)/C		
REGZ_reg_q_reg(13)/D		Rise					
2	3.394	16.432	clk	clk	REGB_reg_q_reg(0)/C		
REGZ_reg_q_reg(13)/D		Rise					
3	3.474	16.352	clk	clk	REGA_reg_q_reg(1)/C		
REGZ_reg_q_reg(13)/D		Rise					
4	3.554	16.272	clk	clk	REGB_reg_q_reg(1)/C		
REGZ_reg_q_reg(13)/D		Rise					
5	3.554	16.272	clk	clk	REGA_reg_q_reg(2)/C		
REGZ_reg_q_reg(13)/D		Rise					
6	3.958	15.868	clk	clk	REGA_reg_q_reg(3)/C		
REGZ_reg_q_reg(13)/D		Rise					
7	4.502	15.324	clk	clk	REGA_reg_q_reg(4)/C		
REGZ_reg_q_reg(13)/D		Rise					
8	4.742	15.084	clk	clk	REGB_reg_q_reg(2)/C		
REGZ_reg_q_reg(13)/D		Rise					
9	5.066	14.760	clk	clk	REGA_reg_q_reg(5)/C		
REGZ_reg_q_reg(13)/D		Rise					
10	5.256	14.570	clk	clk	REGB_reg_q_reg(3)/C		
REGZ_reg_q_reg(13)/D		Rise					

CTE Path Report

Critical path #1, (path slack = 3.214):

```

SOURCE CLOCK: name: clk period: 20.000000
    Times are relative to the 1st rising edge
DEST CLOCK: name: clk period: 20.000000
    Times are relative to the 2nd rising edge

```

NAME	GATE	DELAY	ARRIVAL DIR	FANOUT
------	------	-------	-------------	--------

REGA_reg_q_reg(0)/C	FDCE		0.000	up	
REGA_reg_q_reg(0)/Q	FDCE	0.370	0.370	up	
rega_out(0)	(net)	0.640			35
ix33258z1407/I2	LUT3		1.010	up	
ix33258z1407/O	LUT3	0.264	1.274	up	
a_signed(2)	(net)	0.440			20
MULT/ix7382z1127/I0	LUT4		1.714	up	
MULT/ix7382z1127/O	LUT4	0.264	1.978	dn	
MULT/NOT_c1(2)	(net)	0.280			2
MULT/ix7382z3578/I3	LUT4		2.258	dn	
MULT/ix7382z3578/O	LUT4	0.264	2.522	up	
MULT/c1(3)	(net)	0.290			3
MULT/ix7382z46174/I3	LUT4		2.812	up	
MULT/ix7382z46174/O	LUT4	0.264	3.076	up	
MULT/c1(4)	(net)	0.280			2
MULT/ix7382z1485/I2	LUT3		3.356	up	
MULT/ix7382z1485/O	LUT3	0.264	3.620	up	
MULT/nx7382z4	(net)	0.290			3
MULT/ix7382z43973/I0	LUT4		3.910	up	
MULT/ix7382z43973/O	LUT4	0.264	4.174	up	
MULT/sum1_temp(3)	(net)	0.280			1
MULT/ix7382z65498/I2	LUT4		4.454	up	
MULT/ix7382z65498/O	LUT4	0.264	4.718	up	
MULT/c2(4)	(net)	0.290			4
MULT/ix7382z36062/I3	LUT4		5.008	up	
MULT/ix7382z36062/O	LUT4	0.264	5.272	up	
MULT/sum2_temp(3)	(net)	0.280			1
MULT/ix7382z65509/I2	LUT4		5.552	up	
MULT/ix7382z65509/O	LUT4	0.264	5.816	up	
MULT/c3(4)	(net)	0.290			4
MULT/ix7382z65527/I3	LUT4		6.106	up	
MULT/ix7382z65527/O	LUT4	0.264	6.370	up	
MULT/c3(5)	(net)	0.320			8
MULT/ix7382z36098/I3	LUT4		6.690	up	
MULT/ix7382z36098/O	LUT4	0.264	6.954	up	
MULT/sum3_temp(4)	(net)	0.280			1
MULT/ix7382z65545/I2	LUT4		7.234	up	
MULT/ix7382z65545/O	LUT4	0.264	7.498	up	
MULT/c4(5)	(net)	0.300			5
MULT/ix7382z36118/I3	LUT4		7.798	up	
MULT/ix7382z36118/O	LUT4	0.264	8.062	up	
MULT/sum4_temp(4)	(net)	0.280			1
MULT/ix7382z65565/I2	LUT4		8.342	up	
MULT/ix7382z65565/O	LUT4	0.264	8.606	up	
MULT/c5(5)	(net)	0.300			5
MULT/ix7382z36144/I3	LUT4		8.906	up	
MULT/ix7382z36144/O	LUT4	0.264	9.170	up	
MULT/sum5_temp(4)	(net)	0.280			1
MULT/ix7382z65591/I2	LUT4		9.450	up	
MULT/ix7382z65591/O	LUT4	0.264	9.714	up	
MULT/c6(5)	(net)	0.300			5
MULT/ix7382z36165/I3	LUT4		10.014	up	

MULT/ix7382z36165/O	LUT4	0.264	10.278	up	
MULT/sum6_temp(4)	(net)	0.280			1
MULT/ix7382z65612/I2	LUT4		10.558	up	
MULT/ix7382z65612/O	LUT4	0.264	10.822	up	
MULT/c7(5)	(net)	0.300			5
MULT/ix7382z36185/I3	LUT4		11.122	up	
MULT/ix7382z36185/O	LUT4	0.264	11.386	up	
MULT/sum7_temp(4)	(net)	0.280			1
MULT/ix7382z65632/I2	LUT4		11.666	up	
MULT/ix7382z65632/O	LUT4	0.264	11.930	up	
MULT/c8(5)	(net)	0.300			5
MULT/ix7382z36204/I3	LUT4		12.230	up	
MULT/ix7382z36204/O	LUT4	0.264	12.494	up	
MULT/sum8_temp(4)	(net)	0.280			1
MULT/ix7382z65651/I2	LUT4		12.774	up	
MULT/ix7382z65651/O	LUT4	0.264	13.038	up	
MULT/c9(5)	(net)	0.300			5
MULT/ix7382z28552/I0	LUT4		13.338	up	
MULT/ix7382z28552/O	LUT4	0.264	13.602	up	
MULT/nx7382z47	(net)	0.280			1
MULT/ix7382z28349/I3	LUT4		13.882	up	
MULT/ix7382z28349/O	LUT4	0.264	14.146	up	
MULT/sum12_temp(1)	(net)	0.290			3
MULT/ix7382z39882/I2	LUT4		14.436	up	
MULT/ix7382z39882/O	LUT4	0.264	14.700	up	
MULT/sum13_temp(0)	(net)	0.280			1
MULT/ix7382z20695/I1	LUT4		14.980	up	
MULT/ix7382z20695/O	LUT4	0.264	15.244	up	
MULT/nx7382z1	(net)	0.280			1
MULT/ix7382z28344/I0	LUT4		15.524	up	
MULT/ix7382z28344/O	LUT4	0.264	15.788	up	
MULT/c(15)	(net)	0.280			1
ix63131z45003/I0	LUT4		16.068	up	
ix63131z45003/O	LUT4	0.264	16.332	up	
z_temp(15)	(net)	0.280			1
REGZ_reg_q_reg(13)/D	FDCE		16.612	up	

Initial edge separation:	20.000
Source clock delay:	- 1.359
Dest clock delay:	+ 1.359

Edge separation:	20.000
Setup constraint:	- 0.174

Data required time:	19.826
Data arrival time:	- 16.612 (46.73% cell delay,
53.27% net delay)	

Slack:	3.214

Input Delay Report

Input	Clock Name
Slack (ns)	-----
-----	-----
-----	-----

No input delay constraints.

Output Delay Report

Output Slack (ns)	Clock Name
-----	-----
-----	No output delay constraints.

ALU 16-bit (Radix-4 Booth Multiplier with CLA) Area Report

Resource	Used	Avail	Utilization
<hr/>			
IOs	68	140	48.57%
Global Buffers	2	16	12.50%
LUTs	886	2816	31.46%
CLB Slices	443	1408	31.46%
Dffs or Latches	64	3236	1.98%
Block RAMs	0	12	0.00%
Block Multipliers	0	12	0.00%
Block Multiplier Dffs	0	432	0.00%
GT_CUSTOM	0	4	0.00%
<hr/>			

Library: work Cell: alu 16bit View: alu 16bit arch

Cell	Library	References	Total Area
BUFGP	xcv2p	2 x	
FDC	xcv2p	1 x	1 Dffs or Latches

FDCE	xcv2p	62 x	1	62 Dffs or Latches
FDC_1	xcv2p	1 x	1	1 Dffs or Latches
IBUF	xcv2p	33 x		
LUT1	xcv2p	1 x	1	1 LUTs
LUT2	xcv2p	8 x	1	8 LUTs
LUT3	xcv2p	18 x	1	18 LUTs
LUT4	xcv2p	28 x	1	28 LUTs
OBUF	xcv2p	33 x		
VCC	xcv2p	1 x		
cla_10bit	work	1 x	23	23 gates
			23	23 LUTs
			1	1 MUXF5
cla_10bit_unfolded0	work	1 x	22	22 gates
			22	22 LUTs
cla_10bit_unfolded1	work	1 x	26	26 gates
			26	26 LUTs
			1	1 MUXF5
cla_12bit	work	1 x	35	35 gates
			35	35 LUTs
			3	3 MUXF5
cla_12bit_unfolded0	work	1 x	26	26 gates
			26	26 LUTs
cla_12bit_unfolded1	work	1 x	31	31 gates
			31	31 LUTs
			2	2 MUXF5
cla_12bit_unfolded2	work	1 x	26	26 gates
			26	26 LUTs
cla_14bit	work	1 x	31	31 gates
			31	31 LUTs
cla_14bit_unfolded0	work	1 x	43	43 gates
			42	42 LUTs
			4	4 MUXF5
cla_14bit_unfolded1	work	1 x	31	31 gates
			31	31 LUTs
cla_18bit	work	1 x	44	44 gates
			44	44 LUTs
cla_30bit	work	1 x	46	46 gates
			43	43 LUTs
			1	1 MUXF5
ppg_16bit	work	1 x	53	53 gates
			53	53 LUTs
ppg_16bit_unfolded0	work	1 x	57	57 gates
			57	57 LUTs
ppg_16bit_unfolded1	work	1 x	57	57 gates
			57	57 LUTs
ppg_16bit_unfolded2	work	1 x	57	57 gates
			57	57 LUTs
ppg_16bit_unfolded3	work	1 x	57	57 gates
			57	57 LUTs
ppg_16bit_unfolded4	work	1 x	57	57 gates
			57	57 LUTs
ppg_16bit_unfolded5	work	1 x	57	57 gates

ppg_16bit_unfolded6	work	1 x	57	57 LUTs
			57	57 gates
			57	57 LUTs

Number of ports :	68
Number of nets :	534
Number of instances :	208
Number of references to this view :	0

Total accumulated area :

Number of Dffs or Latches :	64
Number of LUTs :	886
Number of MUXF5 :	12
Number of gates :	892
Number of accumulated instances :	1032

IO Register Mapping Report

Design: work.alu_16bit.alu_16bit_arch

Port	Direction	INFF	OUTFF	TRIFF
a(15)	Input			
a(14)	Input			
a(13)	Input			
a(12)	Input			
a(11)	Input			
a(10)	Input			
a(9)	Input			
a(8)	Input			
a(7)	Input			
a(6)	Input			
a(5)	Input			
a(4)	Input			
a(3)	Input			
a(2)	Input			

a(1)	Input			
a(0)	Input			
b(15)	Input			
b(14)	Input			
b(13)	Input			
b(12)	Input			
b(11)	Input			
b(10)	Input			
b(9)	Input			
b(8)	Input			
b(7)	Input			
b(6)	Input			
b(5)	Input			
b(4)	Input			
b(3)	Input			
b(2)	Input			
b(1)	Input			
b(0)	Input			
load	Input			
clk	Input			
clear	Input			
end_flag	Output			
z(31)	Output			
z(30)	Output			
z(29)	Output			
z(28)	Output			

z(27)	Output			
z(26)	Output			
z(25)	Output			
z(24)	Output			
z(23)	Output			
z(22)	Output			
z(21)	Output			
z(20)	Output			
z(19)	Output			
z(18)	Output			
z(17)	Output			
z(16)	Output			
z(15)	Output			
z(14)	Output			
z(13)	Output			
z(12)	Output			
z(11)	Output			
z(10)	Output			
z(9)	Output			
z(8)	Output			
z(7)	Output			
z(6)	Output			
z(5)	Output			
z(4)	Output			
z(3)	Output			
z(2)	Output			

```

+-----+-----+-----+-----+
| z(1) | Output |       |       |
+-----+-----+-----+-----+
| z(0) | Output |       |       |
+-----+-----+-----+-----+
Total registers mapped: 0

```

ALU 16-bit (Radix-4 Booth Multiplier with CLA) Timing Report

```
=====
=====
```

Clock Frequency Report

Domain Period (Freq)	Clock Name Required Period (Freq)	Min
-----	-----	---
ClockDomain0 23.617 (42.342 MHz)	clk 20.000 (50.000 MHz)	

```
=====
=====
```

Setup Timing Analysis of clk

Setup Slack Path Summary

Data End Index End Pin	Data						Data
	Setup	Path	Source	Dest.	Clock	Clock	
	Slack	Delay	Edge				
-----	-----	-----	-----	-----	-----	-----	-----
1 REGZ_reg_q_reg(29)/D	-3.617	23.443	clk	clk	REGB_reg_q_reg(0)/C		
2 REGZ_reg_q_reg(29)/D	-3.457	23.283	clk	clk	REGA_reg_q_reg(0)/C		
3 REGZ_reg_q_reg(29)/D	-3.437	23.263	clk	clk	REGB_reg_q_reg(1)/C		
4 REGZ_reg_q_reg(29)/D	-3.177	23.003	clk	clk	REGA_reg_q_reg(1)/C		
5 REGZ_reg_q_reg(29)/D	-3.067	22.893	clk	clk	REGA_reg_q_reg(2)/C		
6 REGZ_reg_q_reg(29)/D	-2.873	22.699	clk	clk	REGB_reg_q_reg(2)/C		
7 REGZ_reg_q_reg(29)/D	-2.873	22.699	clk	clk	REGB_reg_q_reg(3)/C		

```

8      -2.753  22.579  clk      clk      REGA_reg_q_reg(3)/C
REGZ_reg_q_reg(29)/D  Rise
9      -2.593  22.419  clk      clk      REGA_reg_q_reg(4)/C
REGZ_reg_q_reg(29)/D  Rise
10     -2.029  21.855  clk      clk      REGA_reg_q_reg(5)/C
REGZ_reg_q_reg(29)/D  Rise

```

CTE Path Report

Critical path #1, (path slack = -3.617):

```

SOURCE CLOCK: name: clk period: 20.000000
    Times are relative to the 1st rising edge
DEST CLOCK: name: clk period: 20.000000
    Times are relative to the 2nd rising edge

```

NAME	GATE	DELAY	ARRIVAL	DIR
FANOUT				
REGB_reg_q_reg(0)/C	FDCE		0.000	up
REGB_reg_q_reg(0)/Q	FDCE	0.370	0.370	up
regb_out(0)	(net)	0.660		37
ix46071z1320/I1	LUT2		1.030	up
ix46071z1320/O	LUT2	0.264	1.294	up
b_signed(1)	(net)	0.640		34
MULT_PP0/ix60683z1313/I0	LUT4		1.934	up
MULT_PP0/ix60683z1313/O	LUT4	0.264	2.198	dn
MULT_PP0/NOT_U2_U2_cout_temp(3)	(net)	0.280		2
MULT_PP0/ix61680z27487/I3	LUT4		2.478	dn
MULT_PP0/ix61680z27487/O	LUT4	0.264	2.742	up
MULT_PP0/twoscompgen_out(4)	(net)	0.280		2
MULT_PP0/ix62677z59362/I2	LUT4		3.022	up
MULT_PP0/ix62677z59362/O	LUT4	0.264	3.286	up
MULT_PP0/ppg_out(4)	(net)	0.290		3
MULT_A1_U1/ix44143z1340/I0	LUT2		3.576	up
MULT_A1_U1/ix44143z1340/O	LUT2	0.264	3.840	up
MULT_A1_U1/nx44143z7	(net)	0.280		1
MULT_A1_U1/ix44143z60716/I3	LUT4		4.120	up
MULT_A1_U1/ix44143z60716/O	LUT4	0.264	4.384	up
MULT_A1_U1/nx44143z6	(net)	0.280		2
MULT_A1_U1/ix44143z62483/I2	LUT4		4.664	up
MULT_A1_U1/ix44143z62483/O	LUT4	0.264	4.928	up
MULT_A1_U1/c(4)	(net)	0.290		3
MULT_A1_U1/ix22782z1464/I2	LUT3		5.218	up
MULT_A1_U1/ix22782z1464/O	LUT3	0.264	5.482	up
MULT_A1_U1/sum(4)	(net)	0.280		2
MULT_A1_U2_U1/ix61094z1556/I0	LUT3		5.762	up
MULT_A1_U2_U1/ix61094z1556/O	LUT3	0.264	6.026	up
MULT_A1_U2_U1/c(3)	(net)	0.280		2
MULT_A1_U2_U1/ix61094z37907/I0	LUT4		6.306	up
MULT_A1_U2_U1/ix61094z37907/O	LUT4	0.264	6.570	up
MULT_A1_U2_U1/c(4)	(net)	0.280		2

MULT_A1_U2_U1/ix61094z1554/I2	LUT3		6.850	up
MULT_A1_U2_U1/ix61094z1554/O	LUT3	0.264	7.114	up
MULT_A1_U2_U1/c(5)	(net)	0.280		2
MULT_A1_U2_U1/ix61094z1553/I2	LUT3		7.394	up
MULT_A1_U2_U1/ix61094z1553/O	LUT3	0.264	7.658	up
MULT_A1_U2_U1/c(6)	(net)	0.280		2
MULT_A1_U2_U1/ix61094z37904/I0	LUT4		7.938	up
MULT_A1_U2_U1/ix61094z37904/O	LUT4	0.264	8.202	up
MULT_A1_U2_U1/c(7)	(net)	0.280		2
MULT_A1_U2_U1/ix61094z1551/I2	LUT3		8.482	up
MULT_A1_U2_U1/ix61094z1551/O	LUT3	0.264	8.746	up
MULT_A1_U2_U1/c(8)	(net)	0.280		2
MULT_A1_U2_U1/ix61094z1550/I2	LUT3		9.026	up
MULT_A1_U2_U1/ix61094z1550/O	LUT3	0.264	9.290	up
MULT_A1_U2_U1/c(9)	(net)	0.280		2
MULT_A1_U2_U1/ix61094z37901/I0	LUT4		9.570	up
MULT_A1_U2_U1/ix61094z37901/O	LUT4	0.264	9.834	up
MULT_A1_U2_U1/c(10)	(net)	0.290		3
MULT_A1_U2_U1/ix62091z60707/I2	LUT4		10.124	up
MULT_A1_U2_U1/ix62091z60707/O	LUT4	0.264	10.388	up
MULT_A1_U2_U1/nx62091z1	(net)	0.280		2
MULT_A1_U2_U1/ix23445z62475/I2	LUT4		10.668	up
MULT_A1_U2_U1/ix23445z62475/O	LUT4	0.264	10.932	up
MULT_A1_U2_U1/c(13)	(net)	0.280		1
MULT_A1_U2_U1/ix23445z1546/I2	LUT3		11.212	up
MULT_A1_U2_U1/ix23445z1546/O	LUT3	0.264	11.476	up
MULT_A1_U2_U1/cout	(net)	0.280		2
MULT_A1_U2_U2/ix61094z1554/I2	LUT3		11.756	up
MULT_A1_U2_U2/ix61094z1554/O	LUT3	0.264	12.020	up
MULT_A1_U2_U2/c(1)	(net)	0.290		3
MULT_A1_U2_U2/ix61094z1553/I2	LUT3		12.310	up
MULT_A1_U2_U2/ix61094z1553/O	LUT3	0.264	12.574	up
MULT_A1_U2_U2/c(2)	(net)	0.320		6
MULT_A1_U2_U2/ix61094z1552/I2	LUT3		12.894	up
MULT_A1_U2_U2/ix61094z1552/O	LUT3	0.264	13.158	up
MULT_A1_U2_U2/c(3)	(net)	0.290		3
MULT_A1_U2_U2/ix61094z1447/I0	LUT3		13.448	up
MULT_A1_U2_U2/ix61094z1447/O	LUT3	0.264	13.712	up
MULT_A1_U2_U2/nx61094z4	(net)	0.290		4
MULT_A1_U2_U2/ix21785z40632/I2	LUT4		14.002	up
MULT_A1_U2_U2/ix21785z40632/O	LUT4	0.264	14.266	up
MULT_A1_U2_U2/sum(5)	(net)	0.320		7
MULT_A1_U3_U2/ix63088z1058/I1	LUT4		14.586	up
MULT_A1_U3_U2/ix63088z1058/O	LUT4	0.264	14.850	up
MULT_A1_U3_U2/nx63088z13	(net)	0.280		1
MULT_A1_U3_U2/ix63088z1499/I2	LUT3		15.130	up
MULT_A1_U3_U2/ix63088z1499/O	LUT3	0.264	15.394	up
MULT_A1_U3_U2/nx63088z12	(net)	0.300		5
MULT_A1_U3_U2/ix63088z1201/I3	LUT4		15.694	up
MULT_A1_U3_U2/ix63088z1201/O	LUT4	0.264	15.958	up
MULT_A1_U3_U2/c(5)	(net)	0.280		2
MULT_A1_U3_U2/ix20788z43964/I3	LUT4		16.238	up

MULT_A1_U3_U2/ix20788z43964/O	LUT4	0.264	16.502	up	
MULT_A1_U3_U2/sum(6)	(net)	0.300			5
MULT_A1_U4_U2/ix63088z1050/I0	LUT4		16.802	up	
MULT_A1_U4_U2/ix63088z1050/O	LUT4	0.264	17.066	up	
MULT_A1_U4_U2/nx63088z6	(net)	0.280			1
MULT_A1_U4_U2/ix63088z1491/I2	LUT3		17.346	up	
MULT_A1_U4_U2/ix63088z1491/O	LUT3	0.264	17.610	up	
MULT_A1_U4_U2/nx63088z5	(net)	0.290			3
MULT_A1_U4_U2/ix18794z1187/I3	LUT4		17.900	up	
MULT_A1_U4_U2/ix18794z1187/O	LUT4	0.264	18.164	up	
MULT_A1_U4_U2/c(7)	(net)	0.290			3
MULT_A1_U4_U2/ix18794z43964/I3	LUT4		18.454	up	
MULT_A1_U4_U2/ix18794z43964/O	LUT4	0.264	18.718	up	
MULT_A1_U4_U2/sum(8)	(net)	0.290			4
MULT_A1_U5_U2/ix17797z1050/I0	LUT4		19.008	up	
MULT_A1_U5_U2/ix17797z1050/O	LUT4	0.264	19.272	up	
MULT_A1_U5_U2/nx17797z6	(net)	0.280			2
MULT_A1_U5_U2/ix18794z1485/I2	LUT3		19.552	up	
MULT_A1_U5_U2/ix18794z1485/O	LUT3	0.264	19.816	up	
MULT_A1_U5_U2/nx18794z1	(net)	0.280			2
MULT_A1_U5_U2/ix18794z1187/I3	LUT4		20.096	up	
MULT_A1_U5_U2/ix18794z1187/O	LUT4	0.264	20.360	up	
MULT_A1_U5_U2/c(7)	(net)	0.280			1
MULT_A1_U5_U2/ix18794z43964/I3	LUT4		20.640	up	
MULT_A1_U5_U2/ix18794z43964/O	LUT4	0.264	20.904	up	
MULT_A1_U5_U2/sum(8)	(net)	0.290			3
MULT_A1_U6_U2/ix17797z1339/I0	LUT2		21.194	up	
MULT_A1_U6_U2/ix17797z1339/O	LUT2	0.264	21.458	up	
MULT_A1_U6_U2/nx17797z8	(net)	0.280			1
MULT_A1_U6_U2/ix17797z45013/I3	LUT4		21.738	up	
MULT_A1_U6_U2/ix17797z45013/O	LUT4	0.264	22.002	up	
MULT_A1_U6_U2/nx17797z7	(net)	0.280			1
MULT_A1_U6_U2/ix17797z55178/I1	MUXF5		22.282	up	
MULT_A1_U6_U2/ix17797z55178/O	MUXF5	0.337	22.619	up	
MULT_A1_U6_U2/sum(9)	(net)	0.280			1
MULT_A1_U7/ix57106z43964/I0	LUT4		22.899	up	
MULT_A1_U7/ix57106z43964/O	LUT4	0.264	23.163	up	
MULT_A1_U7/sum(17)	(net)	0.280			1
REGZ_reg_q_reg(29)/D	FDCE		23.443	up	

Initial edge separation: 20.000

Source clock delay: - 1.359

Dest clock delay: + 1.359

Edge separation: 20.000

Setup constraint: - 0.174

Data required time: 19.826

Data arrival time: - 23.443 (46.94% cell delay,

53.06% net delay)

Slack (VIOLATED): -3.617

```
=====
=====
          Input Delay Report

      Input          Clock Name
Slack (ns)          -----
-----          -----
-----          -----
-----          -----
No input delay constraints.
```

```
=====
=====
          Output Delay Report

      Output          Clock Name
Slack (ns)          -----
-----          -----
-----          -----
-----          -----
No output delay constraints.
```

ALU pipelined-version 16-bit (Radix-4 Booth Multiplier with CLA) Area Report

```
*****
Device Utilization for 2VP2fg256
*****
Resource           Used   Avail   Utilization
-----
IOS                68     140    48.57%
Global Buffers     2      16     12.50%
LUTs               893    2816   31.71%
CLB Slices         447    1408   31.75%
Dffs or Latches   68     3236   2.10%
Block RAMs         0      12     0.00%
Block Multipliers  0      12     0.00%
Block Multiplier Dffs 0    432    0.00%
GT_CUSTOM          0      4      0.00%
-----
*****
***
```

Library: work Cell: alu_pipeline_16bit View:
 alu_pipeline_16bit_arch

Cell	Library	References	Total Area
BUFGP	xcv2p	2 x	
FDC	xcv2p	4 x	4 Dffs or Latches
FDCE	xcv2p	63 x	63 Dffs or Latches
FDC_1	xcv2p	1 x	1 Dffs or Latches
IBUF	xcv2p	33 x	
LUT2	xcv2p	11 x	11 LUTs
LUT3	xcv2p	19 x	19 LUTs
LUT4	xcv2p	31 x	31 LUTs
OBUF	xcv2p	33 x	
VCC	xcv2p	1 x	
cla_10bit	work	1 x	23 gates 23 LUTs 1 MUXF5
cla_10bit_unfolded0	work	1 x	22 gates 22 LUTs
cla_10bit_unfolded1	work	1 x	26 gates 26 LUTs 1 MUXF5
cla_12bit	work	1 x	35 gates 35 LUTs 3 MUXF5
cla_12bit_unfolded0	work	1 x	26 gates 26 LUTs
cla_12bit_unfolded1	work	1 x	31 gates 31 LUTs 2 MUXF5
cla_12bit_unfolded2	work	1 x	26 gates 26 LUTs
cla_14bit	work	1 x	31 gates 31 LUTs
cla_14bit_unfolded0	work	1 x	43 gates 42 LUTs 4 MUXF5
cla_14bit_unfolded1	work	1 x	31 gates 31 LUTs
cla_18bit	work	1 x	44 gates 44 LUTs
cla_30bit	work	1 x	46 gates 43 LUTs 1 MUXF5
ppg_16bit	work	1 x	53 gates 53 LUTs
ppg_16bit_unfolded0	work	1 x	57 gates 57 LUTs
ppg_16bit_unfolded1	work	1 x	57 gates 57 LUTs
ppg_16bit_unfolded2	work	1 x	57 gates

ppg_16bit_unfolded3	work	1 x	57	57 LUTs
			57	57 gates
			57	57 LUTs
ppg_16bit_unfolded4	work	1 x	57	57 gates
			57	57 LUTs
ppg_16bit_unfolded5	work	1 x	57	57 gates
			57	57 LUTs
ppg_16bit_unfolded6	work	1 x	57	57 gates
			57	57 LUTs

Number of ports :	68
Number of nets :	544
Number of instances :	218
Number of references to this view :	0

Total accumulated area :	
Number of Dffs or Latches :	68
Number of LUTs :	893
Number of MUXF5 :	12
Number of gates :	898
Number of accumulated instances :	1042

IO Register Mapping Report

Design: work.alu_pipeline_16bit.alu_pipeline_16bit_arch

Port	Direction	INFF	OUTFF	TRIFF
a(15)	Input			
a(14)	Input			
a(13)	Input			
a(12)	Input			
a(11)	Input			
a(10)	Input			
a(9)	Input			
a(8)	Input			
a(7)	Input			
a(6)	Input			
a(5)	Input			

a(4)	Input			
a(3)	Input			
a(2)	Input			
a(1)	Input			
a(0)	Input			
b(15)	Input			
b(14)	Input			
b(13)	Input			
b(12)	Input			
b(11)	Input			
b(10)	Input			
b(9)	Input			
b(8)	Input			
b(7)	Input			
b(6)	Input			
b(5)	Input			
b(4)	Input			
b(3)	Input			
b(2)	Input			
b(1)	Input			
b(0)	Input			
load	Input			
clk	Input			
clear	Input			
end_flag	Output			
z(31)	Output			

z(30)	Output			
z(29)	Output			
z(28)	Output			
z(27)	Output			
z(26)	Output			
z(25)	Output			
z(24)	Output			
z(23)	Output			
z(22)	Output			
z(21)	Output			
z(20)	Output			
z(19)	Output			
z(18)	Output			
z(17)	Output			
z(16)	Output			
z(15)	Output			
z(14)	Output			
z(13)	Output			
z(12)	Output			
z(11)	Output			
z(10)	Output			
z(9)	Output			
z(8)	Output			
z(7)	Output			
z(6)	Output			
z(5)	Output			

```

+-----+-----+-----+-----+
| z(4) | Output |       |       |
+-----+-----+-----+-----+
| z(3) | Output |       |       |
+-----+-----+-----+-----+
| z(2) | Output |       |       |
+-----+-----+-----+-----+
| z(1) | Output |       |       |
+-----+-----+-----+-----+
| z(0) | Output |       |       |
+-----+-----+-----+-----+
Total registers mapped: 0

```

**ALU pipelined-version 16-bit (Radix-4 Booth Multiplier with CLA)
Timing Report**

```
=====
=====
```

Clock Frequency Report

Domain Period (Freq)	Clock Name Required Period (Freq)	Min
-----	-----	---
-----	-----	-----
ClockDomain0 23.617 (42.342 MHz)	clk 20.000 (50.000 MHz)	

```
=====
=====
```

Setup Timing Analysis of clk

Setup Slack Path Summary

Data End Index End Pin	Data						Data	
	Setup	Path	Source	Dest.				
				Delay	Clock	Clock		
Edge	-----	-----	-----	-----	-----	-----	-----	
1	-3.617	23.443	clk	clk	REGB_reg_q_reg(0)/C			
REGZ_reg_q_reg(29)/D	Rise							
2	-3.457	23.283	clk	clk	REGA_reg_q_reg(0)/C			
REGZ_reg_q_reg(29)/D	Rise							
3	-3.437	23.263	clk	clk	REGB_reg_q_reg(1)/C			
REGZ_reg_q_reg(29)/D	Rise							
4	-3.177	23.003	clk	clk	REGA_reg_q_reg(1)/C			
REGZ_reg_q_reg(29)/D	Rise							

5	-3.067	22.893	clk	clk	REGA_reg_q_reg(2)/C
REGZ_reg_q_reg(29)/D	Rise				
6	-2.873	22.699	clk	clk	REGB_reg_q_reg(3)/C
REGZ_reg_q_reg(29)/D	Rise				
7	-2.873	22.699	clk	clk	REGB_reg_q_reg(2)/C
REGZ_reg_q_reg(29)/D	Rise				
8	-2.753	22.579	clk	clk	REGA_reg_q_reg(3)/C
REGZ_reg_q_reg(29)/D	Rise				
9	-2.593	22.419	clk	clk	REGA_reg_q_reg(4)/C
REGZ_reg_q_reg(29)/D	Rise				
10	-2.029	21.855	clk	clk	REGA_reg_q_reg(5)/C
REGZ_reg_q_reg(29)/D	Rise				

CTE Path Report

Critical path #1, (path slack = -3.617):

```
SOURCE CLOCK: name: clk period: 20.000000
    Times are relative to the 1st rising edge
DEST CLOCK: name: clk period: 20.000000
    Times are relative to the 2nd rising edge
```

NAME	GATE	DELAY	ARRIVAL	DIR
FANOUT				
REGB_reg_q_reg(0)/C	FDCE		0.000	up
REGB_reg_q_reg(0)/Q	FDCE	0.370	0.370	up
regb_out(0)	(net)	0.660		37
ix46071z1320/I1	LUT2		1.030	up
ix46071z1320/O	LUT2	0.264	1.294	up
b_signed(1)	(net)	0.640		34
MULT_PP0/ix60683z1313/I0	LUT4		1.934	up
MULT_PP0/ix60683z1313/O	LUT4	0.264	2.198	dn
MULT_PP0/NOT_U2_U2_cout_temp(3)	(net)	0.280		2
MULT_PP0/ix61680z27487/I3	LUT4		2.478	dn
MULT_PP0/ix61680z27487/O	LUT4	0.264	2.742	up
MULT_PP0/twoscompgen_out(4)	(net)	0.280		2
MULT_PP0/ix62677z59362/I2	LUT4		3.022	up
MULT_PP0/ix62677z59362/O	LUT4	0.264	3.286	up
MULT_PP0/ppg_out(4)	(net)	0.290		3
MULT_A1_U1/ix44143z1340/I0	LUT2		3.576	up
MULT_A1_U1/ix44143z1340/O	LUT2	0.264	3.840	up
MULT_A1_U1/nx44143z7	(net)	0.280		1
MULT_A1_U1/ix44143z60716/I3	LUT4		4.120	up
MULT_A1_U1/ix44143z60716/O	LUT4	0.264	4.384	up
MULT_A1_U1/nx44143z6	(net)	0.280		2
MULT_A1_U1/ix44143z62483/I2	LUT4		4.664	up
MULT_A1_U1/ix44143z62483/O	LUT4	0.264	4.928	up
MULT_A1_U1/c(4)	(net)	0.290		3
MULT_A1_U1/ix22782z1464/I2	LUT3		5.218	up
MULT_A1_U1/ix22782z1464/O	LUT3	0.264	5.482	up
MULT_A1_U1/sum(4)	(net)	0.280		2

MULT_A1_U2_U1/ix61094z1556/I0	LUT3		5.762	up
MULT_A1_U2_U1/ix61094z1556/O	LUT3	0.264	6.026	up
MULT_A1_U2_U1/c(3)	(net)	0.280		2
MULT_A1_U2_U1/ix61094z37907/I0	LUT4		6.306	
MULT_A1_U2_U1/ix61094z37907/O	LUT4	0.264	6.570	up
MULT_A1_U2_U1/c(4)	(net)	0.280		2
MULT_A1_U2_U1/ix61094z1554/I2	LUT3		6.850	
MULT_A1_U2_U1/ix61094z1554/O	LUT3	0.264	7.114	up
MULT_A1_U2_U1/c(5)	(net)	0.280		2
MULT_A1_U2_U1/ix61094z1553/I2	LUT3		7.394	
MULT_A1_U2_U1/ix61094z1553/O	LUT3	0.264	7.658	up
MULT_A1_U2_U1/c(6)	(net)	0.280		2
MULT_A1_U2_U1/ix61094z37904/I0	LUT4		7.938	
MULT_A1_U2_U1/ix61094z37904/O	LUT4	0.264	8.202	up
MULT_A1_U2_U1/c(7)	(net)	0.280		2
MULT_A1_U2_U1/ix61094z1551/I2	LUT3		8.482	
MULT_A1_U2_U1/ix61094z1551/O	LUT3	0.264	8.746	up
MULT_A1_U2_U1/c(8)	(net)	0.280		2
MULT_A1_U2_U1/ix61094z1550/I2	LUT3		9.026	
MULT_A1_U2_U1/ix61094z1550/O	LUT3	0.264	9.290	up
MULT_A1_U2_U1/c(9)	(net)	0.280		2
MULT_A1_U2_U1/ix61094z37901/I0	LUT4		9.570	
MULT_A1_U2_U1/ix61094z37901/O	LUT4	0.264	9.834	up
MULT_A1_U2_U1/c(10)	(net)	0.290		3
MULT_A1_U2_U1/ix62091z60707/I2	LUT4		10.124	
MULT_A1_U2_U1/ix62091z60707/O	LUT4	0.264	10.388	up
MULT_A1_U2_U1/nx62091z1	(net)	0.280		2
MULT_A1_U2_U1/ix23445z62475/I2	LUT4		10.668	
MULT_A1_U2_U1/ix23445z62475/O	LUT4	0.264	10.932	up
MULT_A1_U2_U1/c(13)	(net)	0.280		1
MULT_A1_U2_U1/ix23445z1546/I2	LUT3		11.212	
MULT_A1_U2_U1/ix23445z1546/O	LUT3	0.264	11.476	up
MULT_A1_U2_U1/cout	(net)	0.280		2
MULT_A1_U2_U2/ix61094z1554/I2	LUT3		11.756	
MULT_A1_U2_U2/ix61094z1554/O	LUT3	0.264	12.020	up
MULT_A1_U2_U2/c(1)	(net)	0.290		3
MULT_A1_U2_U2/ix61094z1553/I2	LUT3		12.310	
MULT_A1_U2_U2/ix61094z1553/O	LUT3	0.264	12.574	up
MULT_A1_U2_U2/c(2)	(net)	0.320		6
MULT_A1_U2_U2/ix61094z1552/I2	LUT3		12.894	
MULT_A1_U2_U2/ix61094z1552/O	LUT3	0.264	13.158	up
MULT_A1_U2_U2/c(3)	(net)	0.290		3
MULT_A1_U2_U2/ix61094z1447/I0	LUT3		13.448	
MULT_A1_U2_U2/ix61094z1447/O	LUT3	0.264	13.712	up
MULT_A1_U2_U2/nx61094z4	(net)	0.290		4
MULT_A1_U2_U2/ix21785z40632/I2	LUT4		14.002	
MULT_A1_U2_U2/ix21785z40632/O	LUT4	0.264	14.266	up
MULT_A1_U2_U2/sum(5)	(net)	0.320		7
MULT_A1_U3_U2/ix63088z1058/I1	LUT4		14.586	up
MULT_A1_U3_U2/ix63088z1058/O	LUT4	0.264	14.850	up
MULT_A1_U3_U2/nx63088z13	(net)	0.280		1
MULT_A1_U3_U2/ix63088z1499/I2	LUT3		15.130	

MULT_A1_U3_U2/ix63088z1499/O	LUT3	0.264	15.394	up	
MULT_A1_U3_U2/nx63088z12	(net)	0.300			5
MULT_A1_U3_U2/ix63088z1201/I3	LUT4		15.694	up	
MULT_A1_U3_U2/ix63088z1201/O	LUT4	0.264	15.958	up	
MULT_A1_U3_U2/c(5)	(net)	0.280			2
MULT_A1_U3_U2/ix20788z43964/I3	LUT4		16.238	up	
MULT_A1_U3_U2/ix20788z43964/O	LUT4	0.264	16.502	up	
MULT_A1_U3_U2/sum(6)	(net)	0.300			5
MULT_A1_U4_U2/ix63088z1050/I0	LUT4		16.802	up	
MULT_A1_U4_U2/ix63088z1050/O	LUT4	0.264	17.066	up	
MULT_A1_U4_U2/nx63088z6	(net)	0.280			1
MULT_A1_U4_U2/ix63088z1491/I2	LUT3		17.346	up	
MULT_A1_U4_U2/ix63088z1491/O	LUT3	0.264	17.610	up	
MULT_A1_U4_U2/nx63088z5	(net)	0.290			3
MULT_A1_U4_U2/ix18794z1187/I3	LUT4		17.900	up	
MULT_A1_U4_U2/ix18794z1187/O	LUT4	0.264	18.164	up	
MULT_A1_U4_U2/c(7)	(net)	0.290			3
MULT_A1_U4_U2/ix18794z43964/I3	LUT4		18.454	up	
MULT_A1_U4_U2/ix18794z43964/O	LUT4	0.264	18.718	up	
MULT_A1_U4_U2/sum(8)	(net)	0.290			4
MULT_A1_U5_U2/ix17797z1050/I0	LUT4		19.008	up	
MULT_A1_U5_U2/ix17797z1050/O	LUT4	0.264	19.272	up	
MULT_A1_U5_U2/nx17797z6	(net)	0.280			2
MULT_A1_U5_U2/ix18794z1485/I2	LUT3		19.552	up	
MULT_A1_U5_U2/ix18794z1485/O	LUT3	0.264	19.816	up	
MULT_A1_U5_U2/nx18794z1	(net)	0.280			2
MULT_A1_U5_U2/ix18794z1187/I3	LUT4		20.096	up	
MULT_A1_U5_U2/ix18794z1187/O	LUT4	0.264	20.360	up	
MULT_A1_U5_U2/c(7)	(net)	0.280			1
MULT_A1_U5_U2/ix18794z43964/I3	LUT4		20.640	up	
MULT_A1_U5_U2/ix18794z43964/O	LUT4	0.264	20.904	up	
MULT_A1_U5_U2/sum(8)	(net)	0.290			3
MULT_A1_U6_U2/ix17797z1339/I0	LUT2		21.194	up	
MULT_A1_U6_U2/ix17797z1339/O	LUT2	0.264	21.458	up	
MULT_A1_U6_U2/nx17797z8	(net)	0.280			1
MULT_A1_U6_U2/ix17797z45013/I3	LUT4		21.738	up	
MULT_A1_U6_U2/ix17797z45013/O	LUT4	0.264	22.002	up	
MULT_A1_U6_U2/nx17797z7	(net)	0.280			1
MULT_A1_U6_U2/ix17797z55178/I1	MUXF5		22.282	up	
MULT_A1_U6_U2/ix17797z55178/O	MUXF5	0.337	22.619	up	
MULT_A1_U6_U2/sum(9)	(net)	0.280			1
MULT_A1_U7/ix57106z43964/I0	LUT4		22.899	up	
MULT_A1_U7/ix57106z43964/O	LUT4	0.264	23.163	up	
MULT_A1_U7/sum(17)	(net)	0.280			1
REGZ_reg_q_reg(29)/D	FDCE		23.443	up	

Initial edge separation: 20.000

Source clock delay: - 1.359

Dest clock delay: + 1.359

Edge separation: 20.000

Setup constraint: - 0.174

```

-----  

Data required time:          19.826  

Data arrival time:           - 23.443   ( 46.94% cell delay,  

53.06% net delay )  

-----  

Slack (VIOLATED):          -3.617

```

```
=====
=====  

Input Delay Report
```

Input Slack (ns)	Clock Name
-----	-----
-----	-----

No input delay constraints.

```
=====
=====  

Output Delay Report
```

Output Slack (ns)	Clock Name
-----	-----
-----	-----

No output delay constraints.

ALU with multiply-accumulate 16-bit (Radix-4 Booth Multiplier with CLA) Area Report

```
*****  

Device Utilization for 2VP2fg256  

*****  

Resource           Used     Avail   Utilization
-----  

IOS                72       140    51.43%  

Global Buffers      2        16    12.50%  

LUTs              1043      2816   37.04%  

CLB Slices         522      1408   37.07%  

Dffs or Latches    109      3236    3.37%  

Block RAMs          0        12    0.00%  

Block Multipliers    0        12    0.00%  

Block Multiplier Dffs 0        432    0.00%  

GT_CUSTOM          0         4    0.00%
-----
```

Library: work Cell: alu_accumulate View: alu_accumulate_arch

Cell	Library	References	Total Area
BUFGP	xcv2p	2 x	
FDC	xcv2p	4 x	1 4 Dffs or Latches
FDCE	xcv2p	103 x	103 Dffs or Latches
FDC_1	xcv2p	1 x	1 Dffs or Latches
FDE	xcv2p	1 x	1 Dffs or Latches
IBUF	xcv2p	33 x	
LUT1	xcv2p	1 x	1 LUTs
LUT2	xcv2p	11 x	11 LUTs
LUT3	xcv2p	19 x	19 LUTs
LUT4	xcv2p	32 x	32 LUTs
OBUF	xcv2p	37 x	
VCC	xcv2p	1 x	
cla_10bit	work	1 x	23 gates 23 LUTs 1 MUXF5
cla_10bit_unfolded0	work	1 x	22 gates 22 LUTs
cla_10bit_unfolded1	work	1 x	26 gates 26 LUTs 1 MUXF5
cla_10bit_unfolded2	work	1 x	24 gates 24 LUTs 1 MUXF5
cla_12bit	work	1 x	35 gates 35 LUTs 3 MUXF5
cla_12bit_unfolded0	work	1 x	26 gates 26 LUTs
cla_12bit_unfolded1	work	1 x	31 gates 31 LUTs 2 MUXF5
cla_12bit_unfolded2	work	1 x	26 gates 26 LUTs
cla_12bit_unfolded3	work	1 x	27 gates 27 LUTs
cla_14bit	work	1 x	31 gates 31 LUTs
cla_14bit_unfolded0	work	1 x	43 gates 42 LUTs 4 MUXF5
cla_14bit_unfolded1	work	1 x	31 gates 31 LUTs
cla_14bit_unfolded2	work	1 x	31 gates 31 LUTs

cla_18bit	work	1 x	44	44 gates
			42	42 LUTs
cla_30bit	work	1 x	44	44 gates
			42	42 LUTs
incrementer_34bit	work	1 x	69	69 gates
			68	68 LUTs
ppg_16bit	work	1 x	55	55 gates
			55	55 LUTs
ppg_16bit_unfolded0	work	1 x	57	57 gates
			57	57 LUTs
ppg_16bit_unfolded1	work	1 x	57	57 gates
			57	57 LUTs
ppg_16bit_unfolded2	work	1 x	57	57 gates
			57	57 LUTs
ppg_16bit_unfolded3	work	1 x	57	57 gates
			57	57 LUTs
ppg_16bit_unfolded4	work	1 x	57	57 gates
			57	57 LUTs
ppg_16bit_unfolded5	work	1 x	57	57 gates
			57	57 LUTs
ppg_16bit_unfolded6	work	1 x	57	57 gates
			57	57 LUTs

Number of ports :	72
Number of nets :	667
Number of instances :	269
Number of references to this view :	0

Total accumulated area :	
Number of Dffs or Latches :	109
Number of LUTs :	1043
Number of MUXF5 :	12
Number of gates :	1051
Number of accumulated instances :	1238

IO Register Mapping Report

Design: work.alu_accumulate.alu_accumulate_arch

Port	Direction	INFF	OUTFF	TRIFF
a(15)	Input			
a(14)	Input			
a(13)	Input			
a(12)	Input			

a(11)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
a(10)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
a(9)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
a(8)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
a(7)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
a(6)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
a(5)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
a(4)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
a(3)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
a(2)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
a(1)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
a(0)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
b(15)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
b(14)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
b(13)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
b(12)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
b(11)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
b(10)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
b(9)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
b(8)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
b(7)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
b(6)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
b(5)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
b(4)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
b(3)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
b(2)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+

b(1)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
b(0)	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
load	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
clk	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
clear	Input			
+-----+	+-----+	+-----+	+-----+	+-----+
end_flag	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(35)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(34)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(33)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(32)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(31)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(30)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(29)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(28)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(27)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(26)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(25)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(24)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(23)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(22)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(21)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(20)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(19)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(18)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(17)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+
z(16)	Output			
+-----+	+-----+	+-----+	+-----+	+-----+

z(15)	Output			
+-----+-----+-----+-----+				
z(14)	Output			
+-----+-----+-----+-----+				
z(13)	Output			
+-----+-----+-----+-----+				
z(12)	Output			
+-----+-----+-----+-----+				
z(11)	Output			
+-----+-----+-----+-----+				
z(10)	Output			
+-----+-----+-----+-----+				
z(9)	Output			
+-----+-----+-----+-----+				
z(8)	Output			
+-----+-----+-----+-----+				
z(7)	Output			
+-----+-----+-----+-----+				
z(6)	Output			
+-----+-----+-----+-----+				
z(5)	Output			
+-----+-----+-----+-----+				
z(4)	Output			
+-----+-----+-----+-----+				
z(3)	Output			
+-----+-----+-----+-----+				
z(2)	Output			
+-----+-----+-----+-----+				
z(1)	Output			
+-----+-----+-----+-----+				
z(0)	Output			
+-----+-----+-----+-----+				

Total registers mapped: 0

ALU with multiply-accumulate 16-bit (Radix-4 Booth Multiplier with CLA) Timing Report

Clock Frequency Report

Domain Period (Freq) -----	Clock Name Required Period (Freq) -----	Min ---
ClockDomain0 25.823 (38.725 MHz)	clk 20.000 (50.000 MHz)	

```
=====
=====
Setup Timing Analysis of clk
```

Setup Slack Path Summary

Data							
Data	Setup	Path	Source	Dest.			
End	Index	Slack	Delay	Clock	Clock	Data Start	Pin Data
End Pin			Edge				
	1	-5.823	25.649	clk	clk	REGB_reg_q_reg(0)/C	
REGC_reg_q_reg(35)/D			Rise				
	2	-5.683	25.509	clk	clk	REGA_reg_q_reg(0)/C	
REGC_reg_q_reg(35)/D			Rise				
	3	-5.663	25.489	clk	clk	REGB_reg_q_reg(1)/C	
REGC_reg_q_reg(35)/D			Rise				
	4	-5.403	25.229	clk	clk	REGA_reg_q_reg(1)/C	
REGC_reg_q_reg(35)/D			Rise				
	5	-5.293	25.119	clk	clk	REGA_reg_q_reg(2)/C	
REGC_reg_q_reg(35)/D			Rise				
	6	-5.059	24.885	clk	clk	REGB_reg_q_reg(3)/C	
REGC_reg_q_reg(35)/D			Rise				
	7	-5.059	24.885	clk	clk	REGB_reg_q_reg(2)/C	
REGC_reg_q_reg(35)/D			Rise				
	8	-4.969	24.795	clk	clk	REGA_reg_q_reg(3)/C	
REGC_reg_q_reg(35)/D			Rise				
	9	-4.789	24.615	clk	clk	REGA_reg_q_reg(4)/C	
REGC_reg_q_reg(35)/D			Rise				
	10	-4.689	24.515	clk	clk	REGA_reg_q_reg(5)/C	
REGC_reg_q_reg(35)/D			Rise				

CTE Path Report

Critical path #1, (path slack = -5.823):

```
SOURCE CLOCK: name: clk period: 20.000000
    Times are relative to the 1st rising edge
DEST CLOCK: name: clk period: 20.000000
    Times are relative to the 2nd rising edge
```

NAME	GATE	DELAY	ARRIVAL	DIR
FANOUT				
REGB_reg_q_reg(0)/C	FDCE		0.000	up
REGB_reg_q_reg(0)/Q	FDCE	0.370	0.370	up
regb_out(0)	(net)	0.680		42
ix46071z1320/I1	LUT2		1.050	up
ix46071z1320/O	LUT2	0.264	1.314	up

b_signed(1)	(net)	0.620		33
MULT_PP0/ix53066z1315/I0	LUT4	1.934	up	
MULT_PP0/ix53066z1315/O	LUT4	0.264	dn	
MULT_PP0/NOT_U2_U2_cout_temp(3)	(net)	0.300		5
MULT_PP0/ix62677z39820/I1	LUT4	2.498	dn	
MULT_PP0/ix62677z39820/O	LUT4	0.264	up	
MULT_PP0/twoscompgen_out(3)	(net)	0.280		2
MULT_PP0/ix63674z59362/I2	LUT4	3.042	up	
MULT_PP0/ix63674z59362/O	LUT4	0.264	up	
MULT_PP0/ppg_out(3)	(net)	0.280		2
MULT_A1_U1/ix44143z60876/I0	LUT4	3.586	up	
MULT_A1_U1/ix44143z60876/O	LUT4	0.264	up	
MULT_A1_U1/c(2)	(net)	0.290		3
MULT_A1_U1/ix23779z1547/I2	LUT3	4.140	up	
MULT_A1_U1/ix23779z1547/O	LUT3	0.264	up	
MULT_A1_U1/c(3)	(net)	0.280		1
MULT_A1_U1/ix23779z1464/I2	LUT3	4.684	up	
MULT_A1_U1/ix23779z1464/O	LUT3	0.264	up	
MULT_A1_U1/sum(3)	(net)	0.280		2
MULT_A1_U2_U1/ix61094z60877/I0	LUT4	5.228	up	
MULT_A1_U2_U1/ix61094z60877/O	LUT4	0.264	up	
MULT_A1_U2_U1/c(2)	(net)	0.280		2
MULT_A1_U2_U1/ix61094z1556/I2	LUT3	5.772	up	
MULT_A1_U2_U1/ix61094z1556/O	LUT3	0.264	up	
MULT_A1_U2_U1/c(3)	(net)	0.280		2
MULT_A1_U2_U1/ix61094z1555/I2	LUT3	6.316	up	
MULT_A1_U2_U1/ix61094z1555/O	LUT3	0.264	up	
MULT_A1_U2_U1/c(4)	(net)	0.280		2
MULT_A1_U2_U1/ix61094z37906/I0	LUT4	6.860	up	
MULT_A1_U2_U1/ix61094z37906/O	LUT4	0.264	up	
MULT_A1_U2_U1/c(5)	(net)	0.280		2
MULT_A1_U2_U1/ix61094z1553/I2	LUT3	7.404	up	
MULT_A1_U2_U1/ix61094z1553/O	LUT3	0.264	up	
MULT_A1_U2_U1/c(6)	(net)	0.280		2
MULT_A1_U2_U1/ix61094z1552/I2	LUT3	7.948	up	
MULT_A1_U2_U1/ix61094z1552/O	LUT3	0.264	up	
MULT_A1_U2_U1/c(7)	(net)	0.280		2
MULT_A1_U2_U1/ix61094z37903/I0	LUT4	8.492	up	
MULT_A1_U2_U1/ix61094z37903/O	LUT4	0.264	up	
MULT_A1_U2_U1/c(8)	(net)	0.280		2
MULT_A1_U2_U1/ix61094z1550/I2	LUT3	9.036	up	
MULT_A1_U2_U1/ix61094z1550/O	LUT3	0.264	up	
MULT_A1_U2_U1/c(9)	(net)	0.280		2
MULT_A1_U2_U1/ix61094z1549/I2	LUT3	9.580	up	
MULT_A1_U2_U1/ix61094z1549/O	LUT3	0.264	up	
MULT_A1_U2_U1/c(10)	(net)	0.290		3
MULT_A1_U2_U1/ix61094z37900/I0	LUT4	10.134	up	
MULT_A1_U2_U1/ix61094z37900/O	LUT4	0.264	up	
MULT_A1_U2_U1/c(11)	(net)	0.280		2
MULT_A1_U2_U1/ix61094z1547/I2	LUT3	10.678	up	
MULT_A1_U2_U1/ix61094z1547/O	LUT3	0.264	up	
MULT_A1_U2_U1/c(12)	(net)	0.280		1

MULT_A1_U2_U1/ix61094z7434/I2	LUT4		11.222	up
MULT_A1_U2_U1/ix61094z7434/O	LUT4	0.264	11.486	up
MULT_A1_U2_U1/sum(13)	(net)	0.290		4
MULT_A1_U3_U1/ix62091z1330/I0	LUT2		11.776	up
MULT_A1_U3_U1/ix62091z1330/O	LUT2	0.264	12.040	up
MULT_A1_U3_U1/nx62091z2	(net)	0.280		1
MULT_A1_U3_U1/ix62091z60707/I3	LUT4		12.320	up
MULT_A1_U3_U1/ix62091z60707/O	LUT4	0.264	12.584	up
MULT_A1_U3_U1/nx62091z1	(net)	0.280		2
MULT_A1_U3_U1/ix62091z40632/I2	LUT4		12.864	up
MULT_A1_U3_U1/ix62091z40632/O	LUT4	0.264	13.128	up
MULT_A1_U3_U1/sum(12)	(net)	0.290		4
MULT_A1_U4_U1/ix23445z1330/I0	LUT2		13.418	up
MULT_A1_U4_U1/ix23445z1330/O	LUT2	0.264	13.682	up
MULT_A1_U4_U1/nx23445z2	(net)	0.280		1
MULT_A1_U4_U1/ix23445z60707/I3	LUT4		13.962	up
MULT_A1_U4_U1/ix23445z60707/O	LUT4	0.264	14.226	up
MULT_A1_U4_U1/nx23445z1	(net)	0.280		1
MULT_A1_U4_U1/ix23445z62474/I2	LUT4		14.506	up
MULT_A1_U4_U1/ix23445z62474/O	LUT4	0.264	14.770	up
MULT_A1_U4_U1/cout	(net)	0.290		4
MULT_A1_U4_U2/ix63088z1553/I2	LUT3		15.060	up
MULT_A1_U4_U2/ix63088z1553/O	LUT3	0.264	15.324	up
MULT_A1_U4_U2/c(1)	(net)	0.290		3
MULT_A1_U4_U2/ix63088z1552/I2	LUT3		15.614	up
MULT_A1_U4_U2/ix63088z1552/O	LUT3	0.264	15.878	up
MULT_A1_U4_U2/c(2)	(net)	0.280		2
MULT_A1_U4_U2/ix63088z1551/I2	LUT3		16.158	up
MULT_A1_U4_U2/ix63088z1551/O	LUT3	0.264	16.422	up
MULT_A1_U4_U2/c(3)	(net)	0.280		2
MULT_A1_U4_U2/ix63088z1550/I2	LUT3		16.702	up
MULT_A1_U4_U2/ix63088z1550/O	LUT3	0.264	16.966	up
MULT_A1_U4_U2/c(4)	(net)	0.320		7
MULT_A1_U4_U2/ix22782z1464/I2	LUT3		17.286	up
MULT_A1_U4_U2/ix22782z1464/O	LUT3	0.264	17.550	up
MULT_A1_U4_U2/sum(4)	(net)	0.290		4
MULT_A1_U5_U2/ix17797z1550/I0	LUT3		17.840	up
MULT_A1_U5_U2/ix17797z1550/O	LUT3	0.264	18.104	up
MULT_A1_U5_U2/c(3)	(net)	0.280		2
MULT_A1_U5_U2/ix17797z1549/I2	LUT3		18.384	up
MULT_A1_U5_U2/ix17797z1549/O	LUT3	0.264	18.648	up
MULT_A1_U5_U2/c(4)	(net)	0.320		6
MULT_A1_U5_U2/ix18794z1548/I2	LUT3		18.968	up
MULT_A1_U5_U2/ix18794z1548/O	LUT3	0.264	19.232	up
MULT_A1_U5_U2/c(5)	(net)	0.280		2
MULT_A1_U5_U2/ix20788z43964/I3	LUT4		19.512	up
MULT_A1_U5_U2/ix20788z43964/O	LUT4	0.264	19.776	up
MULT_A1_U5_U2/sum(6)	(net)	0.300		5
MULT_A1_U6_U2/ix17797z1337/I0	LUT2		20.076	up
MULT_A1_U6_U2/ix17797z1337/O	LUT2	0.264	20.340	up
MULT_A1_U6_U2/nx17797z6	(net)	0.280		1
MULT_A1_U6_U2/ix17797z60708/I3	LUT4		20.620	up

MULT_A1_U6_U2/ix17797z60708/O	LUT4	0.264	20.884	up	
MULT_A1_U6_U2/nx17797z2	(net)	0.290			3
MULT_A1_U6_U2/ix19791z43708/I3	LUT4		21.174	up	
MULT_A1_U6_U2/ix19791z43708/O	LUT4	0.264	21.438	up	
MULT_A1_U6_U2/sum(7)	(net)	0.290			4
MULT_A1_U7/ix58103z1330/I0	LUT2		21.728	up	
MULT_A1_U7/ix58103z1330/O	LUT2	0.264	21.992	up	
MULT_A1_U7/nx58103z2	(net)	0.280			1
MULT_A1_U7/ix58103z60707/I3	LUT4		22.272	up	
MULT_A1_U7/ix58103z60707/O	LUT4	0.264	22.536	up	
MULT_A1_U7/nx58103z1	(net)	0.280			1
MULT_A1_U7/ix58103z40632/I2	LUT4		22.816	up	
MULT_A1_U7/ix58103z40632/O	LUT4	0.264	23.080	up	
MULT_A1_U7/sum(16)	(net)	0.320			6
ADD_U3/ix17797z1064/I0	LUT4		23.400	up	
ADD_U3/ix17797z1064/O	LUT4	0.264	23.664	up	
ADD_U3/nx17797z6	(net)	0.280			2
ADD_U3/ix17797z1291/I3	LUT4		23.944	up	
ADD_U3/ix17797z1291/O	LUT4	0.264	24.208	up	
ADD_U3/nx17797z5	(net)	0.280			1
ADD_U3/ix17797z45011/I1	LUT4		24.488	up	
ADD_U3/ix17797z45011/O	LUT4	0.264	24.752	up	
ADD_U3/nx17797z4	(net)	0.280			1
ADD_U3/ix17797z55178/I1	MUXF5		25.032	up	
ADD_U3/ix17797z55178/O	MUXF5	0.337	25.369	up	
ADD_U3/sum(9)	(net)	0.280			1
REGC_reg_q_reg(35)/D	FDCE		25.649	up	

Initial edge separation:	20.000
Source clock delay:	- 1.359
Dest clock delay:	+ 1.359

Edge separation:	20.000
Setup constraint:	- 0.174

Data required time:	19.826
Data arrival time:	- 25.649 (47.02% cell delay, 52.98% net delay)

Slack (VIOLATED):	-5.823

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Input Delay Report

Input Slack (ns)	Clock Name	----
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No input delay constraints.

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          Output Delay Report

  Output                      Clock Name
Slack (ns)
  -----                      -----
  -----
No output delay constraints.
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