PROJECT_Fall_2020

Project description

The goal of this project is to design an arithmetic unit capable of calculating **Z = ¼ [A * B] + 1**. The unit will receive the operands A, and B 8-bit ***unsigned*** numbers. A 1 to 0 transition at the LOAD pin will latch the operands into internal register RA and RB. The unit outputs the results in 16-bit register RZ output port. Each calculation starts with a LOAD signal and ends with an END_FLAG signal.

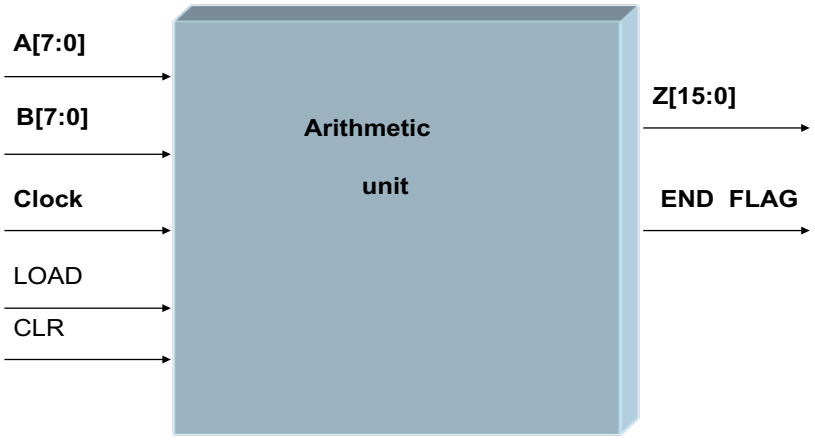

Figure 1: The Unit black box

.1 Requirements

Table 1 is a summary of the design requirements. There are certain behaviors on the inputs that were not specified in the COEN 6501 project description and would allow for different interpretation on these signals.

Requirement number	Description	Comment
Req1	The choice of type of multiplier, is left to the student	
Req2	The design shall be structural.	
Req3	The operands A and B are latched into register RA and RB when LOAD signal transit from high to low.	
Req4	The CLEAR signal will clear all registers to '0'.	
Req5	The 16-bit product shall be loaded into the 16-bit Z port.	
Req6	The unit performs the arithmetic operation until END_FLAG becomes high.	

Table 1: Design Requirements

Signal Specifications

A0-A7: Unsigned 8-bit Operand A
B0-B 7: Unsigned 8-bit Operand B
Z0-Z15 Signed Output
CLR: Clears selected registers
LOAD: Loads Operand into internal registers
CLK: Clock input
END_FLAG Indicates end of operation

.2 Extra features

- *Expansion of the method for 16 bits operand.*
- *Pipelining of the design.*
- *Multiply Accumulate for additional operands*

.3 Evaluation presentation:

- Give breakdown of work by each team member.
- Give full design particulars and all circuits used.
- Give how you Modeled your circuit using VHDL.
- Give Simulation results of your design with various inputs that test your circuit effectively.
- Provide detailed timing diagram.
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Projects will be judged based on:

- Breakdown of work by each team member.
- Delivery on time.
- Specification.
- Design methodology and approach and any methodology used to minimize area delay or power.
- Effectiveness of results, testing methodology and Analysis of results.
- Code organization.
- Presentation and documentation.

.4 Delivery

Project reports due date is 2:00 P.M. Monday Dec 7th, 2020 through moodle. A submission link will be available.