PROJECT

DUE DATE: March 11

Objectives

To learn

1. How to write verification functional test plan based on a design specification,
2. How to create a verification environment for the given design under verification using the test plan
3. How to find errors in the given design.

You are given a hardware design. You should build a traditional testbench based in SystemVerilog. The objective of this project is to apply only direct testing.

Things to do:

1. Create a test plan spreadsheet for the design specification with the following five columns:
   Specification/Feature,
   Reference,
   Test points,
   Test Scenarios,
   Expected Results.

Identify the testable device features and specifications and write them in the Specification/Feature column. These can be copied from the spec doc verbatim if they are already appropriately descriptive. In the reference column, add the section number in which the specification was found. In the Test Points describe the particular feature that you would like to test. In the Test Scenarios column, describe the stimulus that you would apply to exercise the identified specification. This may be a high-level or low-level description depending on the scenario you are creating. If you have more than one scenario, go to a new row in the same column. The Expected Results column should then be used to describe what you would expect to observe to know if the test passed or failed. Note that at this point, we do not need to specify specific verification technologies or verification code/modules that need to be written.

Deliverable

A detailed report containing the test plan, the test cases used for verification, the list of bugs found, and the codes used for verification must be submitted before the deadline.