Task 1:

The **K-N-N** classifier is one of the oldest methods known for classification of data. The idea is extremely simple: to classify **X (unknown entry in the system)** find its closest ***K*** neighbors among the training points and assign to ***X*** the majority label from the K selected neighbors.

In this task, you are

a. Required to present RTL diagram with proper working of K-NN algorithm. Consider the following requirements while designing:
    a. X and all datapoints are **2D** where each datapoint is **8-bit wide**
    b. The closest distance in being computed using city block **($\boldsymbol{Distance} = |\boldsymbol{x2} - \boldsymbol{x1}| + |\boldsymbol{y2} - \boldsymbol{y1}|$)**
    c. The systems get **N-known** data points with their **labels (0-3).**
    d. Clearly specify the bus width, memory (depth, address lines) and type of design (FDA, TSA, Pipelined etc.)
b. Write a synthesizable RTL Verilog code for the design and test it through a proper testbench.
c. Once the code is approved, you will be required to provide timing and utilization summary of your design using Xilinx tools.
d. The last part of the project comprises of running this code on Spartan 6. Details of this part will be shared later.