Zürcher Hochschule für Angewandte Wissenschaften
School of Engineering

Laboratory 4:
AD-DA Conversion

In this laboratory we will investigate different aspects of analog to digital, and, digital to analog signal conversion, plus compare related effects, like aliasing and quantization noise between practical implementation and theory.

We use a HW board containing an analog to digital converter (ADC), which samples and quantizes an analog input signal x(t), with a given number of bits (resolution) and generates the discrete signal output $x_S[n]$. The sampling frequency Fs is a constant and known parameter. Before the ADC an anti-aliasing filter can be deployed (we will see what for).

On the other side the discrete signal $x_S[n]$ is converted back to an analog signal by a digital to analog converter (DAC). The DAC has a zero-order-holder and is often combined with an anti-imaging or reconstruction filter delivering the reconstructed analog signal $x_R(t)$.

The block diagram of this HW board is shown below in figure 1. The detailed schematics is provided in the annex.

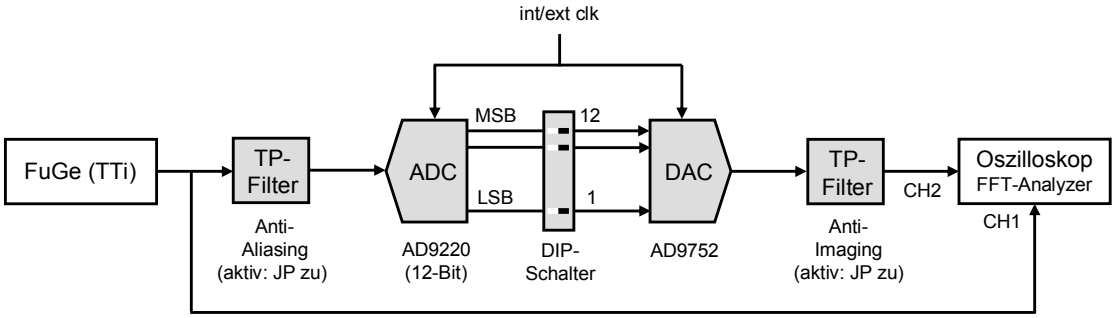


Figure 1: Block diagram of the AD-DA hardware board

Please follow the tasks described below:

(1) Set up the board with the following operating conditions:
- connect the board supply: ground plus a DC voltage in range [+5, +10] V
- put jumpers in position: CLK_INT, VREF_INT, VIN_OFFSET, plus anti-imaging jumper open (filter inactive), and anti-aliasing jumper open (filter inactive)
- set all 12 DIP switches on (ADC using its maximum resolution of 12 bits).

(2) Connect the output of the signal generator (FuGe) to the input V_{IN} of the board, and also to the channel 1 (CH1) input at the oscilloscope.
Plus connect the output V_{OUT} of the board to the channel 2 of the oscilloscope.

(3) Generate with the FuGe a sinusoidal signal x(t) with f_0=50 kHz and amplitude 2.0 V_{pp} . The dynamic range („Aussteuerbereich") of the ADC is about ca. 2.5 V_{pp} .

(4) Control the input (CH1) and ouput (CH2) signals in the oscilloscope. The ouput signal is discrete in both time and amplitude values.
How can you explain the delay between input and output signals?
Why is the output signal always slightly changing?

(5) Determine the sampling period T_s, and the corresponding sampling frequency F_s.
You can freeze the display of the oscilloscope (toggle between run/single measurement) to easy your observation.

(6) Lower now the frequency of V_{IN} to . f_0 = 1 kHz and keep the amplitude at 2.0 V_{pp}.
Then set the DIP switches one by one in off position, starting by the LSB and evolving towards the MSB.
Observe the changes in V_{OUT} and explain why they happen.
Set all 12 DIP switches in the ON position again.

(7) Change again the frequency of V_{IN} to . f_0 = 100 kHz and keep the amplitude at 2.0 V_{pp}.
Observe now the spectrum of the input signal V_{IN}.

Then next observe the spectrum of the output signal V_{OUT}. Which are the new frequency components of V_{OUT} in comparison to V_{IN} ?

The spectrum of V_{OUT} contains the original frequency of V_{IN}, plus copies of it (image frequencies) shifted around multiples of F_s.

Note down the frequency components (original plus images) in the frequency range from 0 Hz till 5 MHz. Verify the position of the image components compared to the multiples of F_s.

(8) Which other frequency of V_{IN} do you expect to produce the same output spectrum at V_{OUT}? Verify your expectation with a measurement.

Is the frequency value of V_{IN} that you set larger than Fs/2 ?

The effect you are observing here (that the original frequency of V_{IN} appears distorted at V_{OUT}) is called aliasing, and will be further discussed again a bit later in this lab.

(9) The DAC contains a zero-order-holder (ZOH), which is a filter taking each input value of the DAC and holding it constant until the next sample arrives.

In the time domain the response of the ZOH to a single impulse is a rectangular pulse with width Ts . Therefore the response of the ZOH in the frequency domain corresponds to a sinc shaped spectrum.

Where are the zero-crossings of the ZOH sinc shaped spectrum? Can you observe them in the spectrum of V_{OUT} ?

(10) Set again the DIP switches one by one in off position, starting by the LSB and observe this time the effect in the frequency domain.

Observe the new frequency components raising as the quantisation noise increases. The range between the maximum signal amplitude, and the maximum noise amplitude (in the frequency domain) is called SFDR (spurious free dynamic range).

Verify that the SFDR in the frequency range from [0…F_s/2] changes by 6dB per bit, as you change the resolution of V_{OUT} . You will only be able to observe this effect for the 8 MSBs, because the oscilloscope numerical calculation has a limited resolution of 8 bits.

The overall signal quality is measured with the signal to noise ratio (SNR). The SNR of V_{OUT} also changes with 6dB / bit used in the quantisation of V_{IN}.

Set all 12 DIP switches in the ON position again.

(11) Close now the jumper at the output of the DAC, setting the anti-imaging filter (passive RC) with a cut off frequency of f_c = 100 kHz (R = 50Ω, C = 33nF), and control the changes in the spectrum of V_{OUT} .

(12) Set now the frequency of V_{IN} to 900kHz, and observe V_{OUT} both in time and frequency domain.

As commented above the effect observed here is called aliasing and it implies the distortion of the frequency contents of the input signal being sampled, when these frequency contents are above Fs/2.

There are basically 2 ways to prevent aliasing. One is to select a higher sampling frequency (which is not always possible for a given hardware), and the other is to deploy an anti-aliasing filter (AAF).

The anti-aliasing filter is placed before the ADC and limits the bandwidth to the ADC input signal. In this board the anti-aliasing filter has a cut off frequency of f_c = 50 kHz.

Close now the jumper setting the anti-aliasing filter active, and control V_{OUT} in time and frequency domain.

(13) Lower again the frequency of V_{IN} to 100kHz, and observe V_{OUT} both with and without the anti-aliasing filter. Does the AAF have a significant effect for this input frequency?

Some further ideas if you still have time:

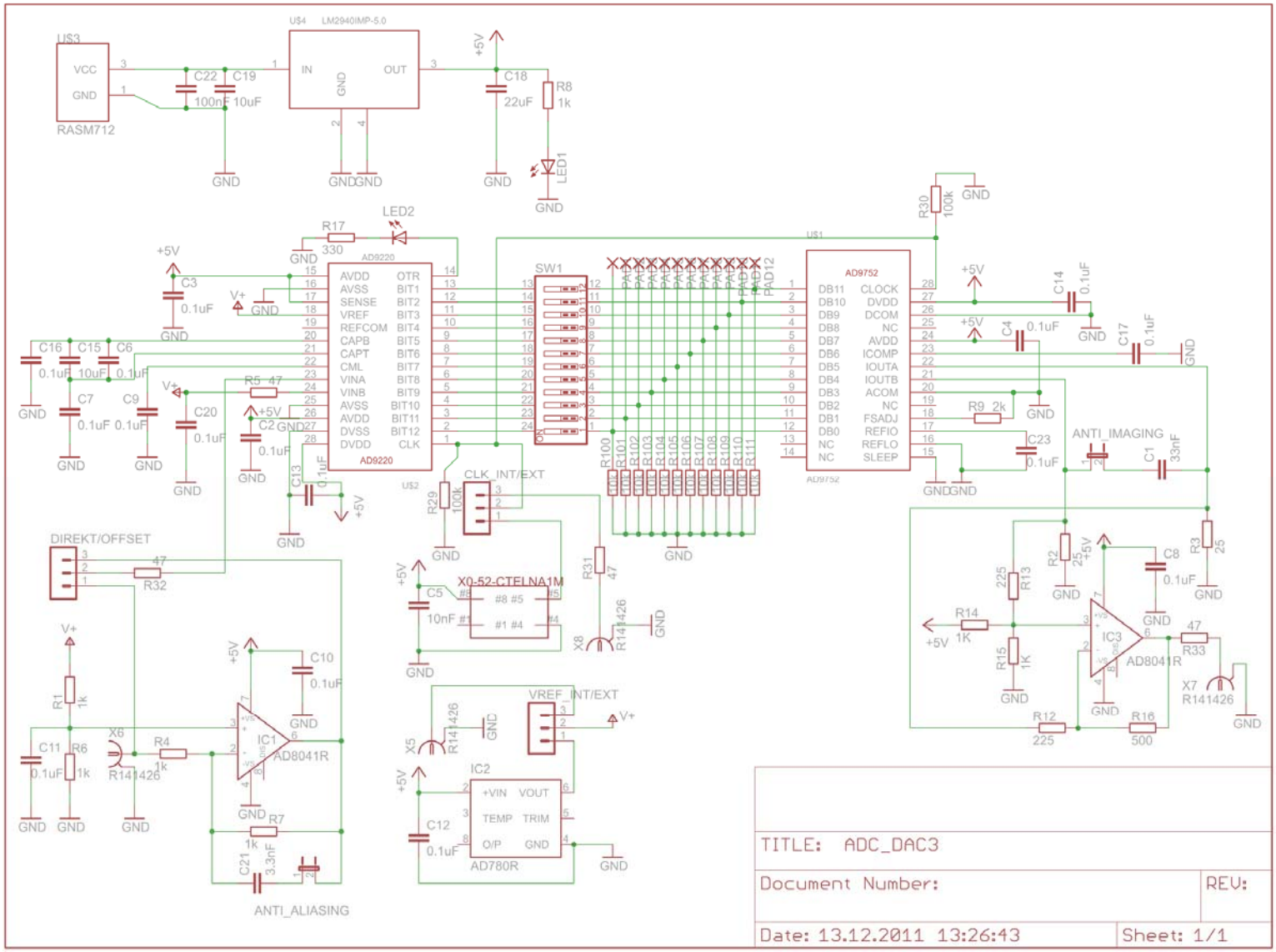
(14) The ADC has besides V_{IN} two further inputs, V_{REF} (reference voltage) and V_{CLOCK} (determining the sampling period).

What is V_{REF} needed for?
What is the influence of a clock jitter (clock period uncertainty) for the ADC performance?
You can study the ADC datasheet to check for answers.

(15) Keep the frequency of V_{IN} to 100kHz .
Open the jumpers of the anti-image and anti-aliasing filters (inactive position).

Set the jumper to CLK_EXT, and connect a second FuGe in the clock-input.

Start with a clock frequency of 1MHz and lower it towards 100kHz, while observing the influence at VOUT both in time and frequency domains.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C22
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C19
10uF
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IN
OUT
GND
+5V
C18
22uF
R8
1k
LED1
LED2
R17
330
AD9220
AVDD
AVSS
SENSE
VREF
REFCOM
CAPB
CAPT
CML
VINA
VINB
AVSS
AVDD
DVSS
DVDD
OTR
BIT1
BIT2
BIT3
BIT4
BIT5
BIT6
BIT7
BIT8
BIT9
BIT10
BIT11
BIT12
CLK
SW1
US1
AD9752
DB11
DB10
DB9
DB8
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
NC
CLOCK
DVDD
DCOM
AVDD
ICOMP
IOUTA
IOUTB
ACOM
FSADJ
REFIO
REFLO
SLEEP
R30
100k
C14
C4
C17
R9
2k
C23
C1
33nF
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US2
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R29
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C5
10nF
R31
47
X8
R141426
DIREKT/OFFSET
R32
R1
R2
R3
25
R13
225
C8
R14
1K
R15
IC3
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