

FINAL PROJECT SINGLE CYCLE CPU

In the final project we were asked to implement a single cycle processor in Verilog. For this I tried to create separate data and instruction memories and also a register file that works with a clock. I have also designed a program counter, ALU, control unit and multiplexers to choose the correct ALU output and also the PC input. Unfortunately, I did not have the time to truly connect these separate parts of the processor together and make them work as a unit. I believe if I had the time, these files would turn out to be a working single cycle CPU.

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