Abraham Gonzalez

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Education

***Ph.D.* — Electrical Engineering and Computer Science** Aug. 2018 - Present
University of California, Berkeley

***Bachelors of Science* — Electrical Engineering** Aug. 2014 - May 2018
The University of Texas at Austin
GPA - Overall 3.98/4.00 Major 3.98/4.00

Experience

Ph.D. Candidate Aug. 2018 - Present
ADEPT/SLICE Lab — Berkeley, CA

- Researching warehouse-scale computing, accelerators, microarchitecture, and architecture tooling.
- Co-lead of the Hyperscale SoC project focused on HW/SW co-design and accelerator enhancements for WSCs.
- Co-lead and main developer of the Chipyard SoC framework and FireSim FPGA-accel. simulation platform.
- Developer of BOOM, a Linux booting open-source RISC-V out-of-order core.
- Lead organizer for over 10+ tutorials/workshops with over 250+ combined attendees at top arch. conferences.
- Published research and tapeouts at top conferences including ISCA, ESSCIRC, and DAC.

System Infrastructure Intern Jun. 2021 - Jul. 2024
Google — Berkeley, CA

- Researched data analytics and RPC acceleration under Partha Ranganathan and Jichuan Chang.
- Collaborated with the Systems Research and System Infrastructure groups on data analytics characterization.
- Published data analytics characterization research at ISCA 2023.
- Open-sourced production RPC benchmark code with the Fleetbench benchmarking team.

BEAGLE: Heterogeneous Multi-Core Multi-Accelerator Chip in Intel 22FFL May 2019 - Sep. 2021
ADEPT Lab — Berkeley, CA

- Led tapeout and testing of first of it's kind heterogeneous multi-core multi-accelerator test chip using Chipyard.
- Coordinated interaction between Berkeley and Intel during physical design process.
- Streamlined Chipyard vendor IP integration and open-sourced newly created bringup collateral.
- Published working test chip at ESSCIRC 2021.

CPU Design Intern Jun. 2020 - Aug. 2020
Apple — Berkeley, CA

- Developed architecture tooling with the CPU infrastructure team under Si-En Chang.

Scalable Performance CPU Development Group Intern May 2018 - Aug. 2018
Intel — Austin, TX

- Built debugging methodologies for the microcontroller integration team in collaboration with firmware teams.

Microsystems Technology Lab Intern Jun. 2017 - Aug. 2017
Massachusetts Institute of Technology — Cambridge, MA

- Developed machine learning models to predict electroplating growth in RDL under Prof. Duane Boning.
- Presented final research poster at MITSRP showcase and SHPE National Conf. 2017 (awarded 2nd place).

Office Shared Graphics Explore Intern May 2016 - Aug. 2016
Microsoft — Redmond, WA

- Developed proof-of-concept "Sketchy Lines" feature in the Office suite using C++.
- Created a synchronized network of Arduino microcontrollers using HTTP requests for OneWeek hackathon.

UIM Driver Intern May 2015 - Aug. 2015
Qualcomm — San Diego, CA

- Designed software framework for smartcard interaction in C++/CLI and C++.
- Built a .NET application managing smartcards via CCID.

Skills

Hardware Experience: RISC-V, Chisel/Verilog/VHDL, ARM Assembly
Software Experience: C/C++/C#/CLI, Python/Bash, Make, Git, TensorFlow/PyTorch
Other Experience: AWS EC2, Google Cloud, Xilinx FPGAs, Cadence EDA tooling

Professional Leadership and Membership

Member of LAGSES (Fall 2018-Pres.)
Vice President (Spr. 2018), Corres. Secretary (Fall 2017), and member (Spr. 2016-Pres.) of HKN Honor Society
Academic Director (Fall 2016-Fall 2017), and member (Fall 2014-Pres.) of Society of Hispanic Professional Engineers

Accomplishments

UC Berkeley: Analog Devices Outstanding Designer (Spr. 2020), Berkeley Fellowship (Fall 2018), EECS Excellence Award (Fall 2018), GEM Fellowship (Spr. 2018)
UT Austin: Highest Honors (Spr. 2017), Distinguished College Scholar (Spr. 2017/2018), College Scholar (Spr. 2016), R. Rocca (Fall 2017), V. L. Hand Endowed (Fall 2016), and TI Diversity Scholarship (Fall 2015)