# Curriculum Vitae

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## Education

***Ph.D.* — Electrical Engineering and Computer Science** Aug. 2018 - Present
University of California, Berkeley

***Bachelors of Science* — Electrical Engineering** Aug. 2014 - May 2018
The University of Texas at Austin
GPA — Overall: 3.98/4.00 Major: 3.98/4.00

## Relevant Coursework

***Graduate School*** — Graduate Computer Architecture, Computer Architecture for Security, Hardware for Machine Learning, Machine Learning Systems, Topics in Circuit Design: Tapeouts, Topics in Computer Systems: OS.
***Undergraduate School*** — Computer Architecture, Digital Systems Design Using HDL, Embedded Systems Design Lab, Real-time Operating Systems, Digital Logic Design, Software Design I & II, Algorithms, and Honors Engineering Design I & II, Electric Circuits Lab, Solid State Electronic Devices, Electromagnetic Engineering, Circuit Theory, Intro to Probability, and Engineering Communication.

## Experience

***Ph.D. Candidate*** Aug. 2018 - Present
ADEPT/SLICE Lab — Berkeley, CA

- Researching warehouse-scale computing, accelerators, microarchitecture, and architecture tooling.
- Co-lead of the Hyperscale SoC project focused on HW/SW co-design and accelerator enhancements for WSCs.
- Co-lead and main developer of the Chipyard SoC framework.
- Co-lead and main developer of the FireSim FPGA-accelerated simulation platform.
- Developer of BOOM, a Linux booting open-source RISC-V out-of-order core.
- Lead organizer for over 10+ tutorials/workshops with over 250+ combined attendees at top arch. conferences.
- Published research and tapeouts at top conferences including ISCA, ESSCIRC, and DAC.

***System Infrastructure Intern*** Jun. 2021 - Jul. 2024
Google — Berkeley, CA

- Researched data analytics and RPC acceleration under Partha Ranganathan and Jichuan Chang.
- Collaborated with the Systems Research and System Infrastructure groups on data analytics characterization.
- Published data analytics characterization research at ISCA 2023.
- Open-sourced production RPC benchmark code with the Fleetbench benchmarking team.

***BEAGLE: Heterogeneous Multi-Core Multi-Accelerator Chip in Intel 22FFL*** May 2019 - Sep. 2021
ADEPT Lab — Berkeley, CA

- Led tapeout and testing of first of it's kind heterogeneous multi-core multi-accelerator test chip using Chipyard.
- Coordinated interaction between Berkeley and Intel during physical design process.
- Streamlined Chipyard vendor IP integration and open-sourced newly created bringup collateral.
- Published working test chip at ESSCIRC 2021.
- SoC Components: In-Order Rocket core with systolic array accelerator, Out-of-Order BOOM core with vector accelerator, shared L2, independent clock domains, multiple IOs (GPIO, SPI, I2C, UART, SerDes).

***CPU Design Intern*** Jun. 2020 - Aug. 2020
Apple — Berkeley, CA

- Developed architecture tooling with the CPU infrastructure team under Si-En Chang.

***Scalable Performance CPU Development Group Intern*** May 2018 - Aug. 2018
Intel — Austin, TX

- Worked on debugging tools for microcontroller integration team.
- Helped setup infrastructure between firmware team and microcontroller integration team to speed up work.

***Microsystems Technology Lab Intern*** Jun. 2017 - Aug. 2017
Massachusetts Institute of Technology — Cambridge, MA

- Researched variations in electroplating growth in redistribution layers under Prof. Duane Boning.
- Designed various neural networks and machine learning models for electroplating growth using Tensorflow.
- Presented final research poster at MITSRP summer-end presentations and participated in MITSRP workshops.
- Awarded 2nd best poster for research at the SHPE National Conference 2017.

***Printing Electronics Research Assistant*** Jan. 2017 - Jun. 2017
The University of Texas at Austin — Austin, TX
- Researched and fabricated printed antennas under the supervision of Prof. Ray Chen.
- Printed and tested fixed PAA antennas on Kapton with various nano-particle inks.

***QCA Research Assistant*** May 2015 - Aug. 2016
The University of Texas at Austin — Austin, TX
- Researched and designed Quantum Cellular Automata (QCA) circuitry with Prof. Earl Swartzlander.
- Optimized QCA implementations of the Carry-Lookahead and Conditional Sum adder through QCA Designer.
- Collaborated with Prof. Swartzlander on results and improvements to QCA circuit designs and layouts.

***Office Shared Graphics Explore Intern*** May 2016 - Aug. 2016
Microsoft — Redmond, WA
- Developed proof-of-concept "Sketchy Lines" feature in the Office suite using C++.
- Investigated new feature sets with other Microsoft Program Managers and customers.
- Created a synchronized network of Arduino microcontrollers using HTTP requests for OneWeek hackathon.
- Collaborated with senior engineers and engineers on software design and implementation.

***UIM Driver Intern*** May 2015 - Aug. 2015
Qualcomm — San Diego, CA
- Designed software framework for smartcard interaction in C++/CLI and C++.
- Integrated designed framework into a .NET application managing smartcards via CCID by utilizing APDU transmission/logging; file system viewing; file data parsing/manipulation; and smartcard reader management.
- Communicated with engineers on software design and implementation.
- Created gesture controlled car with Particle Core for Hack-Mobile hackathon.

***Electronic Cooling Research Lab Assistant*** Jun. 2012
Villanova University — Villanova, PA
- Participated in constructing and remodeling a cooling test mechanism under Prof. Alfonso Ortega.
- Investigated techniques to cool spherical devices within a wind tunnel.
- Communicated with Ph.D. students and Masters students.

**Selected Conferences and Presentations**

***ISCA21-23, MICRO19/21-22/24, ASPLOS20/22-23, and HPCA23 Conferences*** Oct. 2019 - Present
University of California, Berkeley — Various locations
- Lead organizer for over 10+ tutorials/workshops with over 250+ combined attendees.
- Presented the Chipyard SoC framework, FireSim FPGA-accelerated simulation platform, and Berkeley Out-of-Order Machine (BOOM) mainly to academics.
- Hosted the first FireSim and Chipyard User and Developer Workshop at ASPLOS 2023.

***Latch-Up Conferences*** May 2019, Apr. 2023
University of California, Berkeley — Portland, OR and Santa Barbara, CA
- Presented the Chipyard SoC framework, FireSim FPGA-accelerated simulation platform, and Berkeley Out-of-Order Machine (BOOM) mainly to open-source enthusiasts.

***RISC-V Summit*** Dec. 2019
University of California, Berkeley — San Jose, CA
- Presented the Chipyard SoC framework and Berkeley Out-of-Order Machine (BOOM) mainly to industry.

***ACM Richard Tapia Celebration of Diversity in Computing Conference*** Sept. 2018
University of California, Berkeley — Orlando, FL
- Attended multiple workshops on open source software, ethics in AI, networking, and diversity.
- Participated as a UC Berkeley Scholar and FLIP Alliance student.

***Society of Hispanic Professional Engineers National Conference*** Nov. 2017
University of Texas at Austin — Kansas City, MO
- Research Presented: A Machine Learning Approach to Modeling Electroplating Process Variations in IC Redistribution Layers.
- Participated and won the 2nd place award in the Engineering Science Symposium (ESS) Poster Competition.
- Selected as 1 of about 40 students nationally for ESS Poster Competition.
- Attended Engineering Science Symposium Oral Presentations and workshops.

***Supercomputing Conference - SC15*** Nov. 2015
Tezzaron Semiconductor — Austin, TX
- Worked with the Tezzaron company booth as an usher during exhibit fair.
- Networked with other high performance computing (HPC) companies.

***Qualcomm DECA Conference*** Jan. 2015 - Feb. 2015

Qualcomm — San Diego, CA

- Developed professional and social skills through mock interviews and workshops.
- Participated and won Qualcomm QHack hackaton.
- Selected as 1 of 51 students nationally for DECA Conference.

***LEADership, Education and Development Conference*** Jul. 2013

Villanova University — Villanova, PA

- Participated in laboratories in the Chemical Engineering Department.
- Leader of Chemical Engineering Sub-group.
- Developed an accessible and low-cost filtration system for third world countries.
- Selected as 1 of 30 students nationally for LEAD Engineering SEI.

## Selected Publications and Projects

***FireAxe: Partitioned FPGA-Accelerated Simulation of Large-Scale RTL Designs***

- Joonho Whangbo, Edwin Lim, Chengyi Lux Zhang, Kevin Anderson, Abraham Gonzalez, Raghav Gupta, Nivedha Krishnakumar, Sagar Karandikar, Borivoje Nikolic, Yakun Sophia Shao, Krste Asanovic, "FireAxe: Partitioned FPGA-Accelerated Simulation of Large-Scale RTL Designs", 2024 ACM/IEEE 51st Annual International Symposium on Computer Architecture (ISCA), Buenos Aires, Argentina, June 2024.

***Profiling Hyperscale Big Data Processing***

- Abraham Gonzalez, Aasheesh Kolli, Samira Khan, Sihang Liu, Vidushi Dadu, Sagar Karandikar, Jichuan Chang, Krste Asanovic, Parthasarathy Ranganathan, "Profiling Hyperscale Big Data Processing", 2023 ACM/IEEE 51st Annual International Symposium on Computer Architecture (ISCA), Orlando, FL, USA, June 2023.

***A 16mm$^2$ 106.1 GOPS/W Heterogeneous RISC-V Multi-Core Multi-Accelerator SoC in Low-Power 22nm FinFET***

- Abraham Gonzalez, Jerry Zhao, Ben Korpan, Hasan Genc, Colin Schmidt, John Wright, Ayan Biswas, Alon Amid, Farhana Sheikh, Anton Sorokin, Sirisha Kale, Mani Yalamanchi, Ramya Yarlagadda, Mark Flannigan, Larry Abramowitz, Elad Alon, Yakun Sophia Shao, Krste Asanovic, and Bora Nikolic, "A 16mm$^2$ 106.1 GOPS/W Heterogeneous RISC-V Multi-Core Multi-Accelerator SoC in Low-Power 22nm FinFET", In proceedings of 2021 IEEE European Solid State Circuits Conference (ESSCIRC 2021), Virtual Event, September 2021.

***COBRA: A Framework for Evaluating Compositions of Hardware Branch Predictors***

- Jerry Zhao, Abraham Gonzalez, Alon Amid, Sagar Karandikar, and Krste Asanovic, "COBRA: A Framework for Evaluating Compositions of Hardware Branch Predictors", In proceedings of 2021 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS 2021), Virtual Event, March 2021.

***Chipyard - An Integrated SoC Research and Implementation Environment***

- Alon Amid, David Biancolin, Abraham Gonzalez, Daniel Grubb, Sagar Karandikar, Harrison Liew, Albert Magyar, Howard Mao, Albert Ou, Nathan Pemberton, Paul Rigge, Colin Schmidt, John Wright, Jerry Zhao, Yakun Sophia Shao, Krste Asanovic, and Bora Nikolic, "Invited: Chipyard - An Integrated SoC Research and Implementation Environment", In proceedings of 57th ACM/IEEE Design Automation Conference (DAC 2020), San Francisco, CA, USA, July 2020.

***Chipyard: Integrated Design, Simulation, and Implementation Framework for Custom SoCs***

- Alon Amid, David Biancolin, Abraham Gonzalez, Daniel Grubb, Sagar Karandikar, Harrison Liew, Albert Magyar, Howard Mao, Albert Ou, Nathan Pemberton, Paul Rigge, Colin Schmidt, John Wright, Jerry Zhao, Yakun Sophia Shao, Krste Asanovic, and Bora Nikolic, "Chipyard: Integrated Design, Simulation, and Implementation Framework for Custom SoCs", IEEE Micro, vol. 40, no. 4, pp. 10-21, (Special Issue on Agile and Open-Source Hardware), July-August 2020.

***SonicBOOM: The 3rd Generation Berkeley Out-of-Order Machine***

- Jerry Zhao, Ben Korpan, Abraham Gonzalez, and Krste Asanovic, "SonicBOOM: The 3rd Generation Berkeley Out-of-Order Machine", 4th Workshop on Computer Architecture Research with RISC-V (CARRV 2020), Virtual Event, May 2020.

***Replicating and Mitigating Spectre Attacks on an Open Source RISC-V Microarchitecture***

- Abraham Gonzalez, Ben Korpan, Jerry Zhao, Ed Younis, and Krste Asanovic, "Replicating and Mitigating Spectre Attacks on an Open Source RISC-V Microarchitecture", 3rd Workshop on Computer Architecture Research with RISC-V (CARRV 2019), Phoenix, AZ, USA, June 2019.

***Enhancing an Out-of-Order Processor Simulator for Cloud Applications***

- Designed and developed new software data-structures for emulating simultaneous multithreading on ZSim.
- Worked with an out-of-order processor pipeline to introduce new hardware scheduling schemes to ensure quality of service for latency critical tasks.
- Presented a poster of final results at The University of Texas Electrical Engineering Spring Open House.

***Bounce Music App for Android***

- Designed and developed an app in which a user can stream music to multiple phones within the same vicinity.
- Used Spotify API to access and display a catalog of music and sockets for basic connection capabilities.

## Skills

***Programming Languages*** —

- Highly Proficient: Chisel, Verilog, Make, Git, RISC-V Assembly, C, C++, C++/CLI, Python, Bash, and TensorFlow/PyTorch.
- Proficient: VHDL, TCL, ARM Assembly, LC-3 Assembly, Android Java, C#, and Subversion.

***Embedded Systems*** — Tiva Launchpad, Arduino, SparkFun, and Particle Core microcontrollers.
***Electrical Equipment*** — Soldering, oscilloscopes, logic analyzers, and multimeters.
***Other*** — AWS EC2 (F1 platform), Google Cloud, Xilinx Virtex/UltraScale+ FPGAs, and Cadence EDA tooling.

## Professional Leadership and Membership

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| ***Member*** — Latinx Association of Graduate Students in Engineering and Science | Fall 2018 - Present |
| ***Vice President*** — Eta Kappa Nu Electrical Engineering Honor Society | Fall 2017 - Spring 2018 |
| ***Corresponding Secretary*** — Eta Kappa Nu Electrical Engineering Honor Society | Summer 2017 - Fall 2017 |
| ***Member*** — Eta Kappa Nu Electrical Engineering Honor Society | Spring 2016 - Present |
| ***Member*** — Institute of Electrical and Electronic Engineers | Fall 2014 - Present |
| ***Member*** — Society of Hispanic Professional Engineers (SHPE) | Fall 2014 - Present |
| ***Pi Tutor*** — Equal Opportunity in Engineering (EOE) | Fall 2015, Fall 2017 |
| ***Academic Director*** — Society of Hispanic Professional Engineers | Summer 2016 - Summer 2017 |
| ***Organizing Committee Member*** — 3 Day Startup Austin | Fall 2014 - Fall 2015 |
| ***Participant*** — 3 Day Startup Austin | Fall 2014 |

## Honors and Awards

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| ***Analog Devices Outstanding Engineer Award*** — University of Califonia at Berkeley | Spring 2020 |
| ***EECS Excellence Award*** — University of Califonia at Berkeley | Fall 2018 |
| ***Berkeley Fellowship for Graduate Study*** — University of Califonia at Berkeley | Fall 2018 |
| ***GEM Fellowship Recipient*** — GEM | Spring 2018 |
| ***Honorable Mention*** — NSF GRFP | Spring 2018 |
| ***Highest Honors*** — The University of Texas at Austin | Spring 2018 |
| ***Distinguished College Scholar*** — The University of Texas at Austin | Spring 2018 |
| ***Academic Leader Hall of Fame Inductee*** — Equal Opportunity in Engineering Program | Spring 2018 |
| ***Roberto Rocca Scholarship Recipient*** — Tenaris | Fall 2017 |
| ***Second-Place Award Winner*** — SHPE National Conference Poster Competition | Fall 2017 |
| ***Distinguished College Scholar*** — The University of Texas at Austin | Spring 2017 |
| ***Victor L. Hand Scholarship Recipient*** — Victor L. Hand Endowed Scholarship Fund | Fall 2016 |
| ***College Scholar*** — The University of Texas at Austin | Spring 2016 |
| ***Diversity Scholarship Recipient*** — Texas Instruments | Fall 2015 |
| ***Freshman Academic Excellence Award Winner*** — EOE and SHPE | Spring 2015 |