

# Accélérateurs matériels

## TP n°1

Division avec contrainte sur le débit

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## Choix des architectures

On souhaite réaliser une division (euclidienne) signée 12bits÷12bits (c'est-à-dire que les 2 opérandes sont sur 12 bits en code complément à 2) en calculant quotient et reste à un débit de 100 MHz (1 résultat à chaque période de 100 MHz).

Architecture division (12bits÷12bits)	Contrainte (période)	WNS	LUT & DFF
Parallèle avec / et rem en VHDL	10 ns	-18 ns	380 LUT
	30 ns	- 0,086 ns	381 LUT
Division signée sans restauration (décrite en VHDL par A. Exertier)	10 ns	-16,582 ns	199 LUT
	30 ns	1,54 ns	198 LUT

En analysant le tableau, je décide d'utiliser la solution "Division signée sans restauration".

Première Solution : Parallèle avec / et rem en VHDL (période 10 ns) : WNS négatif

Première Solution : Parallèle avec / et rem en VHDL (période 30 ns) : WNS négatif mais proche de zéro. D'autre part, le nombre de LUT et de DFF est élevé comparé à la solution numéro 2.

Seconde solution : Division signée sans restauration (décrite en VHDL par Madame EXERTIER) (10 ns) : WNS négatif

Seconde solution : Division signée sans restauration (décrite en VHDL par Madame EXERTIER) (30 ns) : WNS positif et le nombre de LUT est inférieur à la première solution.

Je choisis d'utiliser cette dernière pour réaliser mon architecture globale.

#### Première architecture : sans PLL

La première architecture doit calculer le quotient et le reste à un débit de 100 MHz. Je dois obtenir 1 résultat à chaque période de 100 MHz.

Néanmoins, l'architecture "Division signée sans restauration" possède un WNS positif lorsque nous mettons une contrainte de 30 ns. Le bloc calculus fournit un résultat à chaque période de 100 MHz. Pour satisfaire la contrainte ( $30 \text{ ns} / 10 \text{ ns} = 3$ ) nous devons mettre en parallèle 3 architectures "Division signée sans restauration".

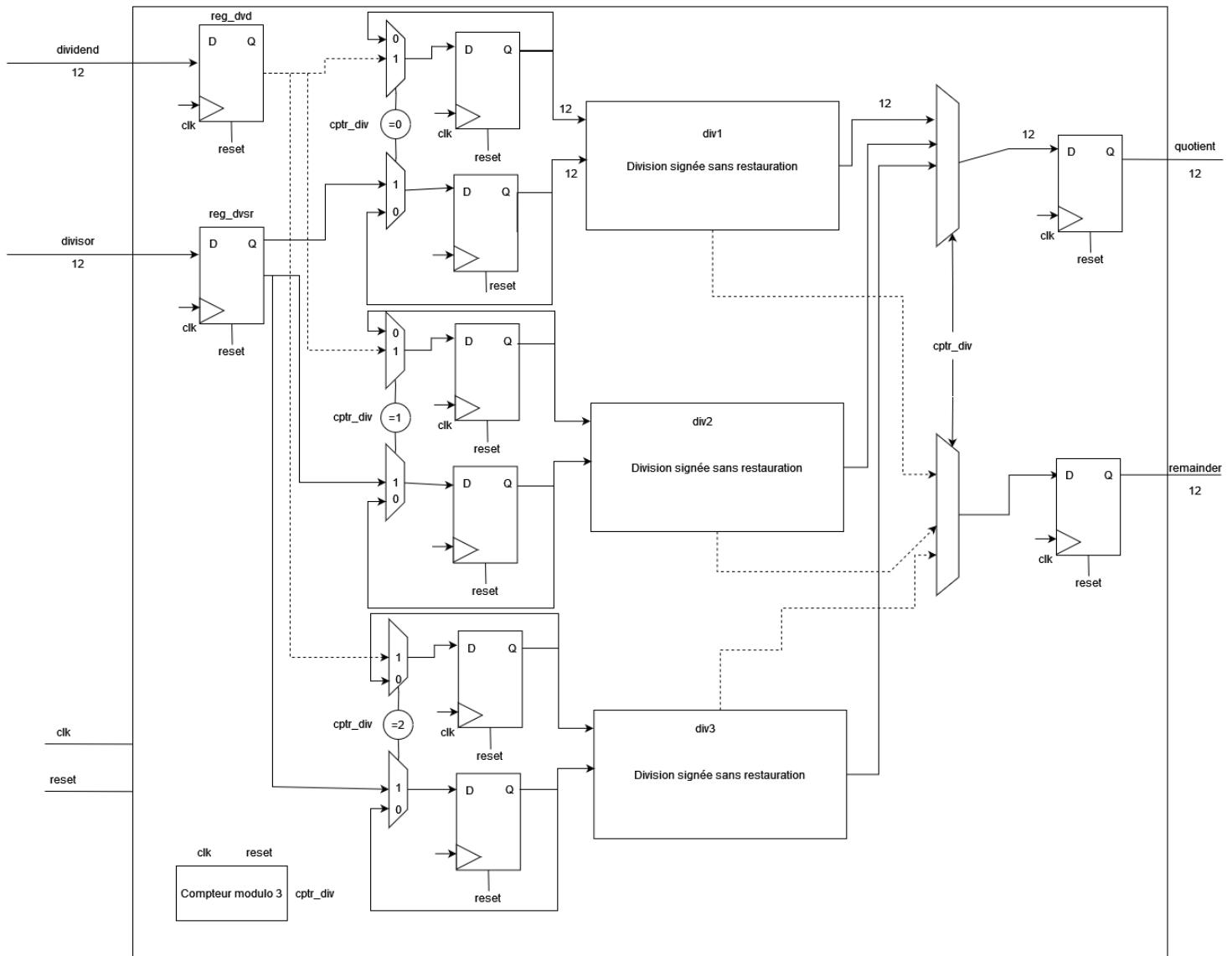
Je réfléchis à une architecture composée de 3 blocs calculus (Division signée sans restauration). Cette architecture utilise une horloge.

#### Explication de l'architecture :

Je positionne deux registres de 12 bits en entrée de l'architecture. Le premier registre récupère et mémorise pendant une période d'horloge (clk) le signal d'entrée dividend. Le second registre récupère et mémorise pendant une période d'horloge (clk) le signal d'entrée divisor.

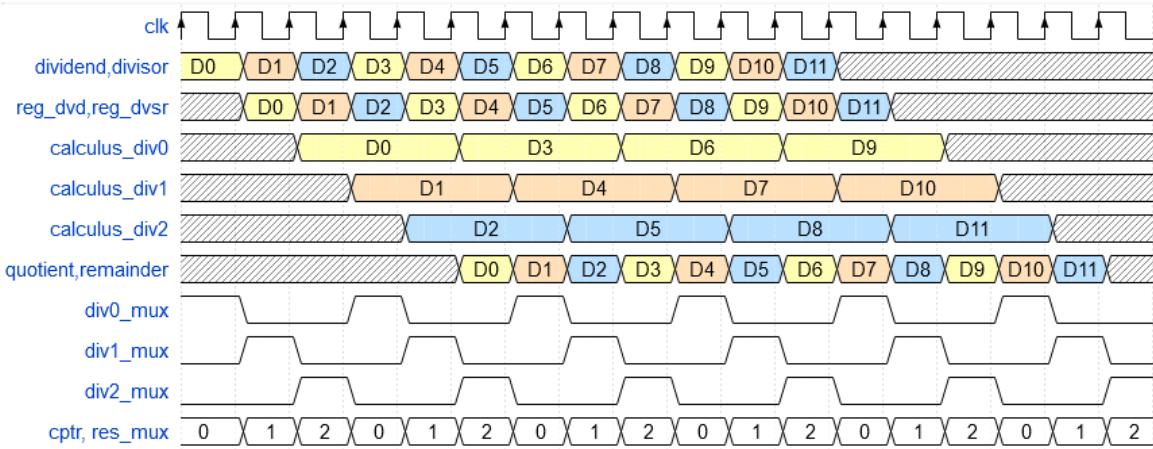
Puis je positionne trois blocs calculus en parallèle. Pour gérer l'envoie de la donnée dans le premier bloc, j'utilise un multiplexeur commandé par un compteur modulo 3 (cptr\_div) et un registre qui mémorise ou reçoit une nouvelle donnée. Ainsi, il y a un multiplexeur et un registre pour le signal dividend et le signal divisor par bloc. Pour récupérer la valeur du quotient et remainder de chaque bloc de calculus je mets un multiplexeur commandé par le compteur modulo 3 (cptr\_div).

J'obtiens l'architecture suivante :



Pour éviter de surcharger mon architecture, certaines flèches sont en pointillés tandis que d'autres flèches sont en trait plein. Toutes les DFFs utilisent le signal clk et le signal reset.

Je réalise le chronogramme suivant :



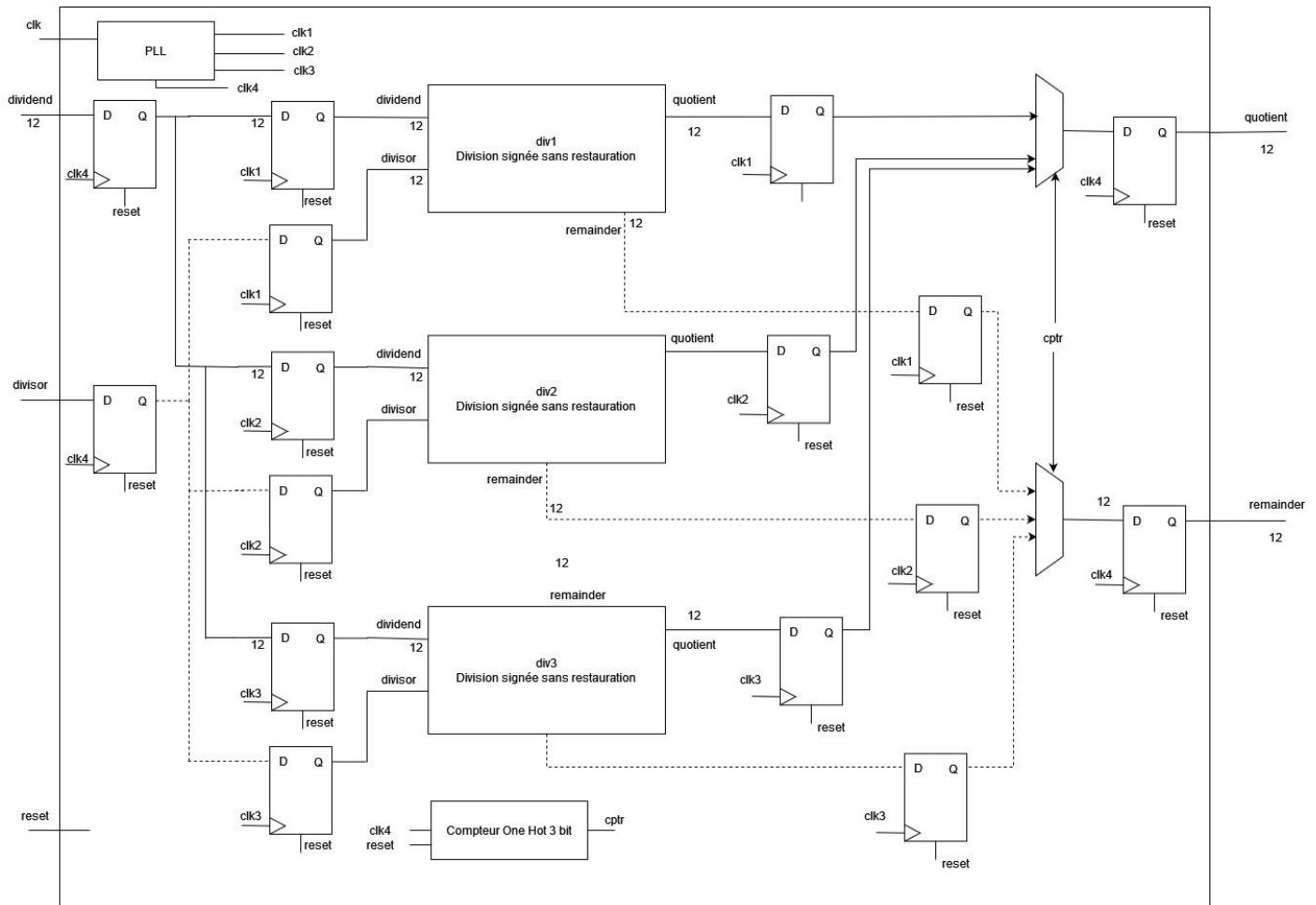
### Séquencement de la donnée :

Soit une donnée  $D_i$  avec  $i$  appartenant à l'intervalle  $[0, 11]$ . Lorsque la donnée est positionnée sur le port dividend et divisor au front d'horloge suivant la donnée  $D_i$  se retrouvent dans le registre `reg_dvd` et `reg_dvsr` respectivement. Au coup d'horloge suivant la donnée est transmise au `calculus`. En fonction du compteur, la donnée sera envoyée au bloc `division 1` ou au bloc `division 2` ou au bloc `division 3`. Les registres se trouvant avant le bloc viennent maintenir la donnée pendant 3 cycles d'horloges.

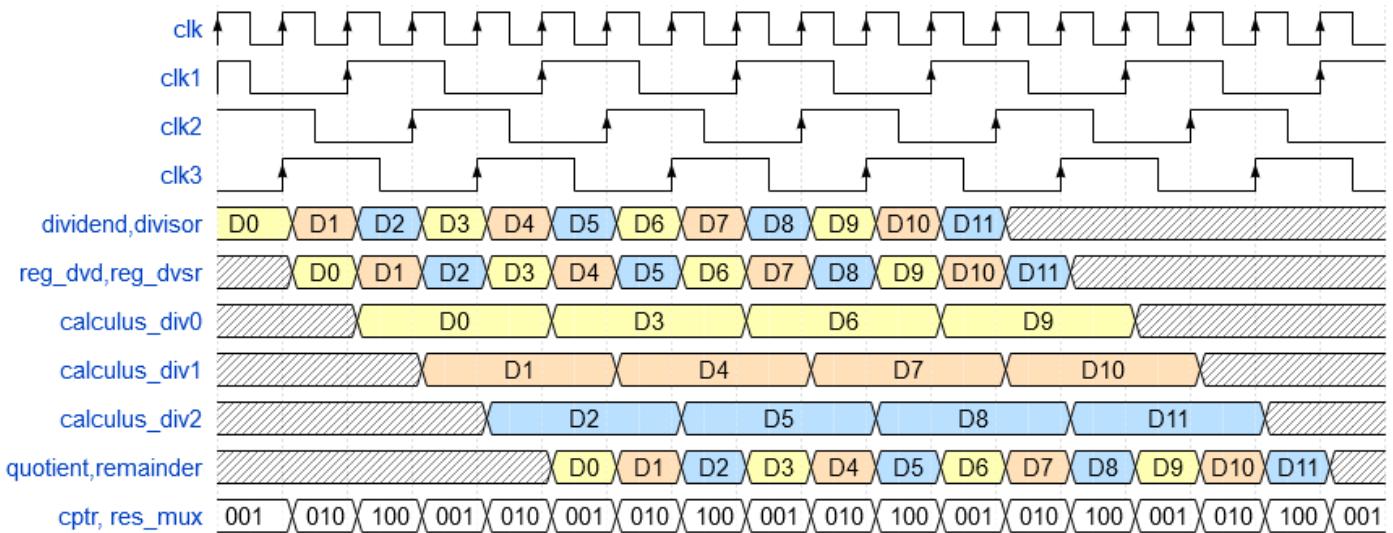
Finalement, nous obtenons une donnée pertinente au bout de 5 cycles d'horloges.

## Seconde architecture : avec PLL

Il est possible de réaliser une architecture n'utilisant pas de multiplexeur en entrée pour choisir quel calcul utiliser. Pour cela, j'utilise une PLL. La PLL va générer trois signaux clk1, clk2 et clk3. Ces signaux d'horloge iront sur chaque registre. La clk1 va cadencer le registre dividend et divisor du premier bloc de calcul, la clk2 va cadencer le registre dividend et divisor du deuxième bloc de calcul et la clk3 va cadencer le registre dividend et divisor du troisième bloc de calcul. La fréquence de clk1, clk2 et clk3 devra être égale à 33.333 MHz.



Je réalise le chronogramme suivant :



Les horloges sont déphasées, ce qui permet d'activer les registres sur le front montant des horloges sur lesquelles ils sont cadencés.

Dans les deux cas, je devrais octroyer un multicycle de 3. D'autre part, les ressources sont alors égales à  $3 \times 198$  LUT = 594 LUT.

## Architecture n°1 (sans PLL)

### Analyse du rapport de synthèse

Dans cette partie, nous allons effectuer une analyse du rapport de synthèse.

Report Check Netlist:

	Item	Errors	Warnings	Status	Description	
1	multi_driven_nets	0	0	Passed	Multi driven nets	

Vivado informe qu'il n'y a aucun court-circuit.

```
WARNING: [Designutils 20-1567] Use of 'set_multicycle_path' with '-hold' is not supported by synthesis. The constraint will not be passed to synthesis.  
[/user/didouha/E4/P3/SEI4301A/TP1/tp1/tp1/impl/nexys4ddr.xdc:6]
```

Vivado informe qu'il ne pourra pas appliquer le multicycle avec comme paramètre Hold lors de la synthèse.

---

Start RTL Component Statistics

---

Detailed RTL Component Info :

----Adders :

```
    3 Input    13 Bit      Adders := 39  
    2 Input    12 Bit      Adders := 3  
    2 Input     2 Bit      Adders := 1
```

----Registers :

```
        12 Bit      Registers := 10  
        2 Bit      Registers := 1
```

----Muxes :

```
    2 Input    13 Bit      Muxes := 48  
    2 Input    12 Bit      Muxes := 3  
    4 Input    12 Bit      Muxes := 2  
    2 Input     2 Bit      Muxes := 1  
    2 Input     1 Bit      Muxes := 39
```

---

Finished RTL Component Statistics

---

Vivado informe qu'il a reconnu 39 additionneurs de nombre sur 13 bits.

Mais également 3 additionneurs de nombres sur 12 bits et un additionneur de nombres sur 2 bits.

Report Cell Usage:		
	Cell	Count
1	BUFG	1
2	CARRY4	165
3	LUT1	36
4	LUT2	149
5	LUT3	34
6	LUT4	370
7	LUT5	19
8	LUT6	79
9	FDCE	122
10	IBUF	26
11	OBUF	24

Il n'y a aucun latch.

## Relevé des ressources

### 1. Slice Logic

-----

Site Type	Used	Fixed	Prohibited	Available	Util%
<b>Slice LUTs</b>	615	0	0	63400	0.97
LUT as Logic	615	0	0	63400	0.97
LUT as Memory	0	0	0	19000	0.00
<b>Slice Registers</b>	122	0	0	126800	0.10
Register as Flip Flop	122	0	0	126800	0.10
Register as Latch	0	0	0	126800	0.00
F7 Muxes	0	0	0	31700	0.00
F8 Muxes	0	0	0	15850	0.00

### 1.1 Summary of Registers by Type

---

Total	Clock Enable	Synchronous	Asynchronous
0	-	-	-
0	-	-	Set
0	-	-	Reset
0	-	Set	-
0	-	Reset	-
0	Yes	-	-
0	Yes	-	Set
122	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-

### 2. Slice Logic Distribution

---

Site Type	Used	Fixed	Prohibited	Available	Util%
<b>Slice</b>	208	0	0	15850	1.31
SLICEL	142	0			
SLICEM	66	0			
LUT as Logic	615	0	0	63400	0.97
using O5 output only	36				
using O6 output only	543				
using O5 and O6	36				
LUT as Memory	0	0	0	19000	0.00
LUT as Distributed RAM	0	0			
LUT as Shift Register	0	0			
Slice Registers	122	0	0	126800	0.10
Register driven from within the Slice	24				
Register driven from outside the Slice	98				
LUT in front of the register is unused	33				
LUT in front of the register is used	65				
Unique Control Sets	4		0	15850	0.03

\* \* Note: Available Control Sets calculated as Slice \* 1, Review the Control Sets Report for more information regarding control sets.

#### Relevé des ressources :

- 208 slices
- 615 LUTS
- 122 DFF

Il y a 198 LUT par division. Il y a trois blocs de division : 594 LUTs. Or notre architecture possède 615 LUTs ce qui est légèrement supérieur à 594 LUTs. Cela semble cohérent.

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### 3. Memory

-----

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	135	0.00
RAMB36/FIFO*	0	0	0	135	0.00
RAMB18	0	0	0	270	0.00

### 4. DSP

-----

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	0	0	0	240	0.00

### 5. IO and GT Specific

-----

Site Type	Used	Fixed	Prohibited	Available	Util%
Bonded IOB	50	0	0	210	23.81
IOB Master Pads	24				
IOB Slave Pads	24				
Bonded IPADS	0	0	0	2	0.00
PHY_CONTROL	0	0	0	6	0.00
PHASER_REF	0	0	0	6	0.00
OUT_FIFO	0	0	0	24	0.00
IN_FIFO	0	0	0	24	0.00
IDELAYCTRL	0	0	0	6	0.00
IBUFDS	0	0	0	202	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	0	24	0.00
PHASER_IN/PHASER_IN_PHY	0	0	0	24	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	0	300	0.00
ILOGIC	0	0	0	210	0.00
OLOGIC	0	0	0	210	0.00

### 6. Clocking

-----

Site Type	Used	Fixed	Prohibited	Available	Util%
BUFGCTRL	1	0	0	32	3.13
BUFIO	0	0	0	24	0.00
MMCME2_ADV	0	0	0	6	0.00
PLLE2_ADV	0	0	0	6	0.00
BUFMRCE	0	0	0	12	0.00
BUFHCE	0	0	0	96	0.00
BUFR	0	0	0	24	0.00

### Relevé des ressources :

- 0 block RAM
- 0 DSP
- 1 arbre d'horloge (BUFGCTRL)
- 0 PLL

## Simulation avant synthèse

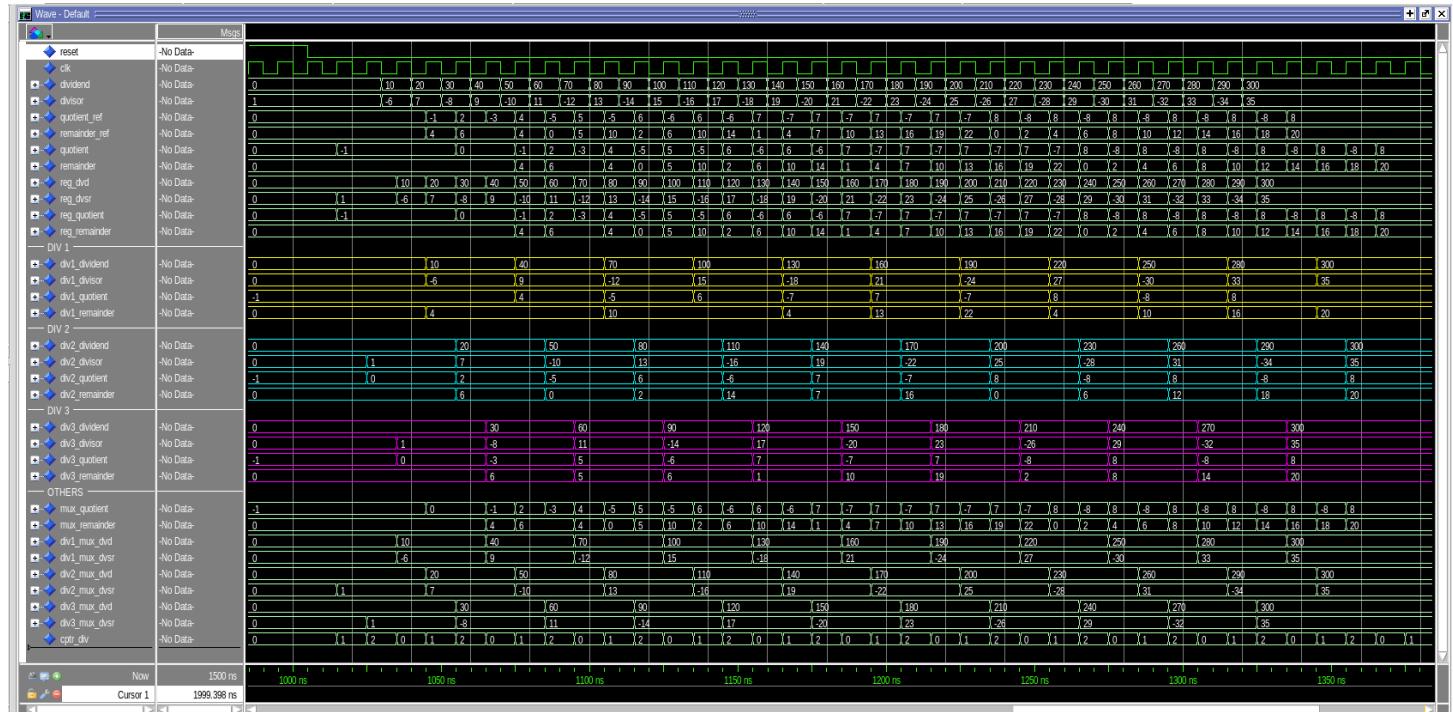
La latence de cette architecture est égale à 5 périodes de l'horloge à 100 MHz.

Nous devons prendre en compte la latence du calculus qui est égale à 3 périodes d'horloges.

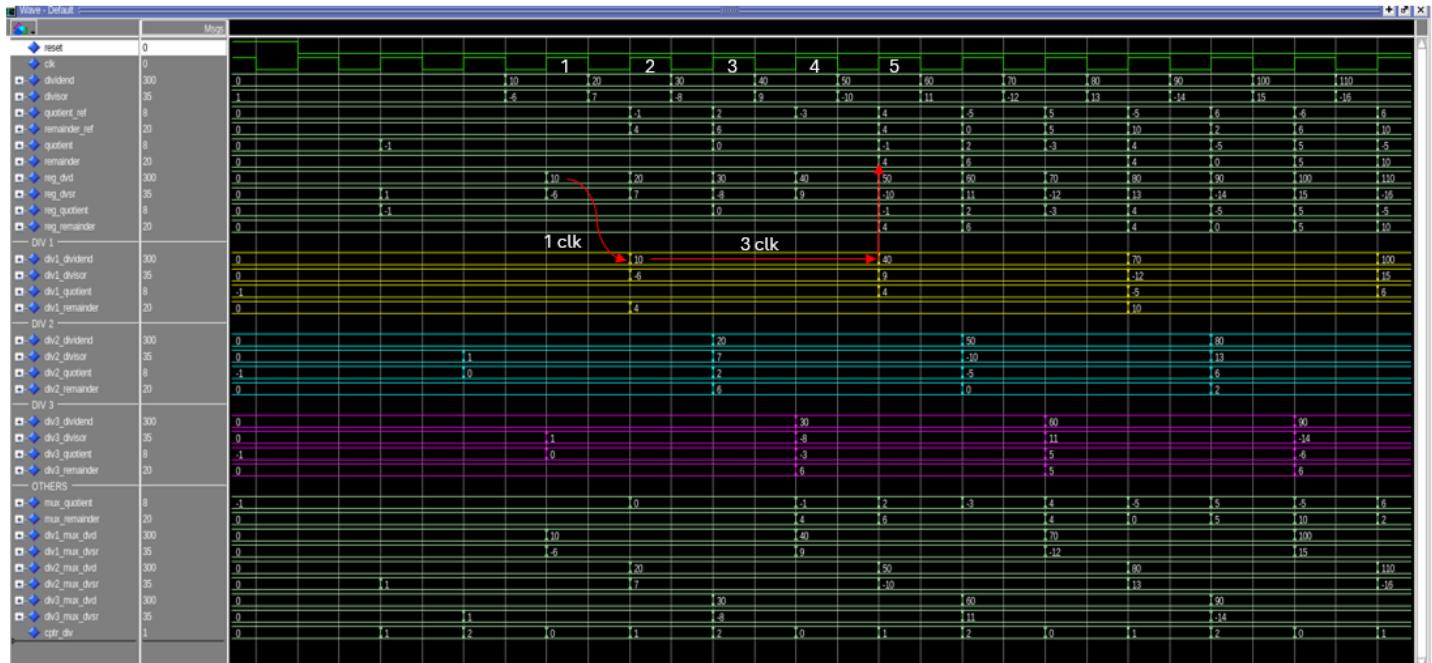
J'obtiens la vue globale pour une simulation comportementale avant synthèse.

### Behavioral Simulation :

#### Vue Globale :



Regardons en détail le séquencement de notre architecture :



La donnée D1 du "dividend" et du "divisor" sont positionnés sur front descendant de l'horloge clk. Les registres "reg\_dvd" et "reg\_dvsr" sont mis à jour au moment du front montant de l'horloge clk. Ainsi, les registres "reg\_dvd" et "reg\_dvsr" mémorisent la donnée D1.

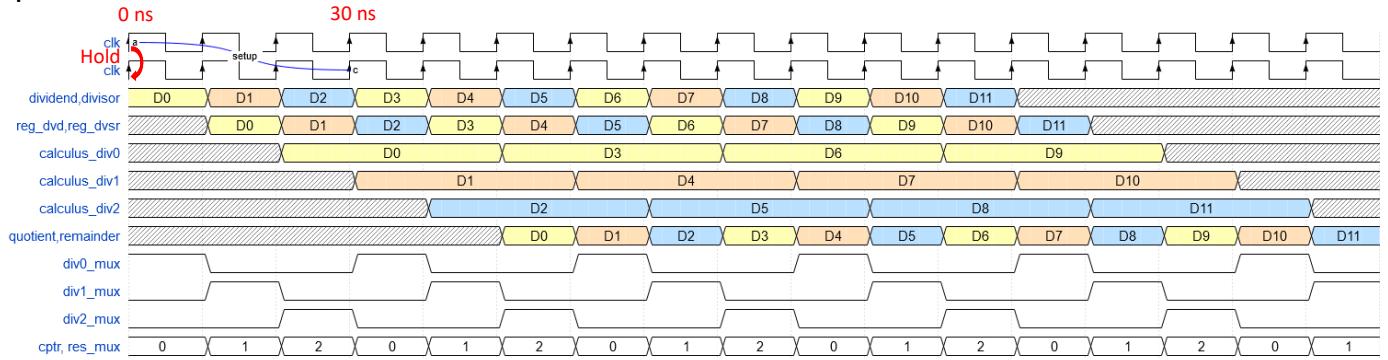
Une période d'horloge plus tard la donnée D1 rentre dans le premier bloc calculus « div1 ».

Trois fronts montant d'horloge plus tard, nous obtenons une donnée pertinente.

Sur le port « quotient » et « remainder » de l'architecture une donnée pertinente est disponible à chaque front montant d'horloge.

## STA et simulation post-implémentation avec délais

Chronogramme des fronts d'horloge entre lesquels doivent être réalisés les analyses de Set-up et de Hold.



Les contraintes que nous devons appliquer sont les suivantes :

```
create_clock -period 10.000 -name sys_clk_pin -waveform {0.000 5.000} -add [get_ports clk]
set_multicycle_path -setup -through [get_cells {div1 div2 div3}] 3
set_multicycle_path -hold -through [get_cells {div1 div2 div3}] 2
```

J'ai utilisé la documentation suivante pour écrire les contraintes.

Page 115 : <https://docs.xilinx.com/v/u/2020.2-English/ug903-vivado-using-constraints>

Design Timing Summary		
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): <b>2.622 ns</b>	Worst Hold Slack (WHS): <b>0.155 ns</b>	Worst Pulse Width Slack (WPWS): <b>4.500 ns</b>
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 170	Total Number of Endpoints: 170	Total Number of Endpoints: 123

All user specified timing constraints are met.

Nous remarquons que les temps de Setup et de Hold sont positifs après synthèse.

Après Implémentation, nous obtenons des temps de Setup et de Hold positifs :

Design Timing Summary		
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): <b>0.154 ns</b>	Worst Hold Slack (WHS): <b>0.172 ns</b>	Worst Pulse Width Slack (WPWS): <b>4.500 ns</b>
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 170	Total Number of Endpoints: 170	Total Number of Endpoints: 123

All user specified timing constraints are met.

Regardons la cohérence de nos résultats.

## Pour le Setup :

Project Summary		Device	Path 1 - timing_1
<b>Summary</b>			
Name	Path 1	Slack	0.154ns
Source	div3_divisor_reg[1]/C	(rising edge-triggered cell FDCE clocked by sys_clk_pin {rise@0.000ns fall@5.000ns period=10.000ns})	
Destination	reg_remainder_reg[4]/D	(rising edge-triggered cell FDCE clocked by sys_clk_pin {rise@0.000ns fall@5.000ns period=10.000ns})	
Path Group	sys_clk_pin		
Path Type	Setup (Max at Slow Process Corner)		
Requirement	30.000ns (sys_clk_pin rise@30.000ns - sys_clk_pin rise@0.000ns)		
Data Path Delay	29.800ns (logic 16.607ns (55.727%) route 13.193ns (44.273%))		
Logic Levels	53 (CARRY4=36 LUT2=6 LUT4=8 LUT5=1 LUT6=2)		
Clock Path Skew	-0.041ns		
Clock Uncertainty	0.035ns		
Timing Exception	MultiCycle Path Setup -end 3		
Source Clock Path			

L'analyse du Setup s'effectue à un moment cohérent du temps : 0ns et 30 ns

## Pour le Hold :

Project Summary		Device	Path 1 - timing_1	Path 11 - timing_1
<b>Summary</b>				
Name	Path 11	Slack (Hold)	0.172ns	
Source	div_dvsr_reg[9]/C	(rising edge-triggered cell FDCE clocked by sys_clk_pin {rise@0.000ns fall@5.000ns period=10.000ns})		
Destination	div3_divisor_reg[9]/D	(rising edge-triggered cell FDCE clocked by sys_clk_pin {rise@0.000ns fall@5.000ns period=10.000ns})		
Path Group	sys_clk_pin			
Path Type	Hold (Min at Fast Process Corner)			
Requirement	0.000ns (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)			
Data P...Delay	0.240ns (logic 0.141ns (58.795%) route 0.099ns (41.205%))			
Logic Levels	0			
Clock ... Skew	0.013ns			

L'analyse du Hold s'effectue à un moment cohérent du temps : 0ns et 0 ns

Nous retrouvons bien un multicycle égale à 3 pour le Setup et pour le hold il n'y a pas de multicycle.

Regardons en détail le rapport de Timing.

### Analyse du rapport de timings

Design Timing Summary				
WNS(ns)	TNS(ns)	TNS Failing Endpoints	TNS Total Endpoints	
0.154	0.000	0	170	
WHS(ns)	THS(ns)	THS Failing Endpoints	THS Total Endpoints	
0.172	0.000	0	170	
WPWS(ns)	TPWS(ns)	TPWS Failing Endpoints	TPWS Total Endpoints	
4.500	0.000	0	123	

| Clock Summary

| -----

Clock	Waveform(ns)	Period(ns)	Frequency(MHz)
sys_clk_pin	{0.000 5.000}	10.000	100.000

| Intra Clock Table

| -----

WNS(ns)	TNS(ns)	TNS Failing Endpoints	TNS Total Endpoints
0.154	0.000	0	170
WHS(ns)	THS(ns)	THS Failing Endpoints	THS Total Endpoints
0.172	0.000	0	170
WPWS(ns)	TPWS(ns)	TPWS Failing Endpoints	TPWS Total Endpoints
4.500	0.000	0	123

Il n'y a pas de changement de domaines d'horloges

Relevé :

- Slack = WNS = 0.154 ns
- WNS ≥ 0 et WHS ≥ 0

Calcul fréquence maximale :

$$f_{max} = \frac{1}{(period - WNS) * 10^{-9}} = \frac{1}{(10 - 0.154) * 10^{-9}} = 101\,564\,086\ Hz$$

## Chemin critique

Setup :

## Max Delay Paths

```

Slack (MET) : 0.154ns (required time - arrival time)
  Source: div3_divisor_reg[1]/C
    (rising edge-triggered cell FDCE clocked by sys_clk_pin {rise@0.000ns fall@5.000ns
period=10.000ns})
  Destination: reg_remainder_reg[4]/D
    (rising edge-triggered cell FDCE clocked by sys_clk_pin {rise@0.000ns fall@5.000ns
period=10.000ns})
Path Group: sys_clk_pin
Path Type: Setup (Max at Slow Process Corner)
Requirement: 30.000ns (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
Data Path Delay: 29.800ns (logic 16.607ns (55.72%) route 13.193ns (44.273%))
Logic Levels: 53 (CARRY4=36 LUT2=6 LUT4=8 LUT5=1 LUT6=2)
Clock Path Skew: -0.041ns (DCD - SCD + CPR)
  Destination Clock Delay (DCD): 4.416ns = (14.416 - 10.000 )
  Source Clock Delay (SCD): 4.780ns
  Clock Pessimism Removal (CPR): 0.323ns
Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
  Total System Jitter (TSJ): 0.071ns
  Total Input Jitter (TIJ): 0.000ns
  Discrete Jitter (DJ): 0.000ns
  Phase Error (PE): 0.000ns
Timing Exception: MultiCycle Path Setup -end 3

```

L'analyse du Setup s'effectue à un moment cohérent du temps : 0ns et 30 ns

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock sys_clk_pin rise edge)				
N15		0.000	0.000 r	
	net (fo=0)	0.000	0.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_0)	0.948	0.948 r	clk_IBUF_inst/0
	net (fo=1, routed)	2.016	2.963	clk_IBUF
BUFGCTRL_X0Y0	BUFG (Prop_bufg_I_0)	0.096	3.059 r	clk_IBUF_BUFG_inst/0
	net (fo=122, routed)	1.720	4.780	clk_IBUF_BUFG
SLICE_X1Y88	FDCE		r	div3_divisor_reg[1]/C
SLICE_X1Y88	FDCE (Prop_fdce_C_0)	0.456	5.236 r	div3_divisor_reg[1]/Q
	net (fo=15, routed)	1.062	6.298	div3_divisor[1]
SLICE_X0Y94	LUT4 (Prop_lut4_I1_0)	0.124	6.422 r	reg_quotient[11]_i_109/0
	net (fo=1, routed)	0.000	6.422	reg_quotient[11]_i_109_n_0
SLICE_X0Y94	CARRY4 (Prop_carry4_S[1]_CO[3])	0.550	6.972 r	reg_quotient_reg[11]_i_77/CO[3]
	net (fo=1, routed)	0.000	6.972	reg_quotient_reg[11]_i_77_n_0
SLICE_X0Y95	CARRY4 (Prop_carry4_CI_CO[3])	0.114	7.086 r	reg_quotient_reg[11]_i_52/CO[3]
	net (fo=1, routed)	0.000	7.086	reg_quotient_reg[11]_i_52_n_0
SLICE_X0Y96	CARRY4 (Prop_carry4_CI_0[3])	0.313	7.399 r	reg_quotient_reg[11]_i_28/0[3]
	net (fo=12, routed)	0.710	8.109	reg_quotient_reg[11]_i_28_n_4
SLICE_X1Y96	LUT4 (Prop_lut4_I2_0)	0.306	8.415 r	reg_quotient[10]_i_48/0
	net (fo=1, routed)	0.000	8.415	reg_quotient[10]_i_48_n_0
SLICE_X1Y96	CARRY4 (Prop_carry4_S[2]_CO[3])	0.398	8.813 r	reg_quotient_reg[10]_i_31/CO[3]
	net (fo=1, routed)	0.000	8.813	reg_quotient_reg[10]_i_31_n_0
SLICE_X1Y97	CARRY4 (Prop_carry4_CI_CO[3])	0.114	8.927 r	reg_quotient_reg[10]_i_16/CO[3]
	net (fo=1, routed)	0.000	8.927	reg_quotient_reg[10]_i_16_n_0
SLICE_X1Y98	CARRY4 (Prop_carry4_CI_0[3])	0.313	9.240 r	reg_quotient_reg[10]_i_9/0[3]
	net (fo=12, routed)	0.840	10.080	reg_quotient_reg[10]_i_9_n_4
SLICE_X2Y93	LUT2 (Prop_lut2_I1_0)	0.298	10.378 r	reg_quotient[9]_i_46/0
	net (fo=1, routed)	0.000	10.378	reg_quotient[9]_i_46_n_0
SLICE_X2Y93	CARRY4 (Prop_carry4_DI[0]_CO[3])	0.471	10.849 r	reg_quotient_reg[9]_i_31/CO[3]
	net (fo=1, routed)	0.000	10.849	reg_quotient_reg[9]_i_31_n_0
SLICE_X2Y94	CARRY4 (Prop_carry4_CI_CO[3])	0.117	10.966 r	reg_quotient_reg[9]_i_16/CO[3]
	net (fo=1, routed)	0.000	10.966	reg_quotient_reg[9]_i_16_n_0
SLICE_X2Y95	CARRY4 (Prop_carry4_CI_0[3])	0.315	11.281 r	reg_quotient_reg[9]_i_9/0[3]
	net (fo=12, routed)	0.750	12.031	reg_quotient_reg[9]_i_9_n_4
SLICE_X1Y92	LUT2 (Prop_lut2_I1_0)	0.301	12.332 r	reg_quotient[8]_i_61/0
	net (fo=1, routed)	0.000	12.332	reg_quotient[8]_i_61_n_0
SLICE_X1Y92	CARRY4 (Prop_carry4_DI[0]_CO[3])	0.483	12.815 r	reg_quotient_reg[8]_i_46/CO[3]
	net (fo=1, routed)	0.000	12.815	reg_quotient_reg[8]_i_46_n_0
SLICE_X1Y93	CARRY4 (Prop_carry4_CI_CO[3])	0.114	12.929 r	reg_quotient_reg[8]_i_31/CO[3]
	net (fo=1, routed)	0.000	12.929	reg_quotient_reg[8]_i_31_n_0
SLICE_X1Y94	CARRY4 (Prop_carry4_CI_0[3])	0.313	13.242 r	reg_quotient_reg[8]_i_16/0[3]
	net (fo=12, routed)	0.847	14.089	reg_quotient_reg[8]_i_16_n_4
SLICE_X0Y89	LUT2 (Prop_lut2_I1_0)	0.332	14.421 r	reg_quotient[7]_i_46/0
	net (fo=1, routed)	0.000	14.421	reg_quotient[7]_i_46_n_0
SLICE_X0Y89	CARRY4 (Prop_carry4_DI[0]_CO[3])	0.483	14.904 r	reg_quotient_reg[7]_i_31/CO[3]
	net (fo=1, routed)	0.000	14.904	reg_quotient_reg[7]_i_31_n_0
SLICE_X0Y90	CARRY4 (Prop_carry4_CI_CO[3])	0.114	15.018 r	reg_quotient_reg[7]_i_16/CO[3]
	net (fo=1, routed)	0.000	15.018	reg_quotient_reg[7]_i_16_n_0
SLICE_X0Y91	CARRY4 (Prop_carry4_CI_0[3])			

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		0.313	15.331 r reg_quotient_reg[7]_i_9/0[3]
SLICE_X1Y88	net (fo=12, routed)	0.752	16.084 reg_quotient_reg[7]_i_9_n_4
	LUT4 (Prop_lut4_I2_0)	0.306	16.390 r reg_quotient[6]_i_49/0
	net (fo=1, routed)	0.000	16.390 reg_quotient[6]_i_49_n_0
SLICE_X1Y88	CARRY4 (Prop_carry4_S[1]_CO[3])	0.550	16.940 r reg_quotient_reg[6]_i_31/CO[3]
	net (fo=1, routed)	0.000	16.940 reg_quotient_reg[6]_i_31_n_0
SLICE_X1Y89	CARRY4 (Prop_carry4_CI_CO[3])	0.114	17.054 r reg_quotient_reg[6]_i_16/CO[3]
	net (fo=1, routed)	0.000	17.054 reg_quotient_reg[6]_i_16_n_0
SLICE_X1Y90	CARRY4 (Prop_carry4_CI_0[3])	0.313	17.367 r reg_quotient_reg[6]_i_9/0[3]
	net (fo=12, routed)	0.863	18.230 reg_quotient_reg[6]_i_9_n_4
SLICE_X0Y85	LUT2 (Prop_lut2_I1_0)	0.332	18.562 r 0_carry_i_31/0
	net (fo=1, routed)	0.000	18.562 0_carry_i_31_n_0
SLICE_X0Y85	CARRY4 (Prop_carry4_DI[0]_CO[3])	0.483	19.045 r 0_carry_i_25/CO[3]
	net (fo=1, routed)	0.000	19.045 0_carry_i_25_n_0
SLICE_X0Y86	CARRY4 (Prop_carry4_CI_CO[3])	0.114	19.159 r reg_quotient_reg[5]_i_16/CO[3]
	net (fo=1, routed)	0.000	19.159 reg_quotient_reg[5]_i_16_n_0
SLICE_X0Y87	CARRY4 (Prop_carry4_CI_0[3])	0.313	19.472 r reg_quotient_reg[5]_i_9/0[3]
	net (fo=12, routed)	0.743	20.215 reg_quotient_reg[5]_i_9_n_4
SLICE_X1Y84	LUT4 (Prop_lut4_I2_0)	0.306	20.521 r 0_carry_i_29/0
	net (fo=1, routed)	0.000	20.521 0_carry_i_29_n_0
SLICE_X1Y84	CARRY4 (Prop_carry4_S[1]_CO[3])	0.550	21.071 r 0_carry_i_19/CO[3]
	net (fo=1, routed)	0.000	21.071 0_carry_i_19_n_0
SLICE_X1Y85	CARRY4 (Prop_carry4_CI_CO[3])	0.114	21.185 r 0_carry_0_i_16/CO[3]
	net (fo=1, routed)	0.000	21.185 0_carry_0_i_16_n_0
SLICE_X1Y86	CARRY4 (Prop_carry4_CI_0[3])	0.313	21.498 r reg_quotient_reg[4]_i_16/0[3]
	net (fo=12, routed)	0.811	22.309 reg_quotient_reg[4]_i_16_n_4
SLICE_X3Y88	LUT4 (Prop_lut4_I2_0)	0.306	22.615 r 0_carry_0_i_19/0
	net (fo=1, routed)	0.000	22.615 0_carry_0_i_19_n_0
SLICE_X3Y88	CARRY4 (Prop_carry4_S[1]_CO[3])	0.550	23.165 r 0_carry_0_i_11/CO[3]
	net (fo=1, routed)	0.000	23.165 0_carry_0_i_11_n_0
SLICE_X3Y89	CARRY4 (Prop_carry4_CI_0[3])	0.313	23.478 r 0_carry_1_i_11/0[3]
	net (fo=12, routed)	0.675	24.153 0_carry_1_i_11_n_4
SLICE_X2Y88	LUT2 (Prop_lut2_I1_0)	0.332	24.485 r 0_carry_i_14/0
	net (fo=1, routed)	0.000	24.485 0_carry_i_14_n_0
SLICE_X2Y88	CARRY4 (Prop_carry4_DI[0]_CO[3])	0.471	24.956 r 0_carry_i_7/CO[3]
	net (fo=1, routed)	0.000	24.956 0_carry_i_7_n_0
SLICE_X2Y89	CARRY4 (Prop_carry4_CI_CO[3])	0.117	25.073 r 0_carry_0_i_6/CO[3]
	net (fo=1, routed)	0.000	25.073 0_carry_0_i_6_n_0
SLICE_X2Y90	CARRY4 (Prop_carry4_CI_0[3])	0.315	25.388 r 0_carry_1_i_6/0[3]
	net (fo=12, routed)	0.657	26.044 div3/0_carry_1_i_1_1[3]
SLICE_X4Y89	LUT4 (Prop_lut4_I2_0)	0.307	26.351 r div3/0_carry_i_11/0
	net (fo=1, routed)	0.000	26.351 div3/0_carry_i_11_n_0
SLICE_X4Y89	CARRY4 (Prop_carry4_S[1]_CO[3])	0.550	26.901 r div3/0_carry_i_1/CO[3]
	net (fo=1, routed)	0.000	26.901 div3/0_carry_i_1_n_0
SLICE_X4Y90	CARRY4 (Prop_carry4_CI_CO[3])	0.114	27.015 r div3/0_carry_0_i_1/CO[3]
	net (fo=1, routed)	0.000	27.015 div3/0_carry_0_i_1_n_0
SLICE_X4Y91	CARRY4 (Prop_carry4_CI_0[3])	0.313	27.328 r div3/0_carry_1_i_1/0[3]
	net (fo=12, routed)	0.815	28.143 div3/0_carry_1_i_1_n_4
SLICE_X3Y93	LUT2 (Prop_lut2_I0_0)	0.306	28.449 r div3/0_carry_1_i_2_0/0
	net (fo=1, routed)	0.000	28.449 div3/0_carry_1_i_2_0_n_0
SLICE_X3Y93	CARRY4 (Prop_carry4_S[3]_CO[3])	0.401	28.850 r div3/0_carry_1/CO[3]
	net (fo=1, routed)	0.000	28.850 div3/0_carry_1_n_0
SLICE_X3Y94	CARRY4 (Prop_carry4_CI_0[0])	0.222	29.072 r div3/0_carry_2/0[0]
	net (fo=17, routed)	0.725	29.797 div3/0_carry_2_n_7
SLICE_X4Y93	LUT4 (Prop_lut4_I2_0)	0.299	30.096 r div3/0_36_carry_i_4/0
	net (fo=1, routed)	0.000	30.096 div3/0_36_carry_i_4_n_0
SLICE_X4Y93	CARRY4 (Prop_carry4_S[1]_CO[3])	0.550	30.646 r div3/0_36_carry/CO[3]
	net (fo=1, routed)	0.000	30.646 div3/0_36_carry_n_0
SLICE_X4Y94	CARRY4 (Prop_carry4_CI_0[3])	0.313	30.959 r div3/0_36_carry_0/0[3]
	net (fo=2, routed)	0.866	31.825 div3/0_36_carry_0_n_4
SLICE_X6Y95	LUT6 (Prop_lut6_I2_0)	0.306	32.131 f div3/reg_quotient[11]_i_31/0
	net (fo=1, routed)	0.590	32.721 div3/reg_quotient[11]_i_31_n_0
SLICE_X6Y96	LUT5 (Prop_lut5_I0_0)	0.124	32.845 f div3/reg_quotient[11]_i_13/0
	net (fo=13, routed)	0.535	33.380 div3/reg_quotient[11]_i_13_n_0
SLICE_X6Y96	LUT4 (Prop_lut4_I3_0)	0.124	33.504 f div3/reg_remainder[11]_i_4/0
	net (fo=12, routed)	0.952	34.456 div3/reg_remainder[11]_i_4_n_0
SLICE_X7Y92	LUT6 (Prop_lut6_I5_0)	0.124	34.580 r div3/reg_remainder[4]_i_1/0
	net (fo=1, routed)	0.000	34.580 mux_remainder[4]
SLICE_X7Y92	FDCE	r	reg_remainder_reg[4]/0

<b>(clock sys_clk_pin rise edge)</b>			
		30.000	30.000 r
N15	net (fo=0)	0.000	30.000 r clk (IN)
N15	IBUF (Prop_ibuf_I_0)	0.814	30.814 r clk_IBUF_inst/0
	net (fo=1, routed)	1.911	32.725 clk_IBUF
BUFGCTRL_X0Y0	BUFG (Prop_bufg_I_0)	0.091	32.816 r clk_IBUF_BUFG_inst/0
	net (fo=122, routed)	1.599	34.416 clk_IBUF_BUFG
SLICE_X7Y92	FDCE	r	reg_remainder_reg[4]/C
	clock pessimism	0.323	34.739
	clock uncertainty	-0.035	34.703
SLICE_X7Y92	FDCE (Setup_fdce_C_D)	0.031	34.734 reg_remainder_reg[4]
	required time	34.734	
	arrival time	-34.580	
	slack	0.154	

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Le chemin critique se trouve entre le bit numéro 1 du registre div3\_divisor\_reg et le bit numéro 4 du registre reg\_remainder\_reg.

Ici, il traverse 17 LUT.

Il traverse 35 CARRY 4 c'est-à-dire des additionneurs.

**Hold :**

Min Delay Paths

```

Slack (MET) :          0.172ns (arrival time - required time)
Source:                reg_dvsr_reg[9]/C
                        (rising edge-triggered cell FDCE clocked by sys_clk_pin {rise@0.000ns fall@5.000ns
period=10.000ns})
Destination:           div3_divisor_reg[9]/D
                        (rising edge-triggered cell FDCE clocked by sys_clk_pin {rise@0.000ns fall@5.000ns
period=10.000ns})
Path Group:            sys_clk_pin
Path Type:             Hold (Min at Fast Process Corner)
Requirement:           0.000ns (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
Data Path Delay:       0.240ns (logic 0.141ns (58.795%) route 0.099ns (41.205%))
Logic Levels:          0
Clock Path Skew:      0.013ns (DCD - SCD - CPR)
Destination Clock Delay (DCD): 1.960ns
Source Clock Delay (SCD):   1.441ns
Clock Pessimism Removal (CPR): 0.505ns

```

L'analyse du Hold s'effectue à un moment cohérent du temps : 0ns et 0 ns

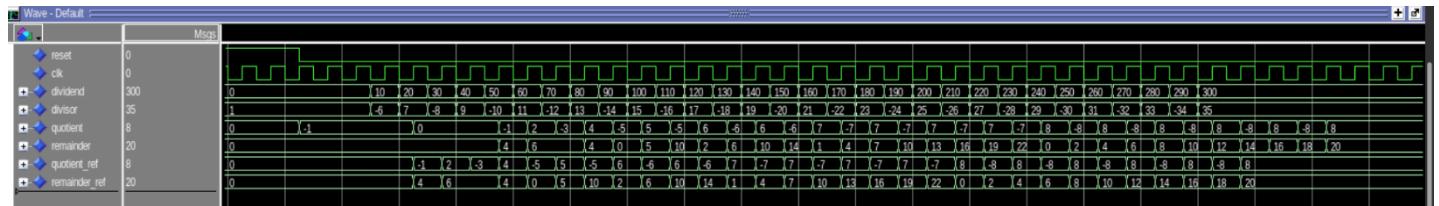
Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock sys_clk_pin rise edge)				
N15		0.000	0.000	r
	net (fo=0)	0.000	0.000	r clk (IN)
N15	IBUF (Prop_ibuf_I_0)	0.177	0.177	r clk_IBUF_inst/0
	net (fo=1, routed)	0.640	0.817	clk_IBUF
BUFGCTRL_X0Y0	BUFG (Prop_bufg_I_0)	0.026	0.843	r clk_IBUF_BUFG_inst/0
	net (fo=122, routed)	0.599	1.441	clk_IBUF_BUFG
SLICE_X0Y87	FDCE			r reg_dvsr_reg[9]/C
SLICE_X0Y87	FDCE (Prop_fdce_C_Q)	0.141	1.582	r reg_dvsr_reg[9]/Q
SLICE_X1Y87	net (fo=3, routed)	0.099	1.681	r reg_dvsr[9]
SLICE_X1Y87	FDCE			r div3_divisor_reg[9]/D

	(clock sys_clk_pin rise edge)	0.000	0.000	r
N15		0.000	0.000	r clk (IN)
	net (fo=0)	0.000	0.000	clk
N15	IBUF (Prop_ibuf_I_0)	0.365	0.365	r clk_IBUF_inst/0
	net (fo=1, routed)	0.695	1.060	clk_IBUF
BUFGCTRL_X0Y0	BUFG (Prop_bufg_I_0)	0.029	1.089	r clk_IBUF_BUFG_inst/0
	net (fo=122, routed)	0.871	1.960	clk_IBUF_BUFG
SLICE_X1Y87	FDCE			r div3_divisor_reg[9]/C
SLICE_X1Y87	clock pessimism	-0.505	1.454	
SLICE_X1Y87	FDCE (Hold_fdce_C_D)	0.055	1.509	div3_divisor_reg[9]
	required time		-1.509	
	arrival time		1.681	
	slack		0.172	

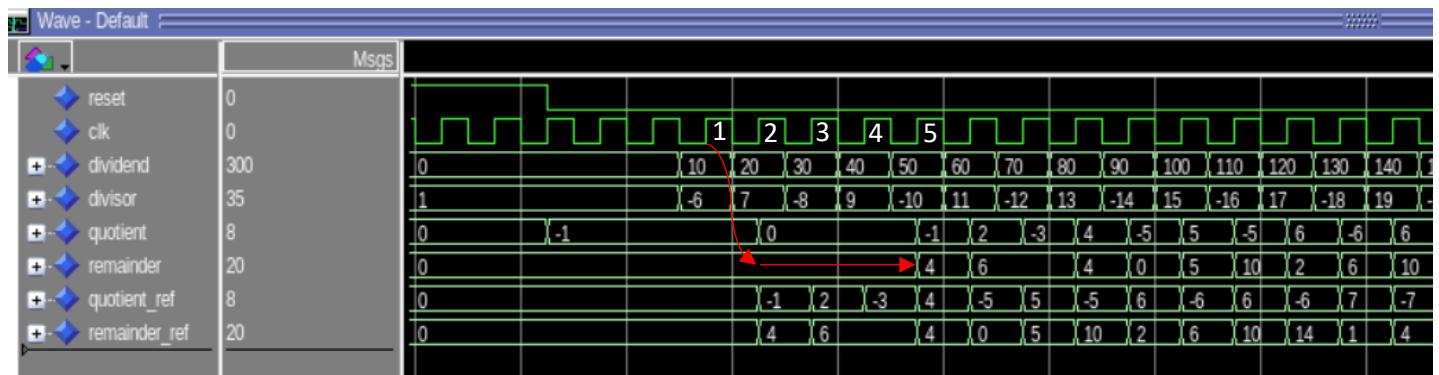
Je réalise une simulation comportementale post-implémentation.

### Post-Implementation Functional Simulation :

Vue globale :



Séquencement :



La simulation est toujours fonctionnelle.

Lorsque l'architecture reçoit la donnée cinq fronts montant plus tard, une donnée pertinente est disponible à la sortie de l'architecture. S'ensuit une nouvelle donnée pertinente à chaque front montant de l'horloge clk sur le port « quotient » et « remainder » de l'architecture.

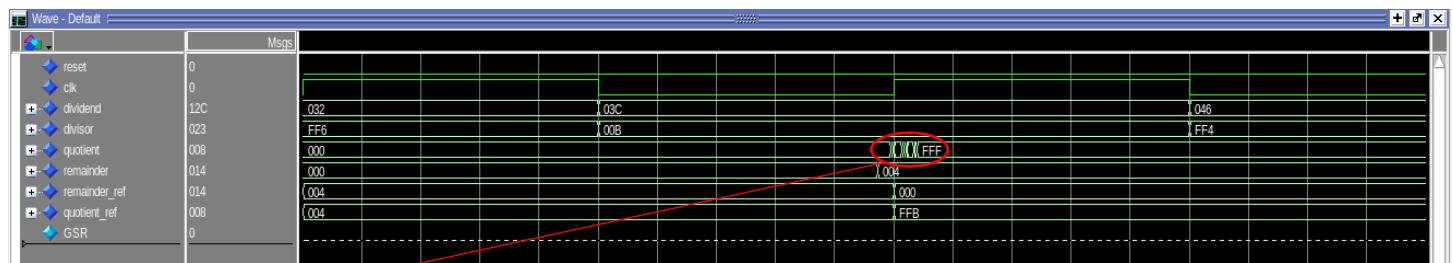
Je réalise une simulation post-implémentation avec prise en compte des délais.

### Post-Implementation Timing Simulation :



Au bout de 5 cycles d'horloge clk, je n'obtiens pas le résultat souhaité. Néanmoins un front montant d'horloge suivant j'obtiens une première donnée pertinente. S'ensuit à chaque front montant d'horloge une nouvelle donnée pertinente.

## Délai de routage :



Il y a un délai de routage important. La donnée prend du temps pour arriver au plot de sortie.

## Architecture n°2 (avec PLL)

Dans cette seconde partie, je vais utiliser une PLL et un compteur one hot pour réaliser une seconde architecture.

### Analyse du rapport de synthèse

Dans cette partie, nous allons effectuer une analyse du rapport de synthèse.

Report Check Netlist:

	Item	Errors	Warnings	Status	Description
1	multi_driven_nets	0	0	Passed	Multi driven nets

Vivado informe qu'il n'y a aucun court-circuit.

-----  
Start RTL Component Statistics  
-----

Detailed RTL Component Info :

Adders :		
2 Input	13 Bit	Adders := 39
3 Input	13 Bit	Adders := 39
2 Input	12 Bit	Adders := 3
Registers :		
	12 Bit	Registers := 16
	3 Bit	Registers := 1
Muxes :		
2 Input	13 Bit	Muxes := 48
2 Input	12 Bit	Muxes := 3
4 Input	12 Bit	Muxes := 2
2 Input	1 Bit	Muxes := 36

-----  
Finished RTL Component Statistics  
-----

Report Cell Usage:

	Cell	Count
1	my_pll_bbox_0	1
2	CARRY4	321
3	LUT1	90
4	LUT2	72
5	LUT3	150
6	LUT4	825
7	LUT5	78
8	LUT6	471
9	FDCE	200
10	FDPE	1
11	IBUF	25
12	OBUF	24

Vivado informe qu'il a reconnu 39 additionneurs de nombres sur 13 bits, 39 additionneurs de nombres avec 3 entrées sur 13 bits et 3 additionneurs de 12 bits.

Il n'y a aucun latch.

## Relevé des ressources

### 1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
<b>Slice LUTs</b>	<b>1482</b>	0	0	63400	2.34
LUT as Logic	1482	0	0	63400	2.34
LUT as Memory	0	0	0	19000	0.00
<b>Slice Registers</b>	<b>201</b>	0	0	126800	0.16
Register as Flip Flop	201	0	0	126800	0.16
Register as Latch	0	0	0	126800	0.00
F7 Muxes	0	0	0	31700	0.00
F8 Muxes	0	0	0	15850	0.00

#### 1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	-	-	-
0	-	-	Set
0	-	-	Reset
0	-	Set	-
0	-	Reset	-
0	Yes	-	-
1	Yes	-	Set
200	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-

### Relevé des ressources :

- 455 slices
- 1482 LUTs
- 201 DFFs

### 2. Slice Logic Distribution

Site Type	Used	Fixed	Prohibited	Available	Util%
<b>Slice</b>	<b>455</b>	0	0	15850	2.87
SLICEL	288	0			
SLICEM	167	0			
LUT as Logic	1482	0	0	63400	2.34
using O5 output only	0				
using O6 output only	1278				
using O5 and O6	204				
LUT as Memory	0	0	0	19000	0.00
LUT as Distributed RAM	0	0			
LUT as Shift Register	0	0			
Slice Registers	201	0	0	126800	0.16
Register driven from within the Slice	99				
Register driven from outside the Slice	102				
LUT in front of the register is unused	10				
LUT in front of the register is used	92				
Unique Control Sets	4		0	15850	0.03

\* \* Note: Available Control Sets calculated as Slice \* 1, Review the Control Sets Report for more information regarding control sets.

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### 3. Memory

-----

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	135	0.00
RAMB36/FIFO*	0	0	0	135	0.00
RAMB18	0	0	0	270	0.00

\* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

### 4. DSP

-----

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	0	0	0	240	0.00

### Relevé des ressources :

- 0 block RAM
- 0 DSP
- 5 arbres d'horloge (BUFGCTRL)
- 1 PLL

### 5. IO and GT Specific

-----

Site Type	Used	Fixed	Prohibited	Available	Util%
Bonded IOB	50	0	0	210	23.81
IOB Master Pads	24				
IOB Slave Pads	24				
Bonded IPADs	0	0	0	2	0.00
PHY_CONTROL	0	0	0	6	0.00
PHASER_REF	0	0	0	6	0.00
OUT_FIFO	0	0	0	24	0.00
IN_FIFO	0	0	0	24	0.00
IDELAYCTRL	0	0	0	6	0.00
IBUFDS	0	0	0	202	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	0	24	0.00
PHASER_IN/PHASER_IN_PHY	0	0	0	24	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	0	300	0.00
ILOGIC	0	0	0	210	0.00
OLOGIC	0	0	0	210	0.00

### 6. Clocking

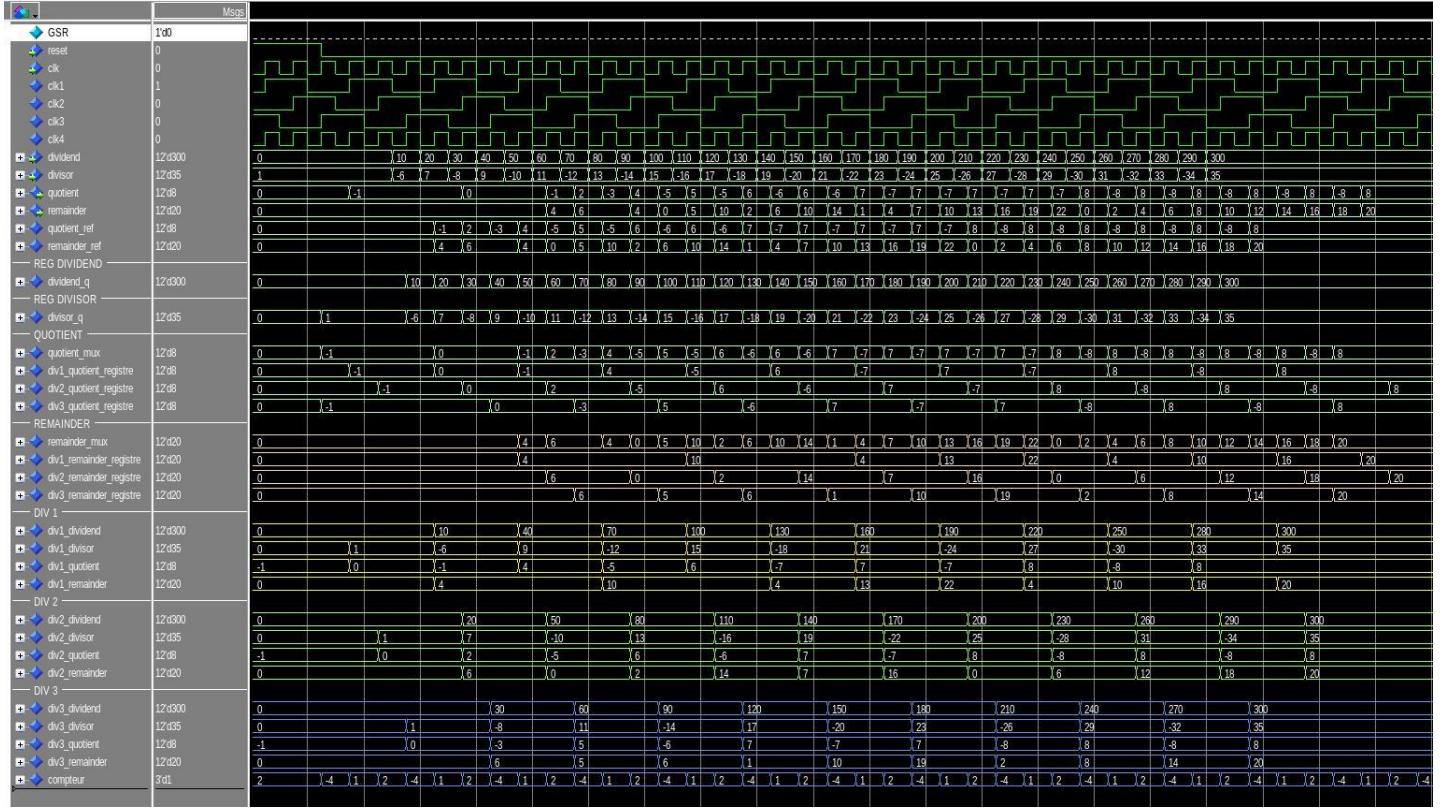
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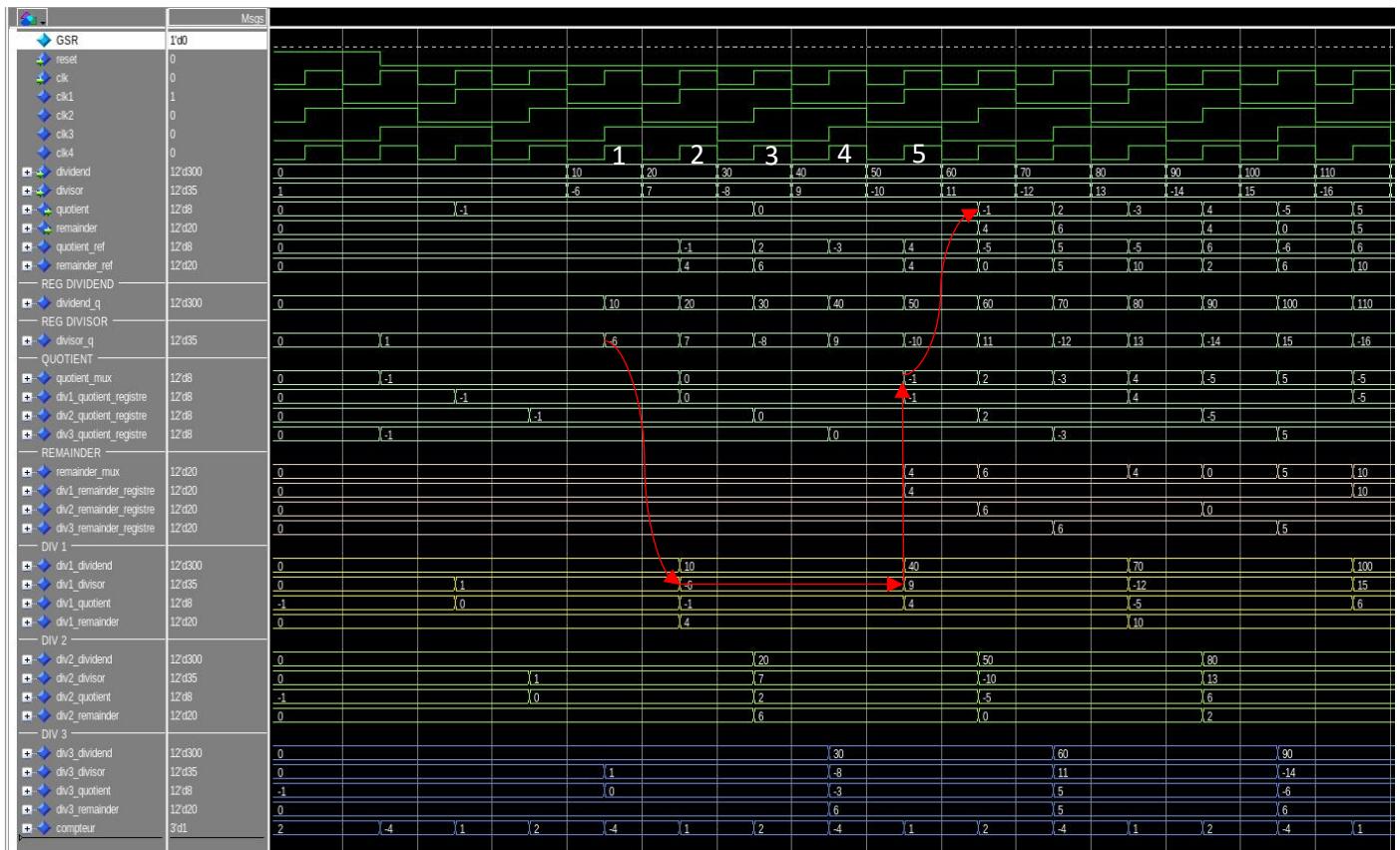
Site Type	Used	Fixed	Prohibited	Available	Util%
BUFGCTRL	5	0	0	32	15.63
BUFIO	0	0	0	24	0.00
MMCME2_ADV	0	0	0	6	0.00
PLLE2_ADV	1	0	0	6	16.67
BUFMRCE	0	0	0	12	0.00
BUFHCE	0	0	0	96	0.00
BUFR	0	0	0	24	0.00

## Simulation avant synthèse

Simulation comportementale :

J'obtiens la vue globale :

Séquencement :



La donnée D1 du "dividend" et du "divisor" sont positionnés sur front descendant de l'horloge clk. Les registres "divided\_q" et "divisor\_q" sont mis à jour au moment du front montant de l'horloge clk. Ainsi, les registres "reg\_dvd" et "reg\_dvsr" mémorisent la donnée D1.

Une période d'horloge plus tard la donnée D1 rentre dans le premier bloc calculus « div1 ».

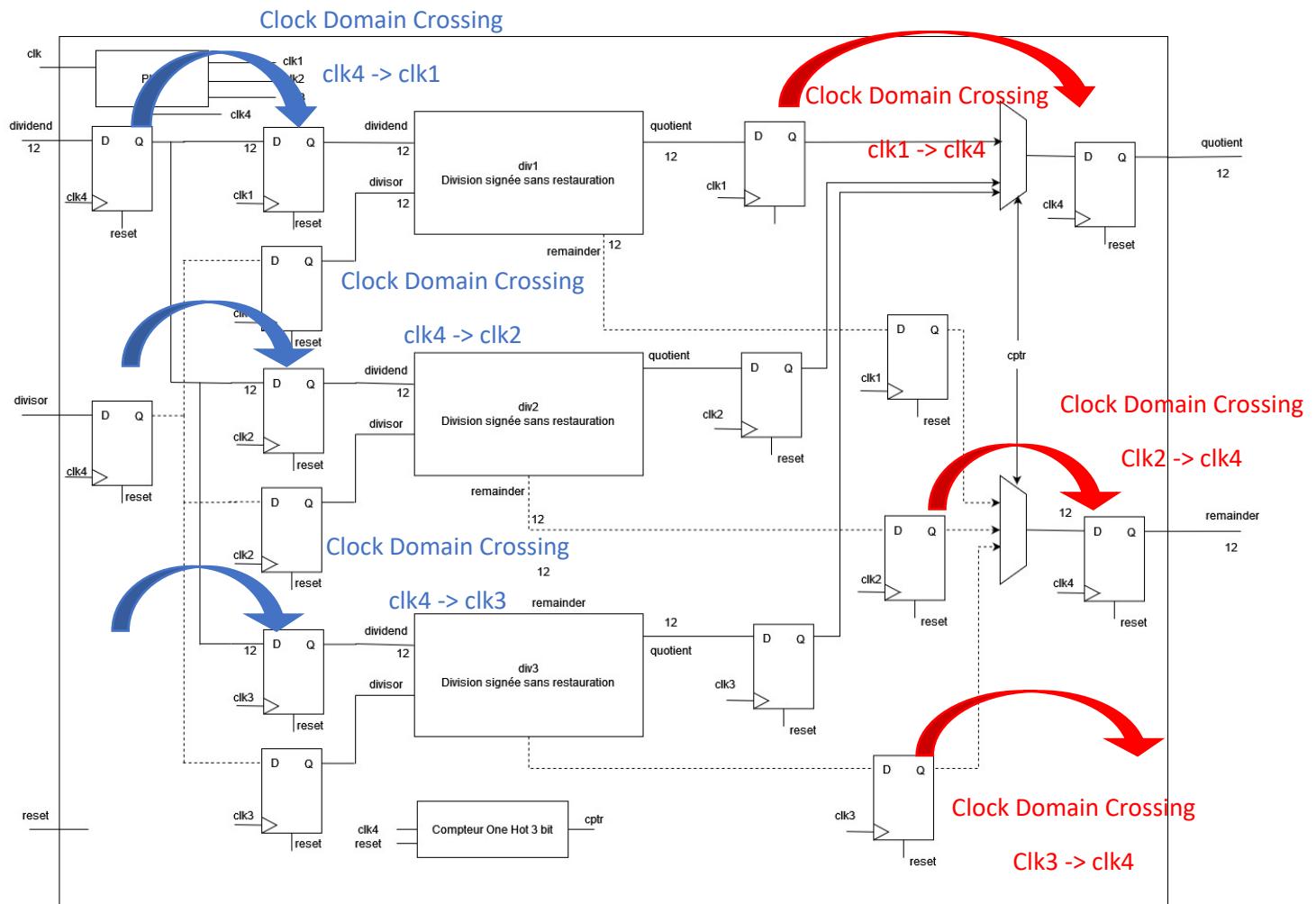
Trois fronts montant d'horloge plus tard, nous obtenons une donnée pertinente.

Une période d'horloge plus tard, la donnée se trouve dans un registre div1\_quotient\_register (respectivement div2\_quotient\_register, div3\_quotient\_register).

Sur le port « quotient » et « remainder » de l'architecture une donnée pertinente est disponible à chaque front montant d'horloge.

STA et simulation post-implémentation avec délais

Dans cette partie, je vais effectuer une analyse temporelle statique de notre architecture.

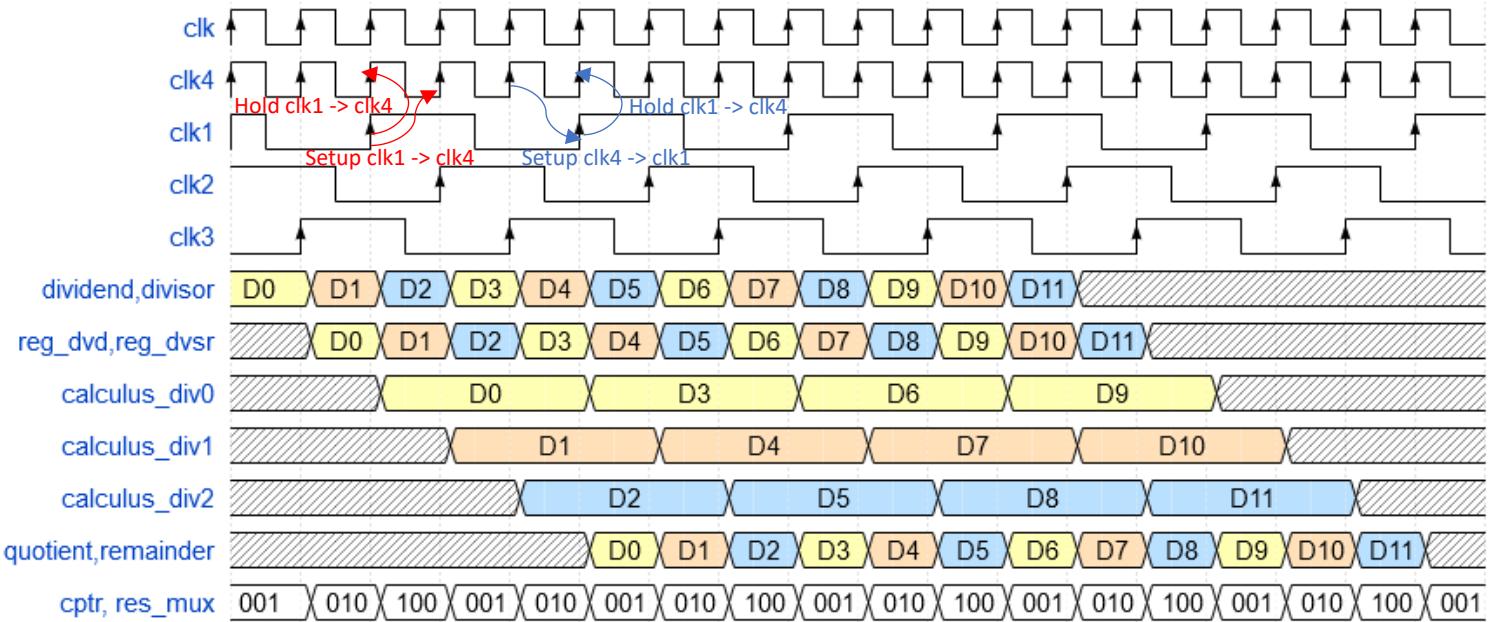


Il y a trois changements de domaine d'horloge :

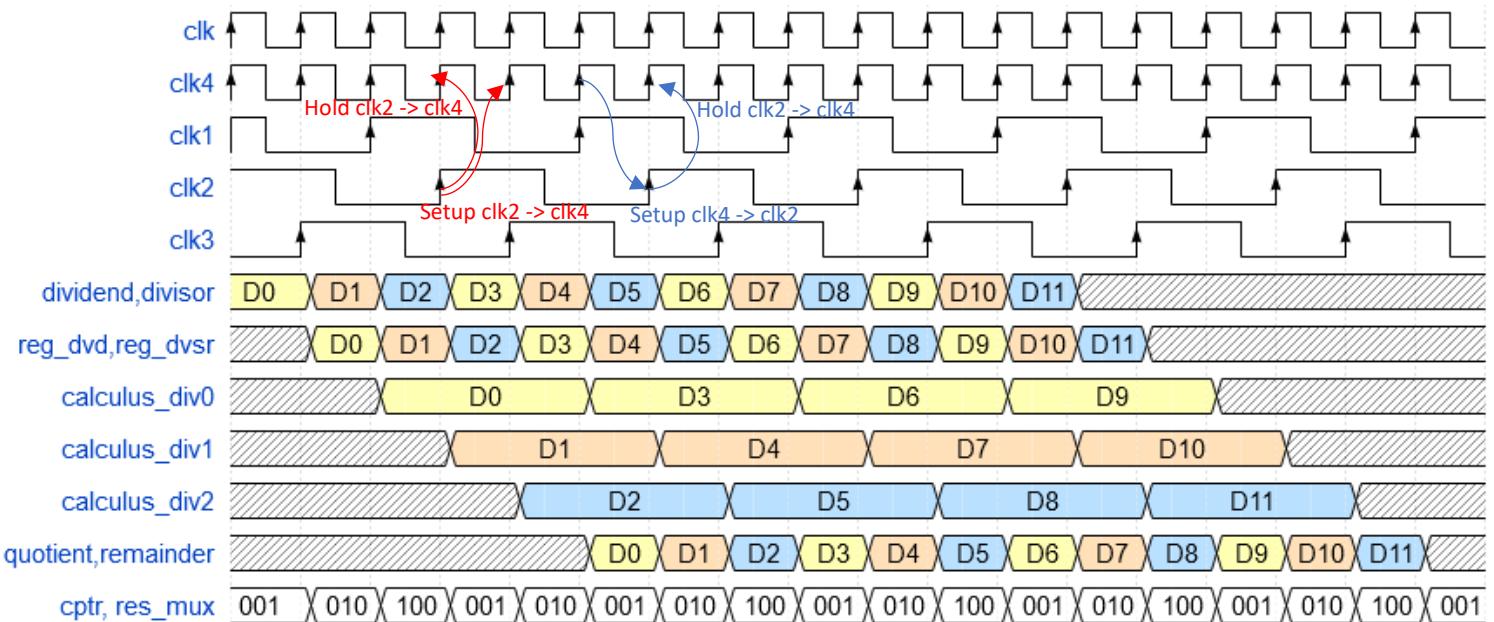
- $\text{clk4} \rightarrow \text{clk1}$
- $\text{clk4} \rightarrow \text{clk2}$
- $\text{clk4} \rightarrow \text{clk3}$
- $\text{clk1} \rightarrow \text{clk4}$
- $\text{clk2} \rightarrow \text{clk4}$
- $\text{clk3} \rightarrow \text{clk4}$

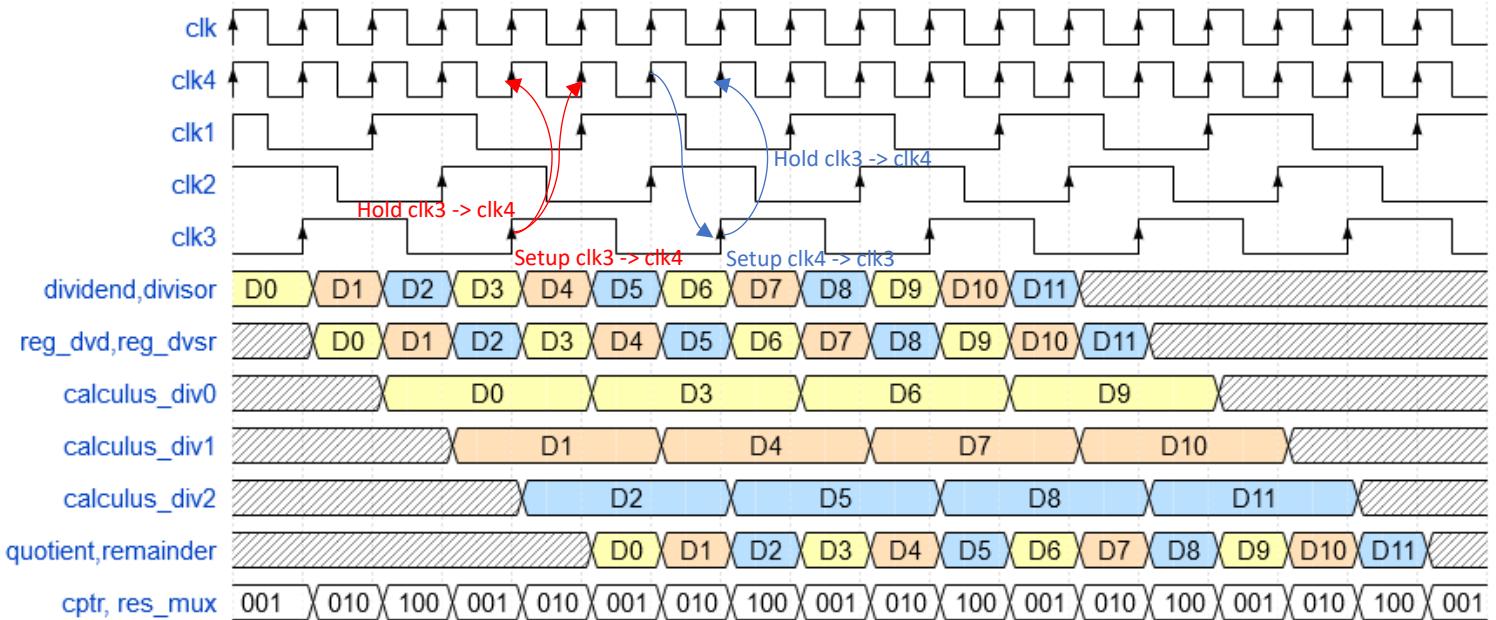
Dans ces zones de changement d'horloge, il n'y a pas de multicycles.

### Chronogrammes CDC $\text{clk4} \rightarrow \text{clk1}$ et $\text{clk1} \rightarrow \text{clk4}$ :



### Chronogrammes CDC $\text{clk4} \rightarrow \text{clk2}$ et $\text{clk2} \rightarrow \text{clk4}$ :



Chronogrammes CDC  $\text{clk4} \rightarrow \text{clk3}$  et  $\text{clk3} \rightarrow \text{clk4}$ :

## Analyse du rapport de timings

Par soucis de lisibilité et de présentation des résultats, j'ai placé le « Timing Details » dans les annexes de ce document.

Néanmoins pour appuyer mes résultats, j'ai utilisé les résultats du « Report Timing Summary ».

```
-----| Design Timing Summary
| -----
```

WNS(ns)	TNS(ns)	TNS Failing Endpoints	TNS Total Endpoints
1.362	0.000	0	177
WHS(ns)	THS(ns)	THS Failing Endpoints	THS Total Endpoints
0.134	0.000	0	177

WPWS(ns)	TPWS(ns)	TPWS Failing Endpoints	TPWS Total Endpoints
3.000	0.000	0	213

```
-----| Clock Summary
| -----
```

Clock	Waveform(ns)	Period(ns)	Frequency (MHz)
clk	{0.000 5.000}	10.000	100.000
clk1_my_pll	{0.000 15.000}	30.000	33.333
clk2_my_pll	{10.000 25.000}	30.000	33.333
clk3_my_pll	{20.000 35.000}	30.000	33.333
clk4_my_pll	{0.000 5.000}	10.000	100.000
clkfbout_my_pll	{0.000 5.000}	10.000	100.000

## Intra Clock Paths :

Clock	Edges (WNS)	WNS (ns)	TNS (ns)	Failing Endpoints (TNS)	Total Endpoints (TNS)	Edges (WHS)	WHS (ns)	THS (ns)	Failing Endpoints (THS)	Total Endpoints (THS)	WPWS (ns)	TPWS (ns)	Failing Endpoints (TPWS)	Total Endpoints (TPWS)
clk											3.000	0.000	0	1
clk1_my_pll	rise - rise	1.362	0.000	0	24	rise - rise	0.346	0.000	0	24	14.500	0.000	0	52
clk2_my_pll	rise - rise	1.808	0.000	0	24	rise - rise	0.505	0.000	0	24	14.500	0.000	0	52
clk3_my_pll	rise - rise	2.104	0.000	0	24	rise - rise	0.442	0.000	0	24	14.500	0.000	0	52
clk4_my_pll	rise - rise	6.393	0.000	0	27	rise - rise	0.250	0.000	0	27	4.500	0.000	0	53
clkfbout_my_pll											7.845	0.000	0	3

## From clk1\_my\_pll To clk1\_my\_pll :

### Setup :

Summary	
Name	Path 1
Slack	<u>1.362ns</u>
Source	div1_divisor_reg[0]/C (rising edge-triggered cell FDCE clocked by clk1_my_pll {rise@0.000ns fall@15.000ns period=30.000ns})
Destination	div1_quotient_registro_reg[10]/D (rising edge-triggered cell FDCE clocked by clk1_my_pll {rise@0.000ns fall@15.000ns period=30.000ns})
Path Group	clk1_my_pll
Path Type	Setup (Max at Slow Process Corner)
Requirement	30.000ns (clk1_my_pll rise@30.000ns - clk1_my_pll rise@0.000ns)
Data Path Delay	28.526ns (logic 11.352ns (39.795%) route 17.174ns (60.205%))
Logic Levels	33 (CARRY4=17 LUT2=1 LUT4=6 LUT5=2 LUT6=7)
Clock Path Skew	-0.047ns
Clock Uncertainty	0.094ns



L'analyse du Setup s'effectue à un moment cohérent du temps : 0ns et 30 ns

### Hold :

Summary	
Name	Path 11
Slack (Hold)	<u>0.346ns</u>
Source	div1_divisor_reg[11]/C (rising edge-triggered cell FDCE clocked by clk1_my_pll {rise@0.000ns fall@15.000ns period=30.000ns})
Destination	div1_quotient_registro_reg[1]/D (rising edge-triggered cell FDCE clocked by clk1_my_pll {rise@0.000ns fall@15.000ns period=30.000ns})
Path Group	clk1_my_pll
Path Type	Hold (Min at Fast Process Corner)
Requirement	0.000ns (clk1_my_pll rise@0.000ns - clk1_my_pll rise@0.000ns)
Data Path Delay	0.500ns (logic 0.209ns (41.776%) route 0.291ns (58.224%))
Logic Levels	1 (LUT6=1)
Clock ... Skew	0.034ns



L'analyse du Hold s'effectue à un moment cohérent du temps : 0ns et 0 ns

## From clk2\_my\_pll To clk2\_my\_pll :

### Setup :

Summary	
Name	Path 21
Slack	<u>1.808ns</u>
Source	div2_divisor_reg[2]/C (rising edge-triggered cell FDCE clocked by clk2_my_pll {rise@10.000ns fall@25.000ns period=30.000ns})
Destination	div2_quotient_registro_reg[8]/D (rising edge-triggered cell FDCE clocked by clk2_my_pll {rise@10.000ns fall@25.000ns period=30.000ns})
Path Group	clk2_my_pll
Path Type	Setup (Max at Slow Process Corner)
Requirement	30.000ns (clk2_my_pll rise@40.000ns - clk2_my_pll rise@10.000ns)
Data Path Delay	28.184ns (logic 11.549ns (40.977%) route 16.635ns (59.023%))
Logic Levels	33 (CARRY4=17 LUT1=1 LUT4=5 LUT5=2 LUT6=8)
Clock Path Skew	0.054ns
Clock Uncertainty	0.094ns



L'analyse du Setup s'effectue à un moment cohérent du temps : 40ns et 10 ns = 30 ns

Hold :

Summary	
Name	Path 31
Slack (Hold)	0.505ns
Source	div2_divisor_reg[11]_rep_0/C (rising edge-triggered cell FDCE clocked by clk2_my_pll {rise@10.000ns fall@25.000ns period=30.000ns})
Destination	div2_quotient_register_reg[8]/D (rising edge-triggered cell FDCE clocked by clk2_my_pll {rise@10.000ns fall@25.000ns period=30.000ns})
Path Group	clk2_my_pll
Path Type	Hold (Min at Fast Process Corner)
Requirement	0.000ns (clk2_my_pll rise@10.000ns - clk2_my_pll rise@10.000ns)
Data P...Delay	0.611ns (logic 0.186ns (30.424%) route 0.425ns (69.576%))
Logic Levels	1 (LUT6=1)
Clock ... Skew	0.014ns



L'analyse du Hold s'effectue à un moment cohérent du temps : 0ns et 0ns

**From clk3\_my\_pll To clk3\_my\_pll :**Setup :

Summary	
Name	Path 41
Slack	2.104ns
Source	div3_divisor_reg[1]/C (rising edge-triggered cell FDCE clocked by clk3_my_pll {rise@20.000ns fall@35.000ns period=30.000ns})
Destination	div3_quotient_register_reg[2]/D (rising edge-triggered cell FDCE clocked by clk3_my_pll {rise@20.000ns fall@35.000ns period=30.000ns})
Path Group	clk3_my_pll
Path Type	Setup (Max at Slow Process Corner)
Requirement	30.000ns (clk3_my_pll rise@50.000ns - clk3_my_pll rise@20.000ns)
Data Path Delay	27.758ns (logic 11.776ns (42.423%) route 15.982ns (57.577%))
Logic Levels	33 (CARRY4=17 LUT1=1 LUT4=5 LUT5=2 LUT6=8)
Clock Path Skew	-0.121ns
Clock Un...rtainty	0.094ns



L'analyse du Setup s'effectue à un moment cohérent du temps : 50 ns et 20 ns = 30 ns

Hold :

Summary	
Name	Path 51
Slack (Hold)	0.442ns
Source	div3_divisor_reg[11]_rep/C (rising edge-triggered cell FDCE clocked by clk3_my_pll {rise@20.000ns fall@35.000ns period=30.000ns})
Destination	div3_quotient_register_reg[11]/D (rising edge-triggered cell FDCE clocked by clk3_my_pll {rise@20.000ns fall@35.000ns period=30.000ns})
Path Group	clk3_my_pll
Path Type	Hold (Min at Fast Process Corner)
Requirement	0.000ns (clk3_my_pll rise@20.000ns - clk3_my_pll rise@20.000ns)
Data P...Delay	0.548ns (logic 0.186ns (33.962%) route 0.362ns (66.038%))
Logic Levels	1 (LUT6=1)
Clock ... Skew	0.014ns



L'analyse du Hold s'effectue à un moment cohérent du temps : 20 ns et 20 ns = 0 ns

Nous vérifions que la cohérence des horloges de l'architecture.

### **From clk4\_my\_pll To clk4\_my\_pll :**

#### Setup :

<b>Summary</b>	
Name	Path 61
Slack	<u>6.393ns</u>
Source	compteur_reg[0]/C (rising edge-triggered cell FDCE clocked by clk4_my_pll {rise@0.000ns fall@5.000ns period=10.000ns})
Destination	remainder_reg[10]/D (rising edge-triggered cell FDCE clocked by clk4_my_pll {rise@0.000ns fall@5.000ns period=10.000ns})
Path Group	clk4_my_pll
Path Type	Setup (Max at Slow Process Corner)
Requirement	10.000ns (clk4_my_pll rise@10.000ns - clk4_my_pll rise@0.000ns)
Data Path Delay	3.507ns (logic 0.580ns (16.538%) route 2.927ns (83.462%))
Logic Levels	1 (LUT6=1)
Clock Path Skew	<u>-0.052ns</u>
Clock Uncertainty	<u>0.077ns</u>

#### Hold :

<b>Summary</b>	
Name	Path 71
Slack (Hold)	<u>0.250ns</u>
Source	compteur_reg[0]/C (rising edge-triggered cell FDCE clocked by clk4_my_pll {rise@0.000ns fall@5.000ns period=10.000ns})
Destination	compteur_reg[1]/D (rising edge-triggered cell FDPE clocked by clk4_my_pll {rise@0.000ns fall@5.000ns period=10.000ns})
Path Group	clk4_my_pll
Path Type	Hold (Min at Fast Process Corner)
Requirement	0.000ns (clk4_my_pll rise@0.000ns - clk4_my_pll rise@0.000ns)
Data Path Delay	0.311ns (logic 0.141ns (45.303%) route 0.170ns (54.697%))
Logic Levels	0
Clock ... Skew	<u>0.000ns</u>

### **Inter Clock Paths :**

From Clock	To Clock	Edges (WNS)	WNS (ns)	TNS (ns)	Failing Endpoints (TNS)	Total Endpoints (TNS)	Edges (WHS)	WHS (ns)	THS (ns)	Failing Endpoints (THS)	Total Endpoints (THS)
clk4_my_pll	clk1_my_pll	rise - rise	4.173	0.000	0	26	rise - rise	0.233	0.000	0	26
clk4_my_pll	clk2_my_pll	rise - rise	4.919	0.000	0	26	rise - rise	0.232	0.000	0	26
clk4_my_pll	clk3_my_pll	rise - rise	5.512	0.000	0	26	rise - rise	0.193	0.000	0	26
clk1_my_pll	clk4_my_pll	rise - rise	6.922	0.000	0	24	rise - rise	0.150	0.000	0	24
clk2_my_pll	clk4_my_pll	rise - rise	6.989	0.000	0	24	rise - rise	0.134	0.000	0	24
clk3_my_pll	clk4_my_pll	rise - rise	6.888	0.000	0	24	rise - rise	0.186	0.000	0	24

### **From clk1\_my\_pll to clk4\_my\_pll :**

#### Setup :

<b>Summary</b>	
Name	Path 81
Slack	<u>6.922ns</u>
Source	div1_quotient_registrore_reg[7]/C (rising edge-triggered cell FDCE clocked by clk1_my_pll {rise@0.000ns fall@15.000ns period=30.000ns})
Destination	quotient_reg[7]/D (rising edge-triggered cell FDCE clocked by clk4_my_pll {rise@0.000ns fall@5.000ns period=10.000ns})
Path Group	clk4_my_pll
Path Type	Setup (Max at Slow Process Corner)
Requirement	10.000ns (clk4_my_pll rise@10.000ns - clk1_my_pll rise@0.000ns)
Data Path Delay	2.773ns (logic 0.642ns (23.154%) route 2.131ns (76.846%))
Logic Levels	1 (LUT6=1)
Clock Path Skew	<u>-0.122ns</u>
Clock Uncertainty	<u>0.214ns</u>

Hold :

Summary	
Name	Path 91
Slack (Hold)	<a href="#">0.150ns</a>
Source	<a href="#">div1_quotient_registre_reg[5]/C</a> (rising edge-triggered cell FDCE clocked by <a href="#">clk1_my_pll</a> {rise@0.000ns fall@15.000ns period=30.000ns})
Destination	<a href="#">quotient_reg[5]/D</a> (rising edge-triggered cell FDCE clocked by <a href="#">clk4_my_pll</a> {rise@0.000ns fall@5.000ns period=10.000ns})
Path Group	<a href="#">clk4_my_pll</a>
Path Type	Hold (Min at Fast Process Corner)
Requirement	0.000ns ( <a href="#">clk4_my_pll</a> rise@0.000ns - <a href="#">clk1_my_pll</a> rise@0.000ns)
Data Path Delay	0.802ns (logic 0.209ns (26.065%) route 0.593ns (73.935%))
Logic Levels	1 (LUT6=1)
Clock Path Skew	<a href="#">0.348ns</a>
Clock Uncertainty	<a href="#">0.214ns</a>

**From clk4\_my\_pll to clk1\_my\_pll :**Setup :

Summary	
Name	Path 141
Slack	<a href="#">4.173ns</a>
Source	<a href="#">divisor_q_reg[11]/C</a> (rising edge-triggered cell FDCE clocked by <a href="#">clk4_my_pll</a> {rise@0.000ns fall@5.000ns period=10.000ns})
Destination	<a href="#">div1_divisor_reg[11]_rep_0/D</a> (rising edge-triggered cell FDCE clocked by <a href="#">clk1_my_pll</a> {rise@0.000ns fall@15.000ns period=30.000ns})
Path Group	<a href="#">clk1_my_pll</a>
Path Type	Setup (Max at Slow Process Corner)
Requirement	10.000ns ( <a href="#">clk1_my_pll</a> rise@30.000ns - <a href="#">clk4_my_pll</a> rise@20.000ns)
Data Path Delay	5.284ns (logic 0.456ns (8.629%) route 4.828ns (91.371%))
Logic Levels	0
Clock Path Skew	<a href="#">-0.268ns</a>
Clock Uncertainty	<a href="#">0.214ns</a>

Hold :

Summary	
Name	Path 151
Slack (Hold)	<a href="#">0.233ns</a>
Source	<a href="#">divisor_q_reg[2]/C</a> (rising edge-triggered cell FDCE clocked by <a href="#">clk4_my_pll</a> {rise@0.000ns fall@5.000ns period=10.000ns})
Destination	<a href="#">div1_divisor_reg[2]/D</a> (rising edge-triggered cell FDCE clocked by <a href="#">clk1_my_pll</a> {rise@0.000ns fall@15.000ns period=30.000ns})
Path Group	<a href="#">clk1_my_pll</a>
Path Type	Hold (Min at Fast Process Corner)
Requirement	0.000ns ( <a href="#">clk1_my_pll</a> rise@0.000ns - <a href="#">clk4_my_pll</a> rise@0.000ns)
Data Path Delay	0.818ns (logic 0.141ns (17.241%) route 0.677ns (82.759%))
Logic Levels	0
Clock Path Skew	<a href="#">0.285ns</a>
Clock Uncertainty	<a href="#">0.214ns</a>

## From clk2\_my\_pll to clk4\_my\_pll :

### Setup :

Summary	
Name	Path 101
Slack	<a href="#">6.989ns</a>
Source	div2_remainder_registre_reg[7]/C (rising edge-triggered cell FDCE clocked by clk2_my_pll {rise@10.000ns fall@25.000ns period=30.000ns})
Destination	remainder_reg[7]/D (rising edge-triggered cell FDCE clocked by clk4_my_pll {rise@0.000ns fall@5.000ns period=10.000ns})
Path Group	clk4_my_pll
Path Type	Setup (Max at Slow Process Corner)
Requirement	10.000ns (clk4_my_pll rise@20.000ns - clk2_my_pll rise@10.000ns)
Data Path Delay	2.675ns (logic 0.642ns (24.002%) route 2.033ns (75.998%))
Logic Levels	1 (LUT6=1)
Clock Path Skew	<a href="#">-0.201ns</a>
Clock Uncertainty	<a href="#">0.214ns</a>

### Hold :

Summary	
Name	Path 111
Slack (Hold)	<a href="#">0.134ns</a>
Source	div2_quotient_registre_reg[8]/C (rising edge-triggered cell FDCE clocked by clk2_my_pll {rise@10.000ns fall@25.000ns period=30.000ns})
Destination	quotient_reg[8]/D (rising edge-triggered cell FDCE clocked by clk4_my_pll {rise@0.000ns fall@5.000ns period=10.000ns})
Path Group	clk4_my_pll
Path Type	Hold (Min at Fast Process Corner)
Requirement	0.000ns (clk4_my_pll rise@10.000ns - clk2_my_pll rise@10.000ns)
Data Path Delay	0.759ns (logic 0.186ns (24.507%) route 0.573ns (75.493%))
Logic Levels	1 (LUT6=1)
Clock Path Skew	<a href="#">0.320ns</a>
Clock Uncertainty	<a href="#">0.214ns</a>

## From clk4\_my\_pll to clk2\_my\_pll :

### Setup :

Summary	
Name	Path 101
Slack	<a href="#">6.989ns</a>
Source	<a href="#">div2_remainder_registre_reg[7]/C</a> (rising edge-triggered cell FDCE clocked by <a href="#">clk2_my_pll</a> {rise@10.000ns fall@25.000ns period=30.000ns})
Destination	<a href="#">remainder_reg[7]/D</a> (rising edge-triggered cell FDCE clocked by <a href="#">clk4_my_pll</a> {rise@0.000ns fall@5.000ns period=10.000ns})
Path Group	<a href="#">clk4_my_pll</a>
Path Type	Setup (Max at Slow Process Corner)
Requirement	10.000ns ( <a href="#">clk4_my_pll</a> rise@20.000ns - <a href="#">clk2_my_pll</a> rise@10.000ns)
Data Path Delay	2.675ns (logic 0.642ns (24.002%) route 2.033ns (75.998%))
Logic Levels	1 (LUT6=1)
Clock Path Skew	<a href="#">-0.201ns</a>
Clock Uncertainty	<a href="#">0.214ns</a>

### Hold :

Summary	
Name	Path 171
Slack (Hold)	<a href="#">0.232ns</a>
Source	<a href="#">divisor_q_reg[4]/C</a> (rising edge-triggered cell FDCE clocked by <a href="#">clk4_my_pll</a> {rise@0.000ns fall@5.000ns period=10.000ns})
Destination	<a href="#">div2_divisor_reg[4]/D</a> (rising edge-triggered cell FDCE clocked by <a href="#">clk2_my_pll</a> {rise@10.000ns fall@25.000ns period=30.000ns})
Path Group	<a href="#">clk2_my_pll</a>
Path Type	Hold (Min at Fast Process Corner)
Requirement	0.000ns ( <a href="#">clk2_my_pll</a> rise@10.000ns - <a href="#">clk4_my_pll</a> rise@10.000ns)
Data Path Delay	0.820ns (logic 0.141ns (17.193%) route 0.679ns (82.807%))
Logic Levels	0
Clock Path Skew	<a href="#">0.312ns</a>
Clock Uncertainty	<a href="#">0.214ns</a>

## From clk3\_my\_pll to clk4\_my\_pll :

### Setup :

Summary	
Name	Path 121
Slack	<a href="#">6.888ns</a>
Source	<a href="#">div3_remainder_registre_reg[3]/C</a> (rising edge-triggered cell FDCE clocked by <a href="#">clk3_my_pll</a> {rise@20.000ns fall@35.000ns period=30.000ns})
Destination	<a href="#">remainder_reg[3]/D</a> (rising edge-triggered cell FDCE clocked by <a href="#">clk4_my_pll</a> {rise@0.000ns fall@5.000ns period=10.000ns})
Path Group	<a href="#">clk4_my_pll</a>
Path Type	Setup (Max at Slow Process Corner)
Requirement	10.000ns ( <a href="#">clk4_my_pll</a> rise@30.000ns - <a href="#">clk3_my_pll</a> rise@20.000ns)
Data Path Delay	2.643ns (logic 0.642ns (24.291%) route 2.001ns (75.709%))
Logic Levels	1 (LUT6=1)
Clock Path Skew	<a href="#">-0.284ns</a>
Clock Uncertainty	<a href="#">0.214ns</a>

### Hold :

Summary	
Name	Path 131
Slack (Hold)	<a href="#">0.186ns</a>
Source	<a href="#">div3_quotient_registre_reg[2]/C</a> (rising edge-triggered cell FDCE clocked by <a href="#">clk3_my_pll</a> {rise@20.000ns fall@35.000ns period=30.000ns})
Destination	<a href="#">quotient_reg[2]/D</a> (rising edge-triggered cell FDCE clocked by <a href="#">clk4_my_pll</a> {rise@0.000ns fall@5.000ns period=10.000ns})
Path Group	<a href="#">clk4_my_pll</a>
Path Type	Hold (Min at Fast Process Corner)
Requirement	0.000ns ( <a href="#">clk4_my_pll</a> rise@20.000ns - <a href="#">clk3_my_pll</a> rise@20.000ns)
Data Path Delay	0.810ns (logic 0.209ns (25.795%) route 0.601ns (74.205%))
Logic Levels	1 (LUT6=1)
Clock Path Skew	<a href="#">0.320ns</a>
Clock Uncertainty	<a href="#">0.214ns</a>

## From clk4\_my\_pll to clk3\_my\_pll :

### Setup :

<b>Summary</b>	
Name	Path 181
Slack	<u>5.512ns</u>
Source	divisor_q_reg[11]/C (rising edge-triggered cell FDCE clocked by clk4_my_pll {rise@0.000ns fall@5.000ns period=10.000ns})
Destination	div3_divisor_reg[11]_rep/D (rising edge-triggered cell FDCE clocked by clk3_my_pll {rise@20.000ns fall@35.000ns period=30.000ns})
Path Group	clk3_my_pll
Path Type	Setup (Max at Slow Process Corner)
Requirement	10.000ns (clk3_my_pll rise@20.000ns - clk4_my_pll rise@10.000ns)
Data Path Delay	4.017ns (logic 0.456ns (11.351%) route 3.561ns (88.649%))
Logic Levels	0
Clock Path Skew	<u>-0.190ns</u>
Clock Uncertainty	<u>0.214ns</u>

### Hold :

<b>Summary</b>	
Name	Path 191
Slack (Hold)	<u>0.193ns</u>
Source	dividend_q_reg[9]/C (rising edge-triggered cell FDCE clocked by clk4_my_pll {rise@0.000ns fall@5.000ns period=10.000ns})
Destination	div3_dividend_reg[9]/D (rising edge-triggered cell FDCE clocked by clk3_my_pll {rise@20.000ns fall@35.000ns period=30.000ns})
Path Group	clk3_my_pll
Path Type	Hold (Min at Fast Process Corner)
Requirement	0.000ns (clk3_my_pll rise@20.000ns - clk4_my_pll rise@20.000ns)
Data Path Delay	0.788ns (logic 0.141ns (17.894%) route 0.647ns (82.106%))
Logic Levels	0
Clock Path Skew	<u>0.323ns</u>
Clock Uncertainty	<u>0.214ns</u>

J'obtiens finalement :

#### Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): <u>1.362 ns</u>	Worst Hold Slack (WHS): <u>0.134 ns</u>	Worst Pulse Width Slack (WPWS): <u>3.000 ns</u>
Total Negative Slack (TNS): <u>0.000 ns</u>	Total Hold Slack (THS): <u>0.000 ns</u>	Total Pulse Width Negative Slack (TPWS): <u>0.000 ns</u>
Number of Failing Endpoints: <u>0</u>	Number of Failing Endpoints: <u>0</u>	Number of Failing Endpoints: <u>0</u>
Total Number of Endpoints: <u>177</u>	Total Number of Endpoints: <u>177</u>	Total Number of Endpoints: <u>213</u>

All user specified timing constraints are met.

Tous les Slacks sont positifs.

### Relevé :

- Slack = WNS = 1.362 ns
- WNS ≥ 0 et WHS ≥ 0

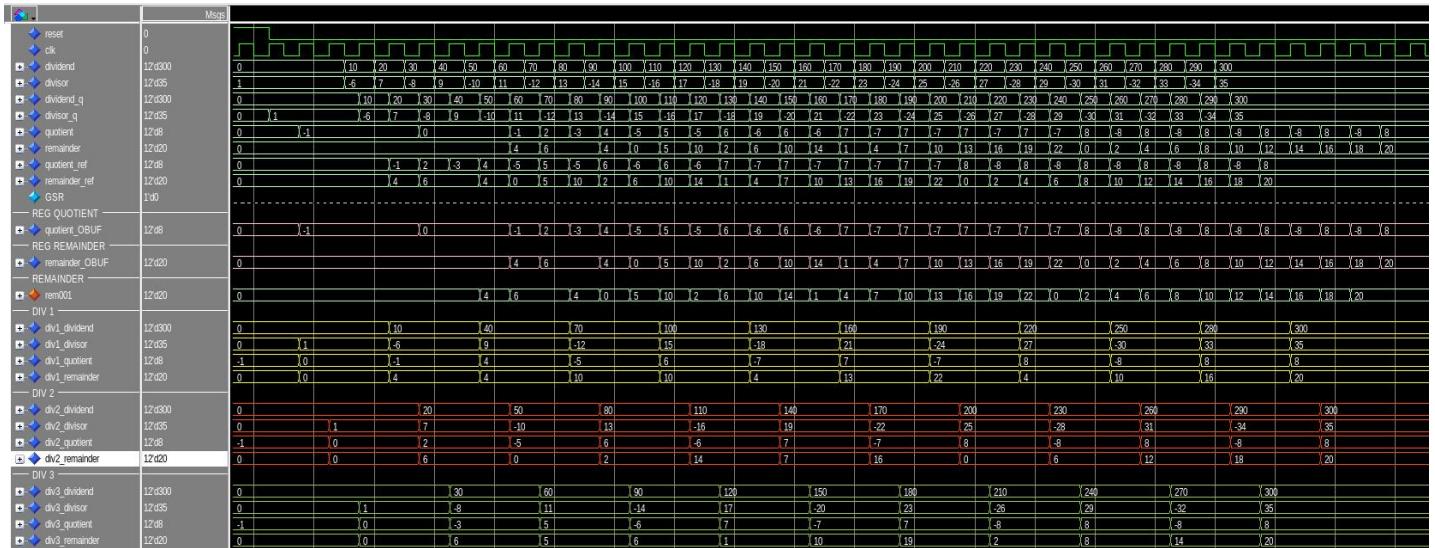
### Calcul fréquence maximale :

$$f_{max} = \frac{1}{(period - WNS) * 10^{-9}} = \frac{1}{(10 - 1.362) * 10^{-9}} = 115\ 767\ 538\ Hz$$

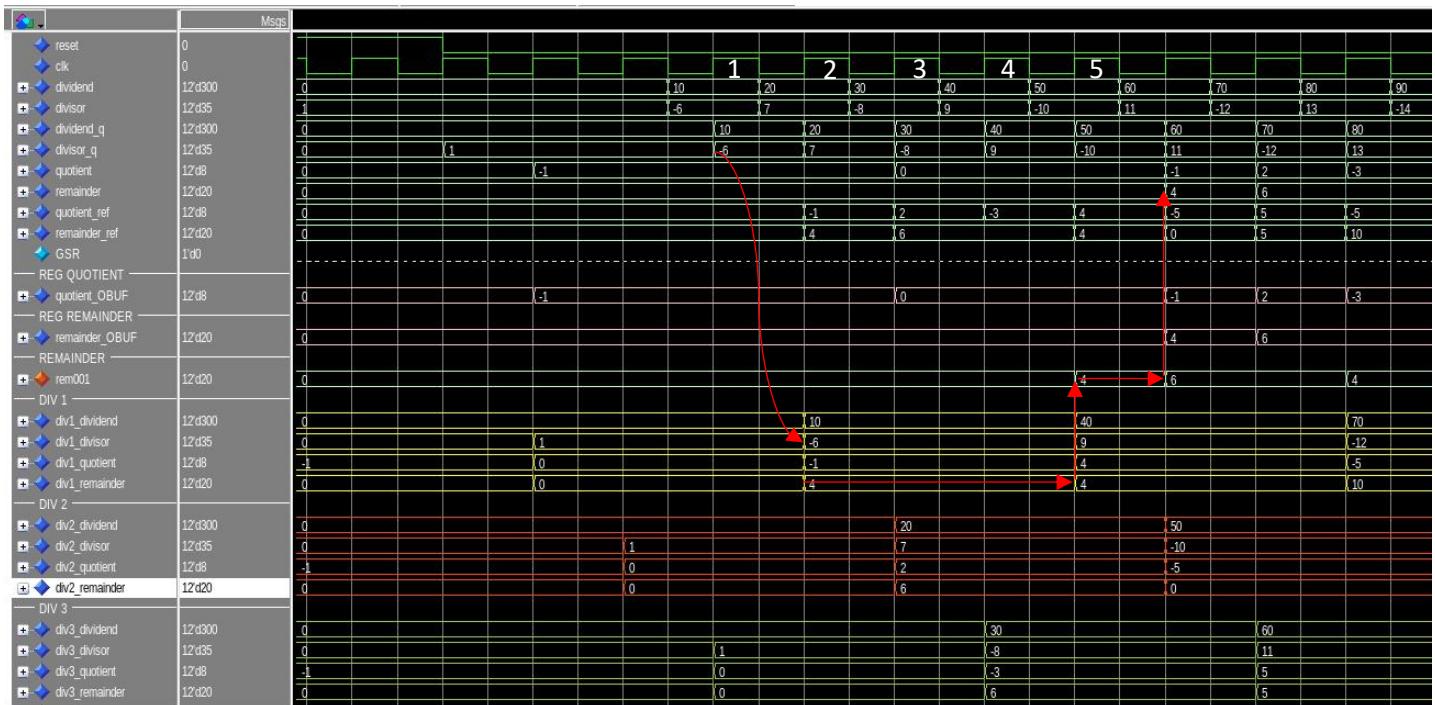
## Simulation

Simulation comportementale post-implémentation :

J'obtiens la vue globale :

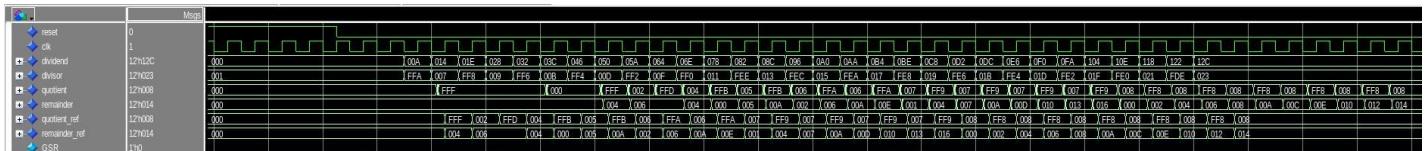


## Séquencement :

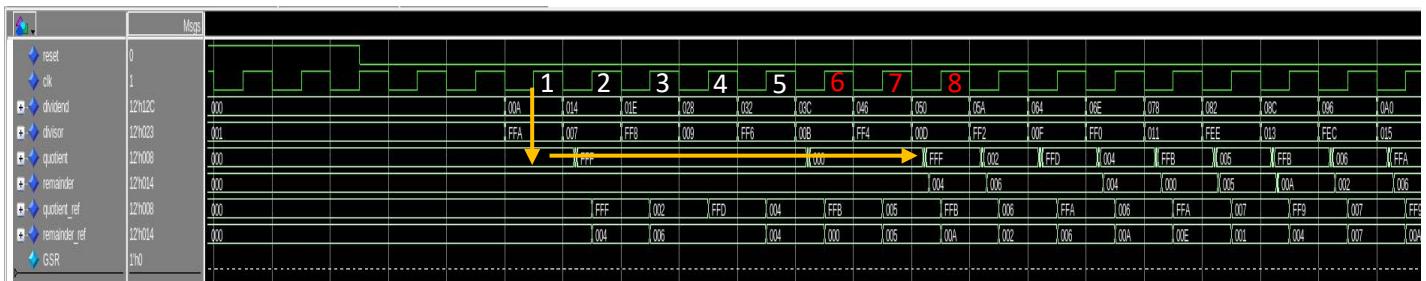


### Simulation post-implémentation avec prise en compte des délais :

J'obtiens la vue globale :



## Séquencement :



Il y a une latence non négligeable au départ. C'est au bout de 8 périodes d'horloges que l'architecture est capable de nous fournir une donnée utile.

La latence est du au délai de routage

## Chemin critique

Max Delay Paths				Point de départ du chemin critique
Slack (MET) :	1.362ns (required time - arrival time)			
Source:	div1_divisor_reg[0]/C			
period=30.000ns})	(rising edge-triggered cell FDCE clocked by clk1_my_pll {rise@0.000ns fall@15.000ns}			
Destination:	div1_quotient_registro[10]/D			Horloge de source
period=30.000ns})	(rising edge-triggered cell FDCE clocked by clk1_my_pll {rise@0.000ns fall@15.000ns}			Horloge de destination
Path Group:	cikl_my_pll			
Path Type:	Setup (Max at Slow Process Corner)			
Requirement:	30.000ns (clk1_my_pll rise@30.000ns - clk1_my_pll rise@0.000ns)			
Data Path Delay:	28.526ns (logic 11.352ns (39.795%) route 17.174ns (60.205%))			
Logic Levels:	33 (CARRY4=17 LUT2=1 LUT4=6 LUT5=2 LUT6=7)			
Clock Path Skew:	-0.047ns (DCD - SCD + CPR)			
Destination Clock Delay (DCD):	-2.627ns = ( 27.373 - 30.000 )			
Source Clock Delay (SCD):	-2.945ns			
Clock Pessimism Removal (CPR):	-0.365ns			
Clock Uncertainty:	0.094ns ((TSJ^2 + DJ^2)^1/2) / 2 + PE			
Total System Jitter (TSJ):	0.071ns			
Discrete Jitter (DJ):	0.173ns			
Phase Error (PE):	0.000ns			
Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
	(clock clk1_my_pll rise edge)			
N15		0.000	0.000 r	
	net (fo=0)	0.000	0.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.948	0.948 r	tp1_pll/inst/clk_in1
	net (fo=1, routed)	1.253	2.201	tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT0)	-8.590	-6.389 r	tp1_pll/inst/plle2_adv_inst/CLKOUT0
	net (fo=1, routed)	1.704	-4.685	tp1_pll/inst/clk1_my_pll
BUFGCTRL_X0Y1	BUFG (Prop_bufg_I_O)	0.096	-4.589 r	tp1_pll/inst/clkout1_buf/O
	net (fo=50, routed)	1.643	-2.945	clk1
SLICE_X11Y90	FDCE		r	div1_divisor_reg[0]/C
SLICE_X11Y90	FDCE (Prop_fdce_C_Q)	0.456	-2.489 r	div1_divisor_reg[0]/Q
	net (fo=27, routed)	1.131	-1.358	div1/div1_divisor[0]
SLICE_X8Y94	LUT2 (Prop_lut2_I0_O)	0.124	-1.234 r	div1/i_carry_i_5_62/O
	net (fo=1, routed)	0.000	-1.234	div1/i_carry_i_5_62_n_0
SLICE_X8Y94	CARRY4 (Prop_carry4_S[0]_O[0])	0.252	-0.982 r	div1/partial_rem0_inferred_0/i_carry/O[0]
	net (fo=3, routed)	0.971	-0.011	div1/partial_rem0_inferred_0/i_carry_n[0]
SLICE_X9Y91	LUT5 (Prop_lut5_I0_O)	0.295	0.284 r	div1/i_carry_i_6/O
	net (fo=1, routed)	0.000	0.284	div1/i_carry_i_6_n_0
SLICE_X9Y91	CARRY4 (Prop_carry4_S[1]_O[2])	0.580	0.864 r	div1/partial_rem0_inferred_2/i_carry/O[2]
	net (fo=3, routed)	0.832	1.697	div1/partial_rem0_inferred_2/i_carry_n_5
SLICE_X8Y93	LUT6 (Prop_lut6_I5_O)	0.302	1.999 r	div1/i_carry_i_1_9/O
	net (fo=1, routed)	0.619	2.617	div1/i_carry_i_1_9_n_0
SLICE_X10Y94	CARRY4 (Prop_carry4_DI[3]_CO[3])	0.396	3.013 r	div1/partial_rem0_inferred_4/i_carry/CO[3]
	net (fo=1, routed)	0.000	3.013	div1/partial_rem0_inferred_4/i_carry_n_0
SLICE_X10Y95	CARRY4 (Prop_carry4_CI_O[1])	0.323	3.336 r	div1/partial_rem0_inferred_4/i_carry_0/O[1]
	net (fo=3, routed)	0.748	4.084	div1/partial_rem0_inferred_4/i_carry_0_n_6
SLICE_X13Y94	LUT4 (Prop_lut4_I3_O)	0.306	4.390 r	div1/i_carry_0_i_2_44/O
	net (fo=1, routed)	0.000	4.390	div1/i_carry_0_i_2_44_n_0
SLICE_X13Y94	CARRY4 (Prop_carry4_S[2]_CO[3])	0.398	4.788 r	div1/partial_rem0_inferred_5/i_carry_0/CO[3]
	net (fo=1, routed)	0.000	4.788	div1/partial_rem0_inferred_5/i_carry_0_n_0
SLICE_X13Y95	CARRY4 (Prop_carry4_CI_O[0])	0.222	5.010 r	div1/partial_rem0_inferred_5/i_carry_1/O[0]
	net (fo=3, routed)	0.574	5.585	div1/partial_rem0_inferred_5/i_carry_1_n_7
SLICE_X12Y97	LUT6 (Prop_lut6_I0_O)	0.299	5.884 r	div1/i_carry_1_i_2_7/O
	net (fo=1, routed)	0.703	6.587	div1/i_carry_1_i_2_7_n_0
SLICE_X15Y93	CARRY4 (Prop_carry4_DI[1]_O[3])	0.596	7.183 r	div1/partial_rem0_inferred_8/i_carry_1/O[3]
	net (fo=20, routed)	0.972	8.155	div1/partial_rem0_inferred_8/i_carry_1_n_4
SLICE_X13Y88	LUT4 (Prop_lut4_I1_O)	0.306	8.461 r	div1/i_carry_i_5_4/O
	net (fo=20, routed)	0.741	9.202	div1/i_carry_i_5_4_n_0
SLICE_X14Y86	LUT4 (Prop_lut4_I2_O)	0.124	9.326 r	div1/i_carry_i_3_41/O
	net (fo=1, routed)	0.000	9.326	div1/i_carry_i_3_41_n_0
SLICE_X14Y86	CARRY4 (Prop_carry4_S[1]_O[2])	0.578	9.904 r	div1/partial_rem0_inferred_11/i_carry/O[2]
	net (fo=3, routed)	1.072	10.976	div1/partial_rem0_inferred_11/i_carry_n_5
SLICE_X29Y85	LUT4 (Prop_lut4_I1_O)	0.301	11.277 r	div1/i_carry_i_1_40/O
	net (fo=1, routed)	0.000	11.277	div1/i_carry_i_1_40_n_0

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SLICE_X29Y85	CARRY4 (Prop_carry4_S[3]_CO[3])	0.401	11.678 r	div1/partial_rem0_inferred_13/i_carry/CO[3]
	net (fo=1, routed)	0.000	11.678	div1/partial_rem0_inferred_13/i_carry_n_0
SLICE_X29Y86	CARRY4 (Prop_carry4_CI_O[0])	0.222	11.900 r	div1/partial_rem0_inferred_13/i_carry_0/O[0]
	net (fo=3, routed)	0.973	12.873	div1/partial_rem0_inferred_13/i_carry_0_n_7
SLICE_X30Y82	LUT6 (Prop_lut6_I0_O)	0.299	13.172 r	div1/i_carry_0_i_3_3/O
	net (fo=1, routed)	0.488	13.660	div1/i_carry_0_i_3_3_n_0
SLICE_X28Y82	CARRY4 (Prop_carry4_DI[1]_CO[3])	0.507	14.167 r	div1/partial_rem0_inferred_16/i_carry_0/CO[3]
	net (fo=1, routed)	0.000	14.167	div1/partial_rem0_inferred_16/i_carry_0_n_0
SLICE_X28Y83	CARRY4 (Prop_carry4_CI_O[0])	0.222	14.389 r	div1/partial_rem0_inferred_16/i_carry_1/O[0]
	net (fo=3, routed)	0.962	15.351	div1/partial_rem0_inferred_16/i_carry_1_n_7
SLICE_X29Y79	LUT4 (Prop_lut4_I0_O)	0.299	15.650 r	div1/i_carry_1_i_7_2/O
	net (fo=1, routed)	0.000	15.650	div1/i_carry_1_i_7_2_n_0
SLICE_X29Y79	CARRY4 (Prop_carry4_S[1]_O[3])	0.640	16.290 r	div1/partial_rem0_inferred_18/i_carry_1/O[3]
	net (fo=3, routed)	0.709	16.999	div1/partial_rem0_inferred_18/i_carry_1_n_4
SLICE_X15Y78	LUT6 (Prop_lut6_I0_O)	0.306	17.305 r	div1/i_carry_i_5/O
	net (fo=57, routed)	1.087	18.393	div1/i_carry_i_5_n_0
SLICE_X14Y71	LUT4 (Prop_lut4_I2_O)	0.124	18.517 r	div1/i_carry_i_3_36/O
	net (fo=1, routed)	0.000	18.517	div1/i_carry_i_3_36_n_0
SLICE_X14Y71	CARRY4 (Prop_carry4_S[1]_CO[3])	0.533	19.050 r	div1/partial_rem0_inferred_21/i_carry/CO[3]
	net (fo=1, routed)	0.000	19.050	div1/partial_rem0_inferred_21/i_carry_n_0
SLICE_X14Y72	CARRY4 (Prop_carry4_CI_O[0])	0.219	19.269 r	div1/partial_rem0_inferred_21/i_carry_0/O[0]
	net (fo=3, routed)	0.642	19.911	div1/partial_rem0_inferred_21/i_carry_0_n_7
SLICE_X14Y70	LUT6 (Prop_lut6_I0_O)	0.295	20.206 r	div1/sum0_carry_0_i_3/O
	net (fo=5, routed)	0.821	21.027	div1/sum0_carry_0_i_3_n_0
SLICE_X12Y72	CARRY4 (Prop_carry4_DI[0]_CO[3])	0.550	21.577 r	div1/sum0_carry_0/CO[3]
	net (fo=1, routed)	0.000	21.577	div1/sum0_carry_0_n_0
SLICE_X12Y73	CARRY4 (Prop_carry4_CI_O[1])	0.323	21.900 r	div1/sum0_carry_1/O[1]
	net (fo=2, routed)	1.036	22.936	div1/sum0[9]
SLICE_X10Y71	LUT5 (Prop_lut5_I1_O)	0.306	23.242 r	div1/div1_quotient_registre[11]_i_10/O
	net (fo=1, routed)	0.504	23.745	div1/div1_quotient_registre[11]_i_10_n_0
SLICE_X11Y71	LUT6 (Prop_lut6_I5_O)	0.124	23.869 r	div1/div1_quotient_registre[11]_i_3/O
	net (fo=24, routed)	1.588	25.457	div1/div1_quotient_registre[11]_i_3_n_0
SLICE_X9Y85	LUT6 (Prop_lut6_I2_O)	0.124	25.581 r	div1/div1_quotient_registre[10]_i_1/O
	net (fo=1, routed)	0.000	25.581	div1_quotient[10]
SLICE_X9Y85	FDCE		r	div1_quotient_registre[10]/D
<hr/>				
(clock clk1_my_pll rise edge)				
N15		30.000	30.000 r	
		0.000	30.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.814	30.814 r	tp1_pll/inst/clk_in1
	net (fo=1, routed)	1.181	31.995	tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT0)	-7.855	24.141 r	tp1_pll/inst/plle2_adv_inst/CLKOUT0
	net (fo=1, routed)	1.625	25.766	tp1_pll/inst/clk1_my_pll
BUFGCTRL_X0Y1	BUFQ (Prop_bufq_I_O)	0.091	25.857 r	tp1_pll/inst/clkout1_buf/O
	net (fo=50, routed)	1.516	27.373	clk1
SLICE_X9Y85	FDCE		r	div1_quotient_registre[10]/C
	clock pessimism	-0.365	27.008	
	clock uncertainty	-0.094	26.914	
SLICE_X9Y85	FDCE (Setup_fdce_C_D)	0.029	26.943	div1_quotient_registre[10]
<hr/>				
	required time		26.943	
	arrival time		-25.581	
<hr/>				
slack	1.362			

Le chemin critique se trouve dans le niveau hiérarchique div1 entre le bit numéro 0 du registre div1\_divisor\_reg et le bit numéro 10 du registre div1\_quotient\_registre .

Ici, il traverse 16 LUT.

Il traverse 17 CARRY 4 c'est-à-dire des additionneurs.

## Annexe : Analyse de rapport Architecture n°2

### From Clock: clk1\_my\_pll To Clock: clk1\_my\_pll

Max Delay Paths

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Slack (MET) : 1.362ns (required time - arrival time)
Source: div1_divisor_reg[0]/C
(rising edge-triggered cell FDCE clocked by clk1_my_pll {rise@0.000ns
fall@15.000ns period=30.000ns})
Destination: div1_quotient_registro_reg[10]/D
(rising edge-triggered cell FDCE clocked by clk1_my_pll {rise@0.000ns
fall@15.000ns period=30.000ns})
Path Group: clk1_my_pll
Path Type: Setup (Max at Slow Process Corner)
Requirement: 30.000ns (clk1_my_pll rise@30.000ns - clk1_my_pll rise@0.000ns)
Data Path Delay: 28.526ns (logic 11.352ns (39.795%) route 17.174ns (60.205%))
Logic Levels: 33 (CARRY4=17 LUT2=1 LUT4=6 LUT5=2 LUT6=7)
Clock Path Skew: -0.047ns (DCD - SCD + CPR)
Destination Clock Delay (DCD): -2.627ns = ( 27.373 - 30.000 )
Source Clock Delay (SCD): -2.945ns
Clock Pessimism Removal (CPR): -0.365ns
Clock Uncertainty: 0.094ns ((TSJ^2 + DJ^2)^1/2) / 2 + PE
Total System Jitter (TSJ): 0.071ns
Discrete Jitter (DJ): 0.173ns
Phase Error (PE): 0.000ns
```

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock clk1_my_pll rise edge)				
N15		0.000	0.000 r	
		0.000	0.000 r	clk (IN)
N15	net (fo=0)	0.000	0.000	tp1_pll/inst/clk_in1
	IBUF (Prop_ibuf_I_O)	0.948	0.948 r	tp1_pll/inst/clkin1_ibufg/O
	net (fo=1, routed)	1.253	2.201	tp1_pll/inst/clk_in1_my_pll
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT0)	-8.590	-6.389 r	tp1_pll/inst/plle2_adv_inst/CLKOUT0
	net (fo=1, routed)	1.704	-4.685	tp1_pll/inst/clk1_my_pll
BUFGCTRL_X0Y1	BUFG (Prop_bufg_I_O)	0.096	-4.589 r	tp1_pll/inst/clkout1_buf/O
	net (fo=50, routed)	1.643	-2.945	clk1
SLICE_X11Y90	FDCE		r	div1_divisor_reg[0]/C
SLICE_X11Y90	FDCE (Prop_fdce_C_Q)	0.456	-2.489 r	div1_divisor_reg[0]/Q
	net (fo=27, routed)	1.131	-1.358	div1/div1_divisor[0]
SLICE_X8Y94	LUT2 (Prop_lut2_I0_O)	0.124	-1.234 r	div1/i_carry_i_5_62/O
	net (fo=1, routed)	0.000	-1.234	div1/i_carry_i_5_62_n_0
SLICE_X8Y94	CARRY4 (Prop_carry4_S[0]_O[0])	0.252	-0.982 r	div1/partial_rem0_inferred_0/i_carry/O[0]
	net (fo=3, routed)	0.971	-0.011	div1/partial_rem0_inferred_0/i_carry/n[0]
SLICE_X9Y91	LUT5 (Prop_lut5_I0_O)	0.295	0.284 r	div1/i_carry_i_6/O
	net (fo=1, routed)	0.000	0.284	div1/i_carry_i_6_n_0
SLICE_X9Y91	CARRY4 (Prop_carry4_S[1]_O[2])	0.580	0.864 r	div1/partial_rem0_inferred_2/i_carry/O[2]
	net (fo=3, routed)	0.832	1.697	div1/partial_rem0_inferred_2/i_carry/n_5
SLICE_X8Y93	LUT6 (Prop_lut6_I5_O)	0.302	1.999 r	div1/i_carry_i_1_9/O
	net (fo=1, routed)	0.619	2.617	div1/i_carry_i_1_9_n_0
SLICE_X10Y94	CARRY4 (Prop_carry4_DI[3]_CO[3])	0.396	3.013 r	div1/partial_rem0_inferred_4/i_carry/CO[3]
	net (fo=1, routed)	0.000	3.013	div1/partial_rem0_inferred_4/i_carry/n_0
SLICE_X10Y95	CARRY4 (Prop_carry4_CI_O[1])	0.323	3.336 r	div1/partial_rem0_inferred_4/i_carry_0/O[1]
	net (fo=3, routed)	0.748	4.084	div1/partial_rem0_inferred_4/i_carry_0_n_6
SLICE_X13Y94	LUT4 (Prop_lut4_I3_O)	0.306	4.390 r	div1/i_carry_0_i_2_44/O
	net (fo=1, routed)	0.000	4.390	div1/i_carry_0_i_2_44_n_0
SLICE_X13Y94	CARRY4 (Prop_carry4_S[2]_CO[3])	0.398	4.788 r	div1/partial_rem0_inferred_5/i_carry_0/CO[3]
	net (fo=1, routed)	0.000	4.788	div1/partial_rem0_inferred_5/i_carry_0_n_0
SLICE_X13Y95	CARRY4 (Prop_carry4_CI_O[0])	0.222	5.010 r	div1/partial_rem0_inferred_5/i_carry_1/O[0]
	net (fo=3, routed)	0.574	5.585	div1/partial_rem0_inferred_5/i_carry_1_n_7
SLICE_X12Y97	LUT6 (Prop_lut6_I0_O)	0.299	5.884 r	div1/i_carry_1_i_2_7/O
	net (fo=1, routed)	0.703	6.587	div1/i_carry_1_i_2_7_n_0
SLICE_X15Y93	CARRY4 (Prop_carry4_DI[1]_O[3])	0.596	7.183 r	div1/partial_rem0_inferred_8/i_carry_1/O[3]
	net (fo=20, routed)	0.972	8.155	div1/partial_rem0_inferred_8/i_carry_1_n_4
SLICE_X13Y88	LUT4 (Prop_lut4_I1_O)	0.306	8.461 r	div1/i_carry_5_4/O
	net (fo=20, routed)	0.741	9.202	div1/i_carry_5_4_n_0

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SLICE_X14Y86	LUT4 (Prop_lut4_I2_O)	0.124	9.326	r	div1/i_carry_i_3_41/O
SLICE_X14Y86	net (fo=1, routed)	0.000	9.326		div1/i_carry_i_3_41_n_0
SLICE_X14Y86	CARRY4 (Prop_carry4_S[1]_O[2])	0.578	9.904	r	div1/partial_rem0_inferred_11/i_carry/O[2]
SLICE_X29Y85	net (fo=3, routed)	1.072	10.976		div1/partial_rem0_inferred_11/i_carry_n_5
SLICE_X29Y85	LUT4 (Prop_lut4_I1_O)	0.301	11.277	r	div1/i_carry_i_1_40/O
SLICE_X29Y85	net (fo=1, routed)	0.000	11.277		div1/i_carry_i_1_40_n_0
SLICE_X29Y85	CARRY4 (Prop_carry4_S[3]_CO[3])	0.401	11.678	r	div1/partial_rem0_inferred_13/i_carry/CO[3]
SLICE_X29Y86	net (fo=1, routed)	0.000	11.678		div1/partial_rem0_inferred_13/i_carry_n_0
SLICE_X29Y86	CARRY4 (Prop_carry4_CI_O[0])	0.222	11.900	r	div1/partial_rem0_inferred_13/i_carry_0/O[0]
SLICE_X30Y82	net (fo=3, routed)	0.973	12.873		div1/partial_rem0_inferred_13/i_carry_0_n_7
SLICE_X30Y82	LUT6 (Prop_lut6_I0_O)	0.299	13.172	r	div1/i_carry_0_i_3_3/O
SLICE_X28Y82	net (fo=1, routed)	0.488	13.660		div1/i_carry_0_i_3_3_n_0
SLICE_X28Y82	CARRY4 (Prop_carry4_DI[1]_CO[3])	0.507	14.167	r	div1/partial_rem0_inferred_16/i_carry_0/CO[3]
SLICE_X28Y83	net (fo=1, routed)	0.000	14.167		div1/partial_rem0_inferred_16/i_carry_0_n_0
SLICE_X28Y83	CARRY4 (Prop_carry4_CI_O[0])	0.222	14.389	r	div1/partial_rem0_inferred_16/i_carry_1/O[0]
SLICE_X29Y79	net (fo=3, routed)	0.962	15.351		div1/partial_rem0_inferred_16/i_carry_1_n_7
SLICE_X29Y79	LUT4 (Prop_lut4_I0_O)	0.299	15.650	r	div1/i_carry_1_i_7_2/O
SLICE_X29Y79	net (fo=1, routed)	0.000	15.650		div1/i_carry_1_i_7_2_n_0
SLICE_X29Y79	CARRY4 (Prop_carry4_S[1]_O[3])	0.640	16.290	r	div1/partial_rem0_inferred_18/i_carry_1/O[3]
SLICE_X15Y78	net (fo=3, routed)	0.709	16.999		div1/partial_rem0_inferred_18/i_carry_1_n_4
SLICE_X15Y78	LUT6 (Prop_lut6_I0_O)	0.306	17.305	r	div1/i_carry_i_5/O
SLICE_X14Y71	net (fo=57, routed)	1.087	18.393		div1/i_carry_i_5_n_0
SLICE_X14Y71	LUT4 (Prop_lut4_I2_O)	0.124	18.517	r	div1/i_carry_i_3_36/O
SLICE_X14Y71	net (fo=1, routed)	0.000	18.517		div1/i_carry_i_3_36_n_0
SLICE_X14Y71	CARRY4 (Prop_carry4_S[1]_CO[3])	0.533	19.050	r	div1/partial_rem0_inferred_21/i_carry/CO[3]
SLICE_X14Y72	net (fo=1, routed)	0.000	19.050		div1/partial_rem0_inferred_21/i_carry_n_0
SLICE_X14Y72	CARRY4 (Prop_carry4_CI_O[0])	0.219	19.269	r	div1/partial_rem0_inferred_21/i_carry_0/O[0]
SLICE_X14Y70	net (fo=3, routed)	0.642	19.911		div1/partial_rem0_inferred_21/i_carry_0_n_7
SLICE_X14Y70	LUT6 (Prop_lut6_I0_O)	0.295	20.206	r	div1/sum0_carry_0_i_3/O
SLICE_X12Y72	net (fo=5, routed)	0.821	21.027		div1/sum0_carry_0_i_3_n_0
SLICE_X12Y72	CARRY4 (Prop_carry4_DI[0]_CO[3])	0.550	21.577	r	div1/sum0_carry_0/CO[3]
SLICE_X12Y73	net (fo=1, routed)	0.000	21.577		div1/sum0_carry_0_n_0
SLICE_X12Y73	CARRY4 (Prop_carry4_CI_O[1])	0.323	21.900	r	div1/sum0_carry_1/O[1]
SLICE_X10Y71	net (fo=2, routed)	1.036	22.936		div1/sum0[9]
SLICE_X10Y71	LUT5 (Prop_lut5_I1_O)	0.306	23.242	r	div1/div1_quotient_registre[11]_i_10/O
SLICE_X11Y71	net (fo=1, routed)	0.504	23.745		div1/div1_quotient_registre[11]_i_10_n_0
SLICE_X11Y71	LUT6 (Prop_lut6_I5_O)	0.124	23.869	r	div1/div1_quotient_registre[11]_i_3/O
SLICE_X9Y85	net (fo=24, routed)	1.588	25.457		div1/div1_quotient_registre[11]_i_3_n_0
SLICE_X9Y85	LUT6 (Prop_lut6_I2_O)	0.124	25.581	r	div1/div1_quotient_registre[10]_i_1/O
SLICE_X9Y85	net (fo=1, routed)	0.000	25.581		div1/quotient[10]
SLICE_X9Y85	FDCE			r	div1/quotient_registre[10]/D
<hr/>					
(clock clk1_my_pll rise edge)					
N15		30.000	30.000	r	
N15	net (fo=0)	0.000	30.000	r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.814	30.814	r	tp1_pll/inst/clk_in1
PLLE2_ADV_X0Y1	net (fo=1, routed)	1.181	31.995		tp1_pll/inst/clk_in1_my_pll
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT0)	-7.855	24.141	r	tp1_pll/inst/plle2_adv_inst/CLKOUT0
BUFGCTRL_X0Y1	net (fo=1, routed)	1.625	25.766		tp1_pll/inst/clk1_my_pll
BUFGCTRL_X0Y1	BUFG (Prop_bufg_I_O)	0.091	25.857	r	tp1_pll/inst/clkout1_buf/O
SLICE_X9Y85	net (fo=50, routed)	1.516	27.373		clk1
SLICE_X9Y85	FDCE			r	div1/quotient_registre[10]/C
SLICE_X9Y85	clock pessimism	-0.365	27.008		
SLICE_X9Y85	clock uncertainty	-0.094	26.914		
SLICE_X9Y85	FDCE (Setup_fdce_C_D)	0.029	26.943		div1/quotient_registre[10]
<hr/>					
required time					
arrival time					
<hr/>					
slack					
1.362					

From Clock: clk1\_my\_pll To Clock: clk1\_my\_pll

Min Delay Paths

Slack (MET) : 0.346ns (arrival time - required time)  
 Source: div1\_divisor\_reg[11]/C  
     (rising edge-triggered cell FDCE clocked by clk1\_my\_pll {rise@0.000ns fall@15.000ns period=30.000ns})  
 Destination: div1\_quotient\_registro[1]/D  
     (rising edge-triggered cell FDCE clocked by clk1\_my\_pll {rise@0.000ns fall@15.000ns period=30.000ns})  
 Path Group: clk1\_my\_pll  
**Path Type:** Hold (Min at Fast Process Corner)  
 Requirement: 0.000ns (clk1\_my\_pll rise@0.000ns - clk1\_my\_pll rise@0.000ns)  
 Data Path Delay: 0.500ns (logic 0.209ns (41.776%) route 0.291ns (58.224%))  
 Logic Levels: 1 (LUT6=1)  
 Clock Path Skew: 0.034ns (DCD - SCD - CPR)  
 Destination Clock Delay (DCD): -0.398ns  
 Source Clock Delay (SCD): -0.625ns  
 Clock Pessimism Removal (CPR): 0.194ns

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock clk1_my_pll rise edge)				
N15		0.000	0.000 r	
	net (fo=0)	0.000	0.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.177	0.177 r	tp1_pll/inst/clk_in1
	net (fo=1, routed)	0.440	0.617	tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT0)	-2.339	-1.722 r	tp1_pll/inst/plle2_adv_inst/CLKOUT0
	net (fo=1, routed)	0.510	-1.212	tp1_pll/inst/clk1_my_pll
BUFGCTRL_X0Y1	BUFG (Prop_bufg_I_O)	0.026	-1.186 r	tp1_pll/inst/clkout1_buf/O
	net (fo=50, routed)	0.561	-0.625	clk1
SLICE_X8Y76	FDCE		r	div1_divisor_reg[11]/C
(clock clk1_my_pll rise edge)				
SLICE_X8Y76	FDCE (Prop_fdce_C_Q)	0.164	-0.461 r	div1_divisor_reg[11]/Q
	net (fo=9, routed)	0.291	-0.170	div1/div1_divisor[11]
SLICE_X12Y76	LUT6 (Prop_lut6_I4_O)	0.045	-0.125 r	div1/div1_quotient_registro[1]_i_1/O
	net (fo=1, routed)	0.000	-0.125	div1_quotient[1]
SLICE_X12Y76	FDCE		r	div1_quotient_registro[1]/D

N15		0.000	0.000 r	
	net (fo=0)	0.000	0.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.365	0.365 r	tp1_pll/inst/clk_in1
	net (fo=1, routed)	0.481	0.846	tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT0)	-2.657	-1.811 r	tp1_pll/inst/plle2_adv_inst/CLKOUT0
	net (fo=1, routed)	0.556	-1.255	tp1_pll/inst/clk1_my_pll
BUFGCTRL_X0Y1	BUFG (Prop_bufg_I_O)	0.029	-1.226 r	tp1_pll/inst/clkout1_buf/O
	net (fo=50, routed)	0.829	-0.398	clk1
SLICE_X12Y76	FDCE		r	div1_quotient_registro[1]/C
	clock pessimism	-0.194	-0.591	
SLICE_X12Y76	FDCE (Hold_fdce_C_D)	0.120	-0.471	div1_quotient_registro[1]
required time				
		0.471		
arrival time				
		-0.125		
slack				
		0.346		

From Clock: clk2\_my\_pll To Clock: clk2\_my\_pll

## Max Delay Paths

Slack (MET) : 1.808ns (required time - arrival time)  
 Source: div2\_divisor\_reg[2]/C  
     (rising edge-triggered cell FDCE clocked by clk2\_my\_pll {rise@10.000ns fall@25.000ns period=30.000ns})  
 Destination: div2\_quotient\_registro[8]/D  
     (rising edge-triggered cell FDCE clocked by clk2\_my\_pll {rise@10.000ns fall@25.000ns period=30.000ns})  
 Path Group: clk2\_my\_pll  
**Path Type:** Setup (Max at Slow Process Corner)  
 Requirement: 30.000ns (clk2\_my\_pll rise@40.000ns - clk2\_my\_pll rise@10.000ns)  
 Data Path Delay: 28.184ns (logic 11.549ns (40.977%) route 16.635ns (59.023%))  
 Logic Levels: 33 (CARRY4=17 LUT1=1 LUT4=5 LUT5=2 LUT6=8)  
 Clock Path Skew: 0.054ns (DCD - SCD + CPR)  
 Destination Clock Delay (DCD): -2.545ns = ( 37.455 - 40.000 )  
 Source Clock Delay (SCD): -2.964ns = ( 7.036 - 10.000 )  
 Clock Pessimism Removal (CPR): -0.365ns  
 Clock Uncertainty: 0.094ns ((TSJ^2 + DJ^2)^1/2) / 2 + PE  
 Total System Jitter (TSJ): 0.071ns  
 Discrete Jitter (DJ): 0.173ns  
 Phase Error (PE): 0.000ns

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock clk2_my_pll rise edge)				
N15		10.000	10.000 r	
		0.000	10.000 r clk (IN)	
N15	net (fo=0)	0.000	10.000 tp1_pll/inst/clk_in1	
	IBUF (Prop_ibuf_I_O)	0.948	10.948 r tp1_pll/inst/clkin1_ibufg/O	
	net (fo=1, routed)	1.253	12.201 tp1_pll/inst/clk_in1_my_pll	
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT1)	-8.590	3.611 r	tp1_pll/inst/plle2_adv_inst/CLKOUT1
	net (fo=1, routed)	1.704	5.315 tp1_pll/inst/clk2_my_pll	
BUFGCTRL_X0Y2	BUFG (Prop_bufg_I_O)	0.096	5.411 r tp1_pll/inst/clkout2_buf/O	
	net (fo=50, routed)	1.624	7.036 clk2	
SLICE_X9Y74	FDCE		r div2_divisor_reg[2]/C	
SLICE_X9Y74	FDCE (Prop_fdce_C_Q)	0.456	7.492 f	div2_divisor_reg[2]/Q
	net (fo=38, routed)	1.349	8.841 div2/div2_divisor[2]	
SLICE_X3Y94	LUT1 (Prop_lut1_I0_O)	0.124	8.965 r	div2/partial_rem0_carry_i_2_0/0
	net (fo=1, routed)	0.000	8.965 div2/partial_rem0_carry_i_2_0_n_0	
SLICE_X3Y94	CARRY4 (Prop_carry4_S[2]_CO[3])	0.398	9.363 r	div2/partial_rem0_carry/CO[3]
	net (fo=1, routed)	0.000	9.363 div2/partial_rem0_carry_n_0	
SLICE_X3Y95	CARRY4 (Prop_carry4_CI_O[0])	0.222	9.585 r	div2/partial_rem0_carry_0/0[0]
	net (fo=3, routed)	0.787	10.372 div2/partial_rem0[4]	
SLICE_X1Y94	LUT5 (Prop_lut5_I1_O)	0.299	10.671 r	div2/i_carry_0_i_3_46/0
	net (fo=1, routed)	0.000	10.671 div2/i_carry_0_i_3_46_n_0	
SLICE_X1Y94	CARRY4 (Prop_carry4_S[1]_O[2])	0.580	11.251 r	div2/partial_rem0_inferred_1/i_carry_0/0[2]
	net (fo=3, routed)	0.583	11.834 div2/partial_rem0_inferred_1/i_carry_0_n_5	
SLICE_X2Y92	LUT6 (Prop_lut6_I0_O)	0.302	12.136 r	div2/i_carry_0_i_1_21/0
	net (fo=1, routed)	0.479	12.615 div2/i_carry_0_i_1_21_n_0	
SLICE_X4Y92	CARRY4 (Prop_carry4_DI[3]_CO[3])	0.385	13.000 r	div2/partial_rem0_inferred_4/i_carry_0/CO[3]
	net (fo=1, routed)	0.000	13.000 div2/partial_rem0_inferred_4/i_carry_0_n_0	
SLICE_X4Y93	CARRY4 (Prop_carry4_CI_O[0])	0.222	13.222 r	div2/partial_rem0_inferred_4/i_carry_1/0[0]
	net (fo=3, routed)	1.129	14.351 div2/partial_rem0_inferred_4/i_carry_1_n_7	
SLICE_X6Y90	LUT4 (Prop_lut4_I0_O)	0.299	14.650 r	div2/i_carry_1_i_7_19/0
	net (fo=1, routed)	0.000	14.650 div2/i_carry_1_i_7_19_n_0	
SLICE_X6Y90	CARRY4 (Prop_carry4_S[1]_O[3])	0.643	15.293 r	div2/partial_rem0_inferred_6/i_carry_1/0[3]
	net (fo=3, routed)	0.580	15.873 div2/partial_rem0_inferred_6/i_carry_1_n_4	
SLICE_X4Y90	LUT6 (Prop_lut6_I0_O)	0.307	16.180 r	div2/i_carry_i_5_15/0
	net (fo=54, routed)	0.926	17.105 div2/i_carry_i_5_15_n_0	
SLICE_X7Y88	LUT4 (Prop_lut4_I2_O)	0.124	17.229 r	div2/i_carry_i_3_53/0
	net (fo=1, routed)	0.000	17.229 div2/i_carry_i_3_53_n_0	
SLICE_X7Y88	CARRY4 (Prop_carry4_S[1]_CO[3])	0.550	17.779 r	div2/partial_rem0_inferred_9/i_carry/CO[3]
	net (fo=1, routed)	0.000	17.779 div2/partial_rem0_inferred_9/i_carry_n_0	
SLICE_X7Y89	CARRY4 (Prop_carry4_CI_O[1])	0.334	18.113 r	div2/partial_rem0_inferred_9/i_carry_0/0[1]
	net (fo=3, routed)	1.126	19.240 div2/partial_rem0_inferred_9/i_carry_0_n_6	

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SLICE_X8Y86	LUT6 (Prop_lut6_I0_O)	0.303	19.543	r	div2/i_carry_0_i_2_17/O
SLICE_X9Y87	net (fo=1, routed)	0.548	20.091		div2/i_carry_0_i_2_17_n_0
	CARRY4 (Prop_carry4_DI[2]_CO[3])				
		0.398	20.489	r	div2/partial_rem0_inferred_12/i_carry_0/CO[3]
	net (fo=1, routed)	0.000	20.489		div2/partial_rem0_inferred_12/i_carry_0_n_0
SLICE_X9Y88	CARRY4 (Prop_carry4_CI_O[0])				
		0.222	20.711	r	div2/partial_rem0_inferred_12/i_carry_1/O[0]
	net (fo=3, routed)	0.837	21.548		div2/partial_rem0_inferred_12/i_carry_1_n_7
SLICE_X10Y88	LUT4 (Prop_lut4_I0_O)	0.299	21.847	r	div2/i_carry_1_i_7_15/O
SLICE_X10Y88	net (fo=1, routed)	0.000	21.847		div2/i_carry_1_i_7_15_n_0
	CARRY4 (Prop_carry4_S[1]_O[3])				
		0.643	22.490	r	div2/partial_rem0_inferred_14/i_carry_1/O[3]
	net (fo=3, routed)	0.730	23.220		div2/partial_rem0_inferred_14/i_carry_1_n_4
SLICE_X10Y85	LUT6 (Prop_lut6_I0_O)	0.307	23.527	r	div2/i_carry_i_5_11/O
SLICE_X14Y80	net (fo=54, routed)	1.103	24.631		div2/i_carry_i_5_11_n_0
SLICE_X14Y80	LUT4 (Prop_lut4_I1_O)	0.124	24.755	r	div2/i_carry_i_6_13/O
SLICE_X14Y80	net (fo=1, routed)	0.000	24.755		div2/i_carry_i_6_13_n_0
	CARRY4 (Prop_carry4_S[1]_O[2])				
		0.578	25.333	r	div2/partial_rem0_inferred_18/i_carry/O[2]
SLICE_X9Y80	net (fo=3, routed)	0.628	25.961		div2/partial_rem0_inferred_18/i_carry_n_5
SLICE_X11Y80	LUT6 (Prop_lut6_I5_O)	0.301	26.262	r	div2/i_carry_i_1_13/O
SLICE_X11Y80	net (fo=1, routed)	0.478	26.740		div2/i_carry_i_1_13_n_0
	CARRY4 (Prop_carry4_DI[3]_CO[3])				
		0.385	27.125	r	div2/partial_rem0_inferred_20/i_carry/CO[3]
SLICE_X11Y81	net (fo=1, routed)	0.000	27.125		div2/partial_rem0_inferred_20/i_carry_n_0
	CARRY4 (Prop_carry4_CI_O[0])				
		0.222	27.347	r	div2/partial_rem0_inferred_20/i_carry_0/O[0]
SLICE_X10Y77	net (fo=3, routed)	0.942	28.288		div2/partial_rem0_inferred_20/i_carry_0_n_7
SLICE_X10Y77	LUT4 (Prop_lut4_I0_O)	0.299	28.587	r	div2/i_carry_0_i_7_11/O
SLICE_X10Y77	net (fo=1, routed)	0.000	28.587		div2/i_carry_0_i_7_11_n_0
	CARRY4 (Prop_carry4_S[1]_O[3])				
		0.643	29.230	r	div2/partial_rem0_inferred_22/i_carry_0/O[3]
SLICE_X11Y75	net (fo=4, routed)	0.719	29.949		div2/partial_rem0_inferred_22/i_carry_0_n_4
SLICE_X11Y75	LUT6 (Prop_lut6_I0_O)	0.307	30.256	r	div2/div2_quotient_registre[11]_i_14/O
SLICE_X8Y75	net (fo=1, routed)	0.551	30.807		div2/div2_quotient_registre[11]_i_14_n_0
	CARRY4 (Prop_carry4_DI[3]_CO[3])				
		0.396	31.203	r	div2/div2_quotient_registre[11]_i_8/CO[3]
SLICE_X8Y76	net (fo=1, routed)	0.000	31.203		div2/div2_quotient_registre[11]_i_8_n_0
	CARRY4 (Prop_carry4_CI_O[1])				
		0.323	31.526	r	div2/div2_remainder_registre[11]_i_5/O[1]
SLICE_X10Y75	net (fo=2, routed)	0.772	32.298		div2/sum00_in[9]
SLICE_X9Y73	LUT5 (Prop_lut5_I0_O)	0.306	32.604	r	div2/div2_quotient_registre[11]_i_10/O
SLICE_X9Y73	net (fo=1, routed)	0.607	33.211		div2/div2_quotient_registre[11]_i_10_n_0
SLICE_X11Y87	LUT6 (Prop_lut6_I5_O)	0.124	33.335	r	div2/div2_quotient_registre[11]_i_3/O
SLICE_X11Y87	net (fo=24, routed)	1.760	35.096		div2/div2_quotient_registre[11]_i_3_n_0
SLICE_X11Y87	LUT6 (Prop_lut6_I2_O)	0.124	35.220	r	div2/div2_quotient_registre[8]_i_1/O
SLICE_X11Y87	net (fo=1, routed)	0.000	35.220		div2/quotient[8]
	FDCE			r	div2/quotient_registre[8]/D

	(clock clk2_my_pll rise edge)				
N15		40.000	40.000	r	
	net (fo=0)	0.000	40.000	r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.814	40.814	r	tp1_pll/inst/clk_in1
	net (fo=1, routed)	1.181	41.995		tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT1)				tp1_pll/inst/plle2_adv_inst/CLKOUT1
		-7.855	34.141	r	tp1_pll/inst/plle2_adv_inst/CLKOUT1
	net (fo=1, routed)	1.625	35.766		tp1_pll/inst/clk2_my_pll
BUFGCTRL_X0Y2	BUFG (Prop_bufg_I_O)	0.091	35.857	r	tp1_pll/inst/clkout2_buf/O
	net (fo=50, routed)	1.598	37.455		clk2
SLICE_X1Y87	FDCE			r	div2_quotient_registre[8]/C
	clock pessimism	-0.365	37.090		
	clock uncertainty	-0.094	36.996		
SLICE_X1Y87	FDCE (Setup_fdce_C_D)	0.031	37.027		div2_quotient_registre[8]
	required time		37.027		
	arrival time		-35.220		
	slack		1.808		

From Clock: clk2\_my\_pll To Clock: clk2\_my\_pll

## Min Delay Paths

Slack (MET) : 0.505ns (arrival time - required time)  
 Source: div2\_divisor\_reg[11]\_rep\_0/C  
           (rising edge-triggered cell FDCE clocked by clk2\_my\_pll {rise@10.000ns fall@25.000ns period=30.000ns})  
 Destination: div2\_quotient\_registro[8]/D  
           (rising edge-triggered cell FDCE clocked by clk2\_my\_pll {rise@10.000ns fall@25.000ns period=30.000ns})  
 Path Group: clk2\_my\_pll  
**Path Type:** Hold (Min at Fast Process Corner)  
 Requirement: 0.000ns (clk2\_my\_pll rise@10.000ns - clk2\_my\_pll rise@10.000ns)  
 Data Path Delay: 0.611ns (logic 0.186ns (30.424%) route 0.425ns (69.576%))  
 Logic Levels: 1 (LUT6=1)  
 Clock Path Skew: 0.014ns (DCD - SCD - CPR)  
 Destination Clock Delay (DCD): -0.356ns = ( 9.644 - 10.000 )  
 Source Clock Delay (SCD): -0.586ns = ( 9.414 - 10.000 )  
 Clock Pessimism Removal (CPR): 0.217ns

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock clk2_my_pll rise edge)				
N15		10.000	10.000 r	
	net (fo=0)	0.000	10.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.177	10.177 r	tp1_pll/inst/clk_in1
	net (fo=1, routed)	0.440	10.617	tp1_pll/inst/clk_in1_my_pll
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT1)	-2.339	8.278 r	tp1_pll/inst/plle2_adv_inst/CLKOUT1
	net (fo=1, routed)	0.510	8.788	tp1_pll/inst/clk2_my_pll
BUFGCTRL_X0Y2	BUFG (Prop_bufg_I_O)	0.026	8.814 r	tp1_pll/inst/clkout2_buf/0
	net (fo=50, routed)	0.600	9.414	clk2
SLICE_X3Y89	FDCE		r	div2_divisor_reg[11]_rep_0/C
(clock clk2_my_pll rise edge)				
N15		10.000	10.000 r	
	net (fo=0)	0.000	10.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.365	10.365 r	tp1_pll/inst/clk_in1
	net (fo=1, routed)	0.481	10.846	tp1_pll/inst/clk_in1_my_pll
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT1)	-2.657	8.189 r	tp1_pll/inst/plle2_adv_inst/CLKOUT1
	net (fo=1, routed)	0.556	8.745	tp1_pll/inst/clk2_my_pll
BUFGCTRL_X0Y2	BUFG (Prop_bufg_I_O)	0.029	8.774 r	tp1_pll/inst/clkout2_buf/0
	net (fo=50, routed)	0.871	9.644	clk2
SLICE_X1Y87	FDCE		r	div2_quotient_registro[8]/C
	clock pessimism	-0.217	9.428	
SLICE_X1Y87	FDCE (Hold_fdce_C_D)	0.092	9.520	div2_quotient_registro[8]
		required time	-9.520	
		arrival time	10.025	
		slack	0.505	

From Clock: clk3\_my\_pll To Clock: clk3\_my\_pll

## Max Delay Paths

```

Slack (MET) : 2.104ns (required time - arrival time)
Source:      div3_divisor_reg[1]/C
              (rising edge-triggered cell FDCE clocked by clk3_my_pll {rise@20.000ns
fall@35.000ns period=30.000ns})
Destination: div3_quotient_register_reg[2]/D
              (rising edge-triggered cell FDCE clocked by clk3_my_pll {rise@20.000ns
fall@35.000ns period=30.000ns})
Path Group:  clk3_my_pll
Path Type: Setup (Max at Slow Process Corner)
Requirement: 30.000ns (clk3_my_pll rise@50.000ns - clk3_my_pll rise@20.000ns)
Data Path Delay: 27.758ns (logic 11.776ns (42.423%) route 15.982ns (57.577%))
Logic Levels: 33 (CARRY4=17 LUT1=1 LUT4=5 LUT5=2 LUT6=8)
Clock Path Skew: -0.121ns (DCD - SCD + CPR)
Destination Clock Delay (DCD): -2.633ns = ( 47.367 - 50.000 )
Source Clock Delay (SCD): -2.877ns = ( 17.123 - 20.000 )
Clock Pessimism Removal (CPR): -0.365ns
Clock Uncertainty: 0.094ns ((TSJ^2 + DJ^2)^1/2) / 2 + PE
Total System Jitter (TSJ): 0.071ns
Discrete Jitter (DJ): 0.173ns
Phase Error (PE): 0.000ns

```

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock clk3_my_pll rise edge)				
N15		20.000	20.000 r	
	net (fo=0)	0.000	20.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.948	20.948 r	tp1_pll/inst/clk_in1
	net (fo=1, routed)	1.253	22.201	tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT2)	-8.590	13.611 r	tp1_pll/inst/plle2_adv_inst/CLKOUT2
	net (fo=1, routed)	1.704	15.315	tp1_pll/inst/clk3_my_pll
BUFGCTRL_X0Y3	BUFG (Prop_bufg_I_O)	0.096	15.411 r	tp1_pll/inst/clkout3_buf/O
	net (fo=50, routed)	1.711	17.123	clk3
SLICE_X6Y81	FDCE		r	div3_divisor_reg[1]/C
(clock clk3_my_pll fall edge)				
SLICE_X6Y81	FDCE (Prop_fdce_C_Q)	0.518	17.641 f	div3_divisor_reg[1]/Q
	net (fo=38, routed)	0.806	18.447	div3/div3_divisor[1]
SLICE_X2Y84	LUT1 (Prop_lut1_I0_O)	0.124	18.571 r	div3/i_carry_i_4_1/0
	net (fo=1, routed)	0.000	18.571	div3/i_carry_i_4_1_n_0
SLICE_X2Y84	CARRY4 (Prop_carry4_S[1]_O[2])	0.578	19.149 r	div3/partial_rem0_inferred_0/i_carry/O[2]
	net (fo=3, routed)	0.800	19.949	div3/partial_rem0_inferred_1/i_carry/O[1]
SLICE_X4Y81	LUT5 (Prop_lut5_I4_O)	0.301	20.250 r	div3/i_carry_i_1_57/0
	net (fo=1, routed)	0.000	20.250	div3/i_carry_i_1_57_n_0
SLICE_X4Y81	CARRY4 (Prop_carry4_S[3]_CO[3])	0.401	20.651 r	div3/partial_rem0_inferred_1/i_carry/CO[3]
	net (fo=1, routed)	0.000	20.651	div3/partial_rem0_inferred_1/i_carry_n_0
SLICE_X4Y82	CARRY4 (Prop_carry4_CI_O[0])	0.222	20.873 r	div3/partial_rem0_inferred_1/i_carry_0/O[0]
	net (fo=3, routed)	0.936	21.809	div3/partial_rem0_inferred_1/i_carry_0_n_7
SLICE_X9Y85	LUT6 (Prop_lut6_I0_O)	0.299	22.108 r	div3/i_carry_0_i_3_33/0
	net (fo=1, routed)	0.552	22.660	div3/i_carry_0_i_3_33_n_0
SLICE_X6Y85	CARRY4 (Prop_carry4_DI[1]_CO[3])	0.520	23.180 r	div3/partial_rem0_inferred_4/i_carry_0/CO[3]
	net (fo=1, routed)	0.000	23.180	div3/partial_rem0_inferred_4/i_carry_0_n_0
SLICE_X6Y86	CARRY4 (Prop_carry4_CI_O[0])	0.219	23.399 r	div3/partial_rem0_inferred_4/i_carry_1/O[0]
	net (fo=3, routed)	0.812	24.211	div3/partial_rem0_inferred_4/i_carry_1_n_7
SLICE_X8Y84	LUT4 (Prop_lut4_I0_O)	0.295	24.506 r	div3/i_carry_1_i_7_30/0
	net (fo=1, routed)	0.000	24.506	div3/i_carry_1_i_7_30_n_0
SLICE_X8Y84	CARRY4 (Prop_carry4_S[1]_O[3])	0.643	25.149 r	div3/partial_rem0_inferred_6/i_carry_1/O[3]
	net (fo=3, routed)	0.954	26.103	div3/partial_rem0_inferred_6/i_carry_1_n_4
SLICE_X5Y81	LUT6 (Prop_lut6_I0_O)	0.307	26.410 r	div3/i_carry_i_5_25/0
	net (fo=54, routed)	0.825	27.235	div3/i_carry_i_5_25_n_0
SLICE_X5Y77	LUT4 (Prop_lut4_I2_O)	0.124	27.359 r	div3/i_carry_i_3_64/0
	net (fo=1, routed)	0.000	27.359	div3/i_carry_i_3_64_n_0
SLICE_X5Y77	CARRY4 (Prop_carry4_S[1]_O[2])	0.580	27.939 r	div3/partial_rem0_inferred_9/i_carry/O[2]
	net (fo=3, routed)	1.027	28.966	div3/partial_rem0_inferred_9/i_carry_n_5
SLICE_X0Y78	LUT6 (Prop_lut6_I0_O)	0.302	29.268 r	div3/i_carry_i_1_29/0
	net (fo=1, routed)	0.331	29.599	div3/i_carry_i_1_29_n_0
SLICE_X1Y77	CARRY4 (Prop_carry4_DI[3]_CO[3])	0.385	29.984 r	div3/partial_rem0_inferred_12/i_carry/CO[3]
	net (fo=1, routed)	0.000	29.984	div3/partial_rem0_inferred_12/i_carry_n_0
SLICE_X1Y78	CARRY4 (Prop_carry4_CI_O[0])			

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SLICE_X7Y78	net (fo=3, routed)	0.222	30.206 r	div3/partial_rem0_inferred_12/i_carry_0/O[0]	
	LUT4 (Prop_lut4_I0_O)	0.953	31.159	div3/partial_rem0_inferred_12/i_carry_0_n_7	
	net (fo=1, routed)	0.299	31.458 r	div3/i_carry_0_i_7_26/O	
SLICE_X7Y78	CARRY4 (Prop_carry4_S[1]_O[2])	0.000	31.458	div3/i_carry_0_i_7_26_n_0	
		0.580	32.038 r	div3/partial_rem0_inferred_14/i_carry_0/O[2]	
SLICE_X2Y77	net (fo=3, routed)	0.585	32.623	div3/partial_rem0_inferred_14/i_carry_0_n_5	
	LUT6 (Prop_lut6_I5_O)	0.302	32.925 r	div3/i_carry_0_i_1_27/O	
	net (fo=1, routed)	0.807	33.732	div3/i_carry_0_i_1_27_n_0	
SLICE_X7Y74	CARRY4 (Prop_carry4_DI[3]_CO[3])	0.385	34.117 r	div3/partial_rem0_inferred_16/i_carry_0/CO[3]	
	net (fo=1, routed)	0.009	34.126	div3/partial_rem0_inferred_16/i_carry_0_n_0	
SLICE_X7Y75	CARRY4 (Prop_carry4_CI_O[0])	0.222	34.348 r	div3/partial_rem0_inferred_16/i_carry_1/O[0]	
	net (fo=3, routed)	0.585	34.933	div3/partial_rem0_inferred_16/i_carry_1_n_7	
SLICE_X4Y75	LUT4 (Prop_lut4_I0_O)	0.299	35.232 r	div3/i_carry_1_i_7_24/O	
	net (fo=1, routed)	0.000	35.232	div3/i_carry_1_i_7_24_n_0	
SLICE_X4Y75	CARRY4 (Prop_carry4_S[1]_O[3])	0.640	35.872 r	div3/partial_rem0_inferred_18/i_carry_1/O[3]	
	net (fo=3, routed)	0.763	36.635	div3/partial_rem0_inferred_18/i_carry_1_n_4	
SLICE_X2Y77	LUT6 (Prop_lut6_I0_O)	0.306	36.941 r	div3/i_carry_i_5_19/O	
	net (fo=57, routed)	1.328	38.268	div3/i_carry_i_5_19_n_0	
SLICE_X0Y73	LUT4 (Prop_lut4_I1_O)	0.124	38.392 r	div3/i_carry_i_6_22/O	
	net (fo=1, routed)	0.000	38.392	div3/i_carry_i_6_22_n_0	
SLICE_X0Y73	CARRY4 (Prop_carry4_S[1]_CO[3])	0.550	38.942 r	div3/partial_rem0_inferred_22/i_carry/CO[3]	
	net (fo=1, routed)	0.000	38.942	div3/partial_rem0_inferred_22/i_carry_n_0	
SLICE_X0Y74	CARRY4 (Prop_carry4_CI_O[1])	0.334	39.276 r	div3/partial_rem0_inferred_22/i_carry_0/O[1]	
	net (fo=4, routed)	0.675	39.951	div3/partial_rem0_inferred_22/i_carry_0_n_6	
SLICE_X3Y69	LUT6 (Prop_lut6_I5_O)	0.303	40.254 r	div3/sum0_carry_0_i_2_1/O	
	net (fo=5, routed)	0.659	40.913	div3/sum0_carry_0_i_2_1_n_0	
SLICE_X1Y70	CARRY4 (Prop_carry4_DI[1]_CO[3])	0.507	41.420 r	div3/sum0_carry_0/CO[3]	
	net (fo=1, routed)	0.000	41.420	div3/sum0_carry_0_n_0	
SLICE_X1Y71	CARRY4 (Prop_carry4_CI_O[1])	0.334	41.754 r	div3/sum0_carry_1/O[1]	
	net (fo=2, routed)	0.566	42.320	div3/sum0[9]	
SLICE_X3Y71	LUT5 (Prop_lut5_I1_O)	0.303	42.623 r	div3/div3_quotient_registre[11]_i_10/O	
	net (fo=1, routed)	0.480	43.103	div3/div3_quotient_registre[11]_i_10_n_0	
SLICE_X3Y70	LUT6 (Prop_lut6_I5_O)	0.124	43.227 r	div3/div3_quotient_registre[11]_i_3/O	
	net (fo=24, routed)	1.530	44.757	div3/div3_quotient_registre[11]_i_3_n_0	
SLICE_X8Y80	LUT6 (Prop_lut6_I2_O)	0.124	44.881 r	div3/div3_quotient_registre[2]_i_1/O	
	net (fo=1, routed)	0.000	44.881	div3_quotient[2]	
SLICE_X8Y80	FDCE		r	div3_quotient_registre_reg[2]/D	

	(clock clk3_my_pll rise edge)				
N15		50.000	50.000 r		
		0.000	50.000 r	clk (IN)	
N15	IBUF (Prop_ibuf_I_O)	0.814	50.814 r	tp1_pll/inst/clk_in1	
	net (fo=1, routed)	1.181	51.995	tp1_pll/inst/clkin1_ibufg/O	
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT2)	-7.855	44.141 r	tp1_pll/inst/plle2_adv_inst/CLKOUT2	
	net (fo=1, routed)	1.625	45.766	tp1_pll/inst/clk3_my_pll	
BUFGCTRL_X0Y3	BUFG (Prop_bufg_I_O)	0.091	45.857 r	tp1_pll/inst/clkout3_buf/O	
	net (fo=50, routed)	1.510	47.367	clk3	
SLICE_X8Y80	FDCE		r	div3_quotient_registre_reg[2]/C	
	clock pessimism	-0.365	47.002		
	clock uncertainty	-0.094	46.908		
SLICE_X8Y80	FDCE (Setup_fdce_C_D)	0.077	46.985	div3_quotient_registre_reg[2]	
	required time		46.985		
	arrival time		-44.881		
	slack		2.104		

From Clock: clk3\_my\_pll To Clock: clk3\_my\_pll

## Min Delay Paths

Slack (MET) : 0.442ns (arrival time - required time)  
 Source: div3\_divisor\_reg[11]\_rep/C  
                  (rising edge-triggered cell FDCE clocked by clk3\_my\_pll {rise@20.000ns fall@35.000ns period=30.000ns})  
 Destination: div3\_quotient\_registro[11]/D  
                  (rising edge-triggered cell FDCE clocked by clk3\_my\_pll {rise@20.000ns fall@35.000ns period=30.000ns})  
 Path Group: clk3\_my\_pll  
**Path Type:** Hold (Min at Fast Process Corner)  
 Requirement: 0.000ns (clk3\_my\_pll rise@20.000ns - clk3\_my\_pll rise@20.000ns)  
 Data Path Delay: 0.548ns (logic 0.186ns (33.962%) route 0.362ns (66.038%))  
 Logic Levels: 1 (LUT6=1)  
 Clock Path Skew: 0.014ns (DCD - SCD - CPR)  
 Destination Clock Delay (DCD): -0.358ns = ( 19.642 - 20.000 )  
 Source Clock Delay (SCD): -0.588ns = ( 19.412 - 20.000 )  
 Clock Pessimism Removal (CPR): 0.217ns

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock clk3_my_pll rise edge)				
N15		20.000	20.000 r	
	net (fo=0)	0.000	20.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.177	20.177 r	tp1_pll/inst/clk_in1
	net (fo=1, routed)	0.440	20.617	tp1_pll/inst/clk_in1_my_pll
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT2)	-2.339	18.278 r	tp1_pll/inst/plle2_adv_inst/CLKOUT2
	net (fo=1, routed)	0.510	18.788	tp1_pll/inst/clk3_my_pll
BUFGCTRL_X0Y3	BUFG (Prop_bufg_I_O)	0.026	18.814 r	tp1_pll/inst/clkout3_buf/0
	net (fo=50, routed)	0.598	19.412	clk3
SLICE_X3Y85	FDCE		r	div3_divisor_reg[11]_rep/C
(clock clk3_my_pll rise edge)				
N15		20.000	20.000 r	
	net (fo=0)	0.000	20.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.365	20.365 r	tp1_pll/inst/clk_in1
	net (fo=1, routed)	0.481	20.846	tp1_pll/inst/clk_in1_my_pll
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT2)	-2.657	18.189 r	tp1_pll/inst/plle2_adv_inst/CLKOUT2
	net (fo=1, routed)	0.556	18.745	tp1_pll/inst/clk3_my_pll
BUFGCTRL_X0Y3	BUFG (Prop_bufg_I_O)	0.029	18.774 r	tp1_pll/inst/clkout3_buf/0
	net (fo=50, routed)	0.869	19.642	clk3
SLICE_X0Y84	FDCE		r	div3_quotient_registro[11]/C
	clock pessimism	-0.217	19.426	
SLICE_X0Y84	FDCE (Hold_fdce_C_D)	0.092	19.518	div3_quotient_registro[11]
required time				
			-19.518	
arrival time				
			19.960	
slack				
			0.442	

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### From Clock: clk4\_my\_pll To Clock: clk4\_my\_pll

Max Delay Paths

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Slack (MET) : 6.393ns (required time - arrival time)
Source:      compteureg[0]/C
              (rising edge-triggered cell FDCE clocked by clk4_my_pll {rise@0.000ns fall@5.000ns
period=10.000ns})
Destination: remainder_reg[10]/D
              (rising edge-triggered cell FDCE clocked by clk4_my_pll {rise@0.000ns fall@5.000ns
period=10.000ns})
Path Group:  clk4_my_pll
Path Type:   Setup (Max at Slow Process Corner)
Requirement: 10.000ns (clk4_my_pll rise@10.000ns - clk4_my_pll rise@0.000ns)
Data Path Delay: 3.507ns (logic 0.580ns (16.538%) route 2.927ns (83.462%))
Logic Levels: 1 (LUT6=1)
Clock Path Skew: -0.052ns (DCD - SCD + CPR)
Destination Clock Delay (DCD): -2.555ns = ( 7.445 - 10.000 )
Source Clock Delay (SCD): -2.868ns
Clock Pessimism Removal (CPR): -0.365ns
Clock Uncertainty: 0.077ns ((TSJ^2 + DJ^2)^1/2) / 2 + PE
Total System Jitter (TSJ): 0.071ns
Discrete Jitter (DJ): 0.138ns
Phase Error (PE): 0.000ns
```

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock clk4_my_pll rise edge)				
N15		0.000	0.000 r	
	net (fo=0)	0.000	0.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.948	0.948 r	tp1_pll/inst/clk_in1
	net (fo=1, routed)	1.253	2.201	tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT3)	-8.590	-6.389 r	tp1_pll/inst/plle2_adv_inst/CLKOUT3
	net (fo=1, routed)	1.704	-4.685	tp1_pll/inst/clk4_my_pll
BUFGCTRL_X0Y0	BUFGE (Prop_bufg_I_O)	0.096	-4.589 r	tp1_pll/inst/clkout4_buf/O
	net (fo=51, routed)	1.720	-2.868	clk4
SLICE_X1Y88	FDCE		r	compteur_reg[0]/C
(clock clk4_my_pll rise edge)				
SLICE_X1Y88	FDCE (Prop_fdce_C_Q)	0.456	-2.412 r	compteur_reg[0]/Q
	net (fo=25, routed)	2.927	0.515	compteur[0]
SLICE_X7Y71	LUT6 (Prop_lut6_I1_O)	0.124	0.639 r	remainder[10]_i_1/O
	net (fo=1, routed)	0.000	0.639	remainder[10]_i_1_n_0
SLICE_X7Y71	FDCE		r	remainder_reg[10]/D

	(clock clk4_my_pll rise edge)	10.000	10.000 r	
N15		0.000	10.000 r	clk (IN)
	net (fo=0)	0.000	10.000 r	tp1_pll/inst/clk_in1
N15	IBUF (Prop_ibuf_I_O)	0.814	10.814 r	tp1_pll/inst/clkin1_ibufg/O
	net (fo=1, routed)	1.181	11.995	tp1_pll/inst/clk_in1_my_pll
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT3)	-7.855	4.141 r	tp1_pll/inst/plle2_adv_inst/CLKOUT3
	net (fo=1, routed)	1.625	5.766	tp1_pll/inst/clk4_my_pll
BUFGCTRL_X0Y0	BUFGE (Prop_bufg_I_O)	0.091	5.857 r	tp1_pll/inst/clkout4_buf/O
	net (fo=51, routed)	1.588	7.445	clk4
SLICE_X7Y71	FDCE		r	remainder_reg[10]/C
	clock pessimism	-0.365	7.080	
	clock uncertainty	-0.077	7.002	
SLICE_X7Y71	FDCE (Setup_fdce_C_D)	0.029	7.031	remainder_reg[10]
required time				
			7.031	
arrival time				
			-0.639	
slack				
			6.393	

```
Slack (MET) : 6.454ns (required time - arrival time)
Source:      compteureg[0]/C
```

## Abel DIDOUH

```

(rising edge-triggered cell FDCE clocked by clk4_my_pll {rise@0.000ns fall@5.000ns
period=10.000ns})
Destination: remainder_reg[7]/D
(rising edge-triggered cell FDCE clocked by clk4_my_pll {rise@0.000ns fall@5.000ns
period=10.000ns})
Path Group: clk4_my_pll
Path Type: Setup (Max at Slow Process Corner)
Requirement: 10.000ns (clk4_my_pll rise@10.000ns - clk4_my_pll rise@0.000ns)
Data Path Delay: 3.417ns (logic 0.580ns (16.97%) route 2.837ns (83.028%))
Logic Levels: 1 (LUT6=1)
Clock Path Skew: -0.130ns (DCD - SCD + CPR)
Destination Clock Delay (DCD): -2.633ns = ( 7.367 - 10.000 )
Source Clock Delay (SCD): -2.868ns
Clock Pessimism Removal (CPR): -0.365ns
Clock Uncertainty: 0.077ns ((TSJ^2 + DJ^2)^1/2) / 2 + PE
Total System Jitter (TSJ): 0.071ns
Discrete Jitter (DJ): 0.138ns
Phase Error (PE): 0.000ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)
-----  

(clock clk4_my_pll rise edge)
0.000 0.000 r
N15 0.000 0.000 r clk (IN)
net (fo=0) 0.000 0.000 tp1_pll/inst/clk_in1
N15 IBUF (Prop_ibuf_I_O) 0.948 0.948 r tp1_pll/inst/clkin1_ibufg/O
net (fo=1, routed) 1.253 2.201 tp1_pll/inst/clk_in1_my_pll
PLLE2_ADV_X0Y1 PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT3)
-8.590 -6.389 r tp1_pll/inst/plle2_adv_inst/CLKOUT3
net (fo=1, routed) 1.704 -4.685 tp1_pll/inst/clk4_my_pll
BUFGCTRL_X0Y0 BUFG (Prop_bufg_I_O) 0.096 -4.589 r tp1_pll/inst/clkout4_buf/O
net (fo=51, routed) 1.720 -2.868 clk4
SLICE_X1Y88 FDCE r compteur_reg[0]/C
-----  

SLICE_X1Y88 FDCE (Prop_fdce_C_Q) 0.456 -2.412 r compteur_reg[0]/Q
net (fo=25, routed) 2.837 0.425 compteur[0]
SLICE_X8Y70 LUT6 (Prop_lut6_I1_O) 0.124 0.549 r remainder[7]_i_1/O
net (fo=1, routed) 0.000 0.549 remainder[7]_i_1_n_0
SLICE_X8Y70 FDCE r remainder_reg[7]/D
-----  

(clock clk4_my_pll rise edge)
10.000 10.000 r
N15 0.000 10.000 r clk (IN)
net (fo=0) 0.000 10.000 tp1_pll/inst/clk_in1
N15 IBUF (Prop_ibuf_I_O) 0.814 10.814 r tp1_pll/inst/clkin1_ibufg/O
net (fo=1, routed) 1.181 11.995 tp1_pll/inst/clk_in1_my_pll
PLLE2_ADV_X0Y1 PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT3)
-7.855 4.141 r tp1_pll/inst/plle2_adv_inst/CLKOUT3
net (fo=1, routed) 1.625 5.766 tp1_pll/inst/clk4_my_pll
BUFGCTRL_X0Y0 BUFG (Prop_bufg_I_O) 0.091 5.857 r tp1_pll/inst/clkout4_buf/O
net (fo=51, routed) 1.510 7.367 clk4
SLICE_X8Y70 FDCE r remainder_reg[7]/C
clock pessimism -0.365 7.002
clock uncertainty -0.077 6.924
SLICE_X8Y70 FDCE (Setup_fdce_C_D) 0.079 7.003 remainder_reg[7]
-----  

required time 7.003
arrival time -0.549
-----  

slack 6.454

```

From Clock: clk4\_my\_pll To Clock: clk4\_my\_pll

## Min Delay Paths

```

Slack (MET) : 0.250ns (arrival time - required time)
  Source: compteur_reg[0]/C
    (rising edge-triggered cell FDCE clocked by clk4_my_pll {rise@0.000ns fall@5.000ns
period=10.000ns})
  Destination: compteur_reg[1]/D
    (rising edge-triggered cell FDPE clocked by clk4_my_pll {rise@0.000ns fall@5.000ns
period=10.000ns})
Path Group: clk4_my_pll
Path Type: Hold (Min at Fast Process Corner)
Requirement: 0.000ns (clk4_my_pll rise@0.000ns - clk4_my_pll rise@0.000ns)
Data Path Delay: 0.311ns (logic 0.141ns (45.303%) route 0.170ns (54.697%))
Logic Levels: 0
Clock Path Skew: 0.000ns (DCD - SCD - CPR)
  Destination Clock Delay (DCD): -0.354ns
  Source Clock Delay (SCD): -0.586ns
  Clock Pessimism Removal (CPR): 0.233ns

```

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock clk4_my_pll rise edge)				
N15		0.000	0.000 r	
	net (fo=0)	0.000	0.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.177	0.177 r	tp1_pll/inst/clk_in1
	net (fo=1, routed)	0.440	0.617	tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT3)	-2.339	-1.722 r	tp1_pll/inst/plle2_adv_inst/CLKOUT3
	net (fo=1, routed)	0.510	-1.212	tp1_pll/inst/clk4_my_pll
BUFGCTRL_X0Y0	BUFG (Prop_bufg_I_O)	0.026	-1.186 r	tp1_pll/inst/clkout4_buf/O
	net (fo=51, routed)	0.600	-0.586	clk4
SLICE_X1Y88	FDCE		r	compteur_reg[0]/C
(clock clk4_my_pll rise edge)				
SLICE_X1Y88	FDCE (Prop_fdce_C_Q)	0.141	-0.445 r	compteur_reg[0]/Q
	net (fo=25, routed)	0.170	-0.275	compteur[0]
SLICE_X1Y88	FDPE		r	compteur_reg[1]/D

	(clock clk4_my_pll rise edge)			
N15		0.000	0.000 r	
	net (fo=0)	0.000	0.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.365	0.365 r	tp1_pll/inst/clk_in1
	net (fo=1, routed)	0.481	0.846	tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT3)	-2.657	-1.811 r	tp1_pll/inst/plle2_adv_inst/CLKOUT3
	net (fo=1, routed)	0.556	-1.255	tp1_pll/inst/clk4_my_pll
BUFGCTRL_X0Y0	BUFG (Prop_bufg_I_O)	0.029	-1.226 r	tp1_pll/inst/clkout4_buf/O
	net (fo=51, routed)	0.873	-0.354	clk4
SLICE_X1Y88	FDPE		r	compteur_reg[1]/C
	clock pessimism	-0.233	-0.586	
SLICE_X1Y88	FDPE (Hold_fdpe_C_D)	0.061	-0.525	compteur_reg[1]
required time				
		0.525		
arrival time				
		-0.275		
slack				
		0.250		

From Clock: clk4\_my\_pll To Clock: clk1\_my\_pll

## Max Delay Paths

Slack (MET) : 4.173ns (required time - arrival time)  
 Source: divisor\_q\_reg[11]/C  
     (rising edge-triggered cell FDCE clocked by clk4\_my\_pll {rise@0.000ns fall@5.000ns period=10.000ns})  
 Destination: div1\_divisor\_reg[11]\_rep\_0/D  
     (rising edge-triggered cell FDCE clocked by clk1\_my\_pll {rise@0.000ns fall@15.000ns period=30.000ns})  
 Path Group: clk1\_my\_pll  
**Path Type:** Setup (Max at Slow Process Corner)  
 Requirement: 10.000ns (clk1\_my\_pll rise@30.000ns - clk4\_my\_pll rise@20.000ns)  
 Data Path Delay: 5.284ns (logic 0.456ns (8.629%) route 4.828ns (91.371%))  
 Logic Levels: 0  
 Clock Path Skew: -0.268ns (DCD - SCD + CPR)  
 Destination Clock Delay (DCD): -2.624ns = ( 27.376 - 30.000 )  
 Source Clock Delay (SCD): -2.885ns = ( 17.115 - 20.000 )  
 Clock Pessimism Removal (CPR): -0.530ns  
 Clock Uncertainty: 0.214ns ((TSJ^2 + DJ^2)^1/2) / 2 + PE  
 Total System Jitter (TSJ): 0.071ns  
 Discrete Jitter (DJ): 0.173ns  
 Phase Error (PE): 0.120ns

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock clk4_my_pll rise edge)				
N15		20.000	20.000 r	
		0.000	20.000 r	clk (IN)
N15	net (fo=0)	0.000	20.000	tp1_pll/inst/clk_in1
	IBUF (Prop_ibuf_I_O)	0.948	20.948 r	tp1_pll/inst/clkinl_ibufg/O
	net (fo=1, routed)	1.253	22.201	tp1_pll/inst/clk_in1_my_pll
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT3)	-8.590	13.611 r	tp1_pll/inst/plle2_adv_inst/CLKOUT3
	net (fo=1, routed)	1.704	15.315	tp1_pll/inst/clk4_my_pll
BUFGCTRL_X0Y0	BUFGE (Prop_bufg_I_O)	0.096	15.411 r	tp1_pll/inst/clkout4_buf/O
	net (fo=51, routed)	1.703	17.115	clk4
SLICE_X0Y75	FDCE		r	divisor_q_reg[11]/C
(clock clk1_my_pll rise edge)				
N15		30.000	30.000 r	
		0.000	30.000 r	clk (IN)
N15	net (fo=0)	0.000	30.000	tp1_pll/inst/clk_in1
	IBUF (Prop_ibuf_I_O)	0.814	30.814 r	tp1_pll/inst/clkinl_ibufg/O
	net (fo=1, routed)	1.181	31.995	tp1_pll/inst/clk_in1_my_pll
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT0)	-7.855	24.141 r	tp1_pll/inst/plle2_adv_inst/CLKOUT0
	net (fo=1, routed)	1.625	25.766	tp1_pll/inst/clk1_my_pll
BUFGCTRL_X0Y1	BUFGE (Prop_bufg_I_O)	0.091	25.857 r	tp1_pll/inst/clkout1_buf/O
	net (fo=50, routed)	1.519	27.376	clk1
SLICE_X8Y89	FDCE		r	div1_divisor_reg[11]_rep_0/C
	clock pessimism	-0.530	26.846	
	clock uncertainty	-0.214	26.633	
SLICE_X8Y89	FDCE (Setup_fdce_C_D)	-0.061	26.572	div1_divisor_reg[11]_rep_0
		required time	26.572	
		arrival time	-22.399	
		slack	4.173	

From Clock: clk4\_my\_pll To Clock: clk1\_my\_pll

Min Delay Paths

```

Slack (MET) :          0.233ns (arrival time - required time)
Source:               divisor_q_reg[2]/C
                      (rising edge-triggered cell FDCE clocked by clk4_my_pll {rise@0.000ns fall@5.000ns
period=10.000ns})
Destination:          div1_divisor_reg[2]/D
                      (rising edge-triggered cell FDCE clocked by clk1_my_pll {rise@0.000ns
fall@15.000ns period=30.000ns)
Path Group:           clk1_my_pll
Path Type:          Hold (Min at Fast Process Corner)
Requirement:          0.000ns (clk1_my_pll rise@0.000ns - clk4_my_pll rise@0.000ns)
Data Path Delay:      0.818ns (logic 0.141ns (17.241%) route 0.677ns (82.759%))
Logic Levels:         0
Clock Path Skew:     0.285ns (DCD - SCD - CPR)
Destination Clock Delay (DCD): -0.399ns
Source Clock Delay (SCD): -0.594ns
Clock Pessimism Removal (CPR): -0.089ns
Clock Uncertainty:    0.214ns ((TSJ^2 + DJ^2)^1/2) / 2 + PE
Total System Jitter (TSJ): 0.071ns
Discrete Jitter (DJ): 0.173ns
Phase Error (PE): 0.120ns

```

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock clk4_my_pll rise edge)				
N15	net (fo=0)	0.000	0.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.177	0.177 r	tp1_pll/inst/clk_in1
	net (fo=1, routed)	0.440	0.617	tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT3)	-2.339	-1.722 r	tp1_pll/inst/plle2_adv_inst/CLKOUT3
	net (fo=1, routed)	0.510	-1.212	tp1_pll/inst/clk4_my_pll
BUFGCTRL_X0Y0	BUFGE (Prop_bufg_I_O)	0.026	-1.186 r	tp1_pll/inst/clkout4_buf/O
	net (fo=51, routed)	0.592	-0.594	clk4
SLICE_X7Y70	FDCE		r	divisor_q_reg[2]/C
(clock clk1_my_pll rise edge)				
N15	net (fo=0)	0.000	0.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.365	0.365 r	tp1_pll/inst/clk_in1
	net (fo=1, routed)	0.481	0.846	tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT0)	-2.657	-1.811 r	tp1_pll/inst/plle2_adv_inst/CLKOUT0
	net (fo=1, routed)	0.556	-1.255	tp1_pll/inst/clk1_my_pll
BUFGCTRL_X0Y1	BUFGE (Prop_bufg_I_O)	0.029	-1.226 r	tp1_pll/inst/clkout1_buf/O
	net (fo=50, routed)	0.828	-0.399	clk1
SLICE_X8Y74	FDCE		r	div1_divisor_reg[2]/C
	clock pessimism	0.089	-0.309	
	clock uncertainty	0.214	-0.096	
SLICE_X8Y74	FDCE (Hold_fdce_C_D)	0.087	-0.009	div1_divisor_reg[2]
required time				
		0.009		
arrival time				
		0.224		
slack				
		0.233		

From Clock: clk4\_my\_pll To Clock: clk2\_my\_pll

Max Delay Paths

```

Slack (MET) : 4.919ns (required time - arrival time)
Source: divisor_q_reg[11]/C
         (rising edge-triggered cell FDCE clocked by clk4_my_pll {rise@0.000ns fall@5.000ns
period=10.000ns})
Destination: div2_divisor_reg[11]_rep_0/D
         (rising edge-triggered cell FDCE clocked by clk2_my_pll {rise@10.000ns
fall@25.000ns period=30.000ns})
Path Group: clk2_my_pll
Path Type: Setup (Max at Slow Process Corner)
Requirement: 10.000ns (clk2_my_pll rise@10.000ns - clk4_my_pll rise@0.000ns)
Data Path Delay: 4.572ns (logic 0.456ns (9.973%) route 4.116ns (90.027%))
Logic Levels: 0
Clock Path Skew: -0.187ns (DCD - SCD + CPR)
Destination Clock Delay (DCD): -2.543ns = ( 7.457 - 10.000 )
Source Clock Delay (SCD): -2.885ns
Clock Pessimism Removal (CPR): -0.530ns
Clock Uncertainty: 0.214ns ((TSJ^2 + DJ^2)^1/2) / 2 + PE
Total System Jitter (TSJ): 0.071ns
Discrete Jitter (DJ): 0.173ns
Phase Error (PE): 0.120ns

```

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock clk4_my_pll rise edge)				
N15	net (fo=0)	0.000	0.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.948	0.948 r	tp1_pll/inst/clk_in1
	net (fo=1, routed)	1.253	2.201	tp1_pll/inst/clk_in1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT3)	-8.590	-6.389 r	tp1_pll/inst/plle2_adv_inst/CLKOUT3
	net (fo=1, routed)	1.704	-4.685	tp1_pll/inst/clk4_my_pll
BUFGCTRL_X0Y0	BUFG (Prop_bufg_I_O)	0.096	-4.589 r	tp1_pll/inst/clkout4_buf/O
	net (fo=51, routed)	1.703	-2.885	clk4
SLICE_X0Y75	FDCE		r	divisor_q_reg[11]/C
(clock clk2_my_pll rise edge)				
N15	net (fo=0)	10.000	10.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.000	10.000 r	tp1_pll/inst/clk_in1
	net (fo=1, routed)	0.814	10.814 r	tp1_pll/inst/clk_in1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT1)	-7.855	4.141 r	tp1_pll/inst/plle2_adv_inst/CLKOUT1
	net (fo=1, routed)	1.625	5.766	tp1_pll/inst/clk2_my_pll
BUFGCTRL_X0Y2	BUFG (Prop_bufg_I_O)	0.091	5.857 r	tp1_pll/inst/clkout2_buf/O
	net (fo=50, routed)	1.600	7.457	clk2
SLICE_X3Y89	FDCE		r	div2_divisor_reg[11]_rep_0/C
	clock pessimism	-0.530	6.927	
	clock uncertainty	-0.214	6.714	
SLICE_X3Y89	FDCE (Setup_fdce_C_D)	-0.108	6.606	div2_divisor_reg[11]_rep_0
required time				
	arrival time		-1.687	
slack				
			4.919	

From Clock: clk4\_my\_pll To Clock: clk2\_my\_pll

Min Delay Paths

```

Slack (MET) :          0.232ns (arrival time - required time)
Source:               divisor_q_reg[4]/C
                      (rising edge-triggered cell FDCE clocked by clk4_my_pll {rise@0.000ns fall@5.000ns
period=10.000ns})
Destination:          div2_divisor_reg[4]/D
                      (rising edge-triggered cell FDCE clocked by clk2_my_pll {rise@10.000ns
fall@25.000ns period=30.000ns})
Path Group:           clk2_my_pll
Path Type:          Hold (Min at Fast Process Corner)
Requirement:          0.000ns (clk2_my_pll rise@10.000ns - clk4_my_pll rise@10.000ns)
Data Path Delay:      0.820ns (logic 0.141ns (17.193%) route 0.679ns (82.807%))
Logic Levels:         0
Clock Path Skew:     0.312ns (DCD - SCD - CPR)
Destination Clock Delay (DCD): -0.370ns = ( 9.630 - 10.000 )
Source Clock Delay (SCD): -0.592ns = ( 9.408 - 10.000 )
Clock Pessimism Removal (CPR): -0.089ns
Clock Uncertainty:    0.214ns ((TSJ^2 + DJ^2)^1/2) / 2 + PE
Total System Jitter (TSJ): 0.071ns
Discrete Jitter (DJ):   0.173ns
Phase Error (PE):     0.120ns

```

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock clk4_my_pll rise edge)				
N15		10.000	10.000	r
	net (fo=0)	0.000	10.000	r clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.177	10.177	r tp1_pll/inst/clk_in1
	net (fo=1, routed)	0.440	10.617	r tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT3)	-2.339	8.278	r tp1_pll/inst/plle2_adv_inst/CLKOUT3
	net (fo=1, routed)	0.510	8.788	r tp1_pll/inst/clk4_my_pll
BUFGCTRL_X0Y0	BUFG (Prop_bufg_I_O)	0.026	8.814	r tp1_pll/inst/clkout4_buf/O
	net (fo=51, routed)	0.594	9.408	r clk4
SLICE_X5Y68	FDCE		r	divisor_q_reg[4]/C
(clock clk2_my_pll rise edge)				
N15		10.000	10.000	r
	net (fo=0)	0.000	10.000	r clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.365	10.365	r tp1_pll/inst/clk_in1
	net (fo=1, routed)	0.481	10.846	r tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT1)	-2.657	8.189	r tp1_pll/inst/plle2_adv_inst/CLKOUT1
	net (fo=1, routed)	0.556	8.745	r tp1_pll/inst/clk2_my_pll
BUFGCTRL_X0Y2	BUFG (Prop_bufg_I_O)	0.029	8.774	r tp1_pll/inst/clkout2_buf/O
	net (fo=50, routed)	0.857	9.630	r clk2
SLICE_X5Y73	FDCE		r	div2_divisor_reg[4]/C
	clock pessimism	0.089	9.720	
	clock uncertainty	0.214	9.933	
SLICE_X5Y73	FDCE (Hold_fdce_C_D)	0.063	9.996	div2_divisor_reg[4]
required time				
	arrival time		-9.996	
slack				
			10.228	
			0.232	

From Clock: clk4\_my\_pll To Clock: clk3\_my\_pll

Max Delay Paths

---

Slack (MET) : 5.512ns (required time - arrival time)  
 Source: divisor\_q\_reg[11]/C  
 (rising edge-triggered cell FDCE clocked by clk4\_my\_pll {rise@0.000ns fall@5.000ns period=10.000ns})  
 Destination: div3\_divisor\_reg[11]\_rep/D  
 (rising edge-triggered cell FDCE clocked by clk3\_my\_pll {rise@20.000ns fall@35.000ns period=30.000ns})  
 Path Group: clk3\_my\_pll  
**Path Type:** Setup (Max at Slow Process Corner)  
 Requirement: 10.000ns (clk3\_my\_pll rise@20.000ns - clk4\_my\_pll rise@10.000ns)  
 Data Path Delay: 4.017ns (logic 0.456ns (11.351%) route 3.561ns (88.649%))  
 Logic Levels: 0  
 Clock Path Skew: -0.190ns (DCD - SCD + CPR)  
 Destination Clock Delay (DCD): -2.546ns = ( 17.454 - 20.000 )  
 Source Clock Delay (SCD): -2.885ns = ( 7.115 - 10.000 )  
 Clock Pessimism Removal (CPR): -0.530ns  
 Clock Uncertainty: 0.214ns ((TSJ^2 + DJ^2)^1/2) / 2 + PE  
 Total System Jitter (TSJ): 0.071ns  
 Discrete Jitter (DJ): 0.173ns  
 Phase Error (PE): 0.120ns

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock clk4_my_pll rise edge)				
N15		10.000	10.000	r
	net (fo=0)	0.000	10.000	r clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.948	10.948	r tp1_pll/inst/clk_in1
	net (fo=1, routed)	1.253	12.201	r tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT3)	-8.590	3.611	r tp1_pll/inst/plle2_adv_inst/CLKOUT3
	net (fo=1, routed)	1.704	5.315	r tp1_pll/inst/clk4_my_pll
BUFGCTRL_X0Y0	BUFGE (Prop_bufg_I_O)	0.096	5.411	r tp1_pll/inst/clkout4_buf/O
	net (fo=51, routed)	1.703	7.115	r clk4
SLICE_X0Y75	FDCE		r	divisor_q_reg[11]/C
(clock clk3_my_pll rise edge)				
N15		20.000	20.000	r
	net (fo=0)	0.000	20.000	r clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.814	20.814	r tp1_pll/inst/clk_in1
	net (fo=1, routed)	1.181	21.995	r tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT2)	-7.855	14.141	r tp1_pll/inst/plle2_adv_inst/CLKOUT2
	net (fo=1, routed)	1.625	15.766	r tp1_pll/inst/clk3_my_pll
BUFGCTRL_X0Y3	BUFGE (Prop_bufg_I_O)	0.091	15.857	r tp1_pll/inst/clkout3_buf/O
	net (fo=50, routed)	1.597	17.454	r clk3
SLICE_X3Y85	FDCE		r	div3_divisor_reg[11]_rep/C
	clock pessimism	-0.530	16.924	
	clock uncertainty	-0.214	16.711	
SLICE_X3Y85	FDCE (Setup_fdce_C_D)	-0.067	16.644	div3_divisor_reg[11]_rep
required time				
			16.644	
arrival time				
			-11.132	
slack				
			5.512	

From Clock: clk4\_my\_pll To Clock: clk3\_my\_pll

Min Delay Paths

```

Slack (MET) : 0.193ns (arrival time - required time)
Source: dividend_q_reg[9]/C
         (rising edge-triggered cell FDCE clocked by clk4_my_pll {rise@0.000ns fall@5.000ns
period=10.000ns})
Destination: div3_dividend_reg[9]/D
         (rising edge-triggered cell FDCE clocked by clk3_my_pll {rise@20.000ns
fall@35.000ns period=30.000ns})
Path Group: clk3_my_pll
Path Type: Hold (Min at Fast Process Corner)
Requirement: 0.000ns (clk3_my_pll rise@20.000ns - clk4_my_pll rise@20.000ns)
Data Path Delay: 0.788ns (logic 0.141ns (17.894%) route 0.647ns (82.106%))
Logic Levels: 0
Clock Path Skew: 0.323ns (DCD - SCD - CPR)
Destination Clock Delay (DCD): -0.390ns = ( 19.610 - 20.000 )
Source Clock Delay (SCD): -0.623ns = ( 19.377 - 20.000 )
Clock Pessimism Removal (CPR): -0.089ns
Clock Uncertainty: 0.214ns ((TSJ^2 + DJ^2)^1/2) / 2 + PE
Total System Jitter (TSJ): 0.071ns
Discrete Jitter (DJ): 0.173ns
Phase Error (PE): 0.120ns

```

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock clk4_my_pll rise edge)				
N15		20.000	20.000	r
	net (fo=0)	0.000	20.000	r clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.177	20.177	r tp1_pll/inst/clk_in1
	net (fo=1, routed)	0.440	20.617	r tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT3)	-2.339	18.278	r tp1_pll/inst/plle2_adv_inst/CLKOUT3
	net (fo=1, routed)	0.510	18.788	r tp1_pll/inst/clk4_my_pll
BUFGCTRL_X0Y0	BUFG (Prop_bufg_I_O)	0.026	18.814	r tp1_pll/inst/clkout4_buf/O
	net (fo=51, routed)	0.563	19.377	r clk4
SLICE_X9Y78	FDCE		r	dividend_q_reg[9]/C
(clock clk3_my_pll rise edge)				
N15		20.000	20.000	r
	net (fo=0)	0.000	20.000	r clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.365	20.365	r tp1_pll/inst/clk_in1
	net (fo=1, routed)	0.481	20.846	r tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT2)	-2.657	18.189	r tp1_pll/inst/plle2_adv_inst/CLKOUT2
	net (fo=1, routed)	0.556	18.745	r tp1_pll/inst/clk3_my_pll
BUFGCTRL_X0Y3	BUFG (Prop_bufg_I_O)	0.029	18.774	r tp1_pll/inst/clkout3_buf/O
	net (fo=50, routed)	0.837	19.610	r clk3
SLICE_X8Y83	FDCE		r	div3_dividend_reg[9]/C
	clock pessimism	0.089	19.700	
	clock uncertainty	0.214	19.913	
SLICE_X8Y83	FDCE (Hold_fdce_C_D)	0.059	19.972	div3_dividend_reg[9]
required time			-19.972	
arrival time			20.165	
slack			0.193	

## Abel DIDOUH

### From Clock: clk1\_my\_pll To Clock: clk4\_my\_pll

Max Delay Paths

```

Slack (MET) : 6.922ns (required time - arrival time)
  Source: div1_quotient_registre_reg[7]/C
            (rising edge-triggered cell FDCE clocked by clk1_my_pll {rise@0.000ns
fall@15.000ns period=30.000ns})
  Destination: quotient_reg[7]/D
            (rising edge-triggered cell FDCE clocked by clk4_my_pll {rise@0.000ns fall@5.000ns
period=10.000ns})
Path Group: clk4_my_pll
Path Type: Setup (Max at Slow Process Corner)
Requirement: 10.000ns (clk4_my_pll rise@10.000ns - clk1_my_pll rise@0.000ns)
Data Path Delay: 2.773ns (logic 0.642ns (23.154%) route 2.131ns (76.846%))
Logic Levels: 1 (LUT6=1)
Clock Path Skew: -0.122ns (DCD - SCD + CPR)
  Destination Clock Delay (DCD): -2.548ns = ( 7.452 - 10.000 )
  Source Clock Delay (SCD): -2.955ns
  Clock Pessimism Removal (CPR): -0.530ns
Clock Uncertainty: 0.214ns ((TSJ^2 + DJ^2)^1/2) / 2 + PE
  Total System Jitter (TSJ): 0.071ns
  Discrete Jitter (DJ): 0.173ns
  Phase Error (PE): 0.120ns

```

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock clk1_my_pll rise edge)				
N15		0.000	0.000 r	
	net (fo=0)	0.000	0.000 r clk (IN)	
N15	IBUF (Prop_ibuf_I_O)	0.948	0.948 r tp1_pll/inst/clk_in1	
	net (fo=1, routed)	1.253	2.201 r tp1_pll/inst/clkin1_ibufg/0	
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT0)	-8.590	-6.389 r tp1_pll/inst/plle2_adv_inst/CLKOUT0	
	net (fo=1, routed)	1.704	-4.685 r tp1_pll/inst/clk1_my_pll	
BUFGCTRL_X0Y1	BUFG (Prop_bufg_I_O)	0.096	-4.589 r tp1_pll/inst/clkout1_buf/0	
SLICE_X12Y81	FDCE	1.633	-2.955 r clk1	
			r div1_quotient_registre_reg[7]/C	
SLICE_X12Y81	FDCE (Prop_fdce_C_Q)	0.518	-2.437 r div1_quotient_registre_reg[7]/Q	
	net (fo=1, routed)	2.131	-0.307 r div1_quotient_registre[7]	
SLICE_X0Y83	LUT6 (Prop_lut6_I0_O)	0.124	-0.183 r quotient[7]_i_1/0	
	net (fo=1, routed)	0.000	-0.183 r p_0_in[7]	
SLICE_X0Y83	FDCE		r quotient_reg[7]/D	
(clock clk4_my_pll rise edge)				
N15		10.000	10.000 r	
	net (fo=0)	0.000	10.000 r clk (IN)	
N15	IBUF (Prop_ibuf_I_O)	0.814	10.814 r tp1_pll/inst/clk_in1	
	net (fo=1, routed)	1.181	11.995 r tp1_pll/inst/clkin1_ibufg/0	
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT3)	-7.855	4.141 r tp1_pll/inst/plle2_adv_inst/CLKOUT3	
	net (fo=1, routed)	1.625	5.766 r tp1_pll/inst/clk4_my_pll	
BUFGCTRL_X0Y0	BUFG (Prop_bufg_I_O)	0.091	5.857 r tp1_pll/inst/clkout4_buf/0	
	net (fo=51, routed)	1.595	7.452 r clk4	
SLICE_X0Y83	FDCE		r quotient_reg[7]/C	
	clock pessimism	-0.530	6.922	
	clock uncertainty	-0.214	6.709	
SLICE_X0Y83	FDCE (Setup_fdce_C_D)	0.031	6.740 r quotient_reg[7]	
				required time 6.740
				arrival time 0.183
				slack 6.922

From Clock: clk1\_my\_pll To Clock: clk4\_my\_pll

Min Delay Paths

---

Slack (MET) : 0.150ns (arrival time - required time)  
 Source: div1\_quotient\_registro[5]/C  
     (rising edge-triggered cell FDCE clocked by clk1\_my\_pll {rise@0.000ns fall@15.000ns period=30.000ns})  
 Destination: quotient\_reg[5]/D  
     (rising edge-triggered cell FDCE clocked by clk4\_my\_pll {rise@0.000ns fall@5.000ns period=10.000ns})  
 Path Group: clk4\_my\_pll  
**Path Type:** Hold (Min at Fast Process Corner)  
 Requirement: 0.000ns (clk4\_my\_pll rise@0.000ns - clk1\_my\_pll rise@0.000ns)  
 Data Path Delay: 0.802ns (logic 0.209ns (26.06%) route 0.593ns (73.935%))  
 Logic Levels: 1 (LUT6=1)  
 Clock Path Skew: 0.348ns (DCD - SCD - CPR)  
 Destination Clock Delay (DCD): -0.359ns  
 Source Clock Delay (SCD): -0.617ns  
 Clock Pessimism Removal (CPR): -0.089ns  
 Clock Uncertainty: 0.214ns ((TSJ^2 + DJ^2)^1/2) / 2 + PE  
 Total System Jitter (TSJ): 0.071ns  
 Discrete Jitter (DJ): 0.173ns  
 Phase Error (PE): 0.120ns

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock clk1_my_pll rise edge)				
N15	net (fo=0)	0.000	0.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.177	0.177 r	tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	net (fo=1, routed)	0.440	0.617	tp1_pll/inst/clk_in1_my_pll
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT0)	-2.339	-1.722 r	tp1_pll/inst/plle2_adv_inst/CLKOUT0
BUFGCTRL_X0Y1	net (fo=1, routed)	0.510	-1.212	tp1_pll/inst/clk1_my_pll
BUFGCTRL_X0Y1	BUFQ (Prop_bufq_I_O)	0.026	-1.186 r	tp1_pll/inst/clkout1_buf/O
SLICE_X10Y84	net (fo=50, routed)	0.569	-0.617	clk1
SLICE_X10Y84	FDCE		r	div1_quotient_registro[5]/C
<hr/>				
SLICE_X10Y84	FDCE (Prop_fdce_C_Q)	0.164	-0.453 r	div1_quotient_registro[5]/Q
SLICE_X0Y83	net (fo=1, routed)	0.593	0.140	div1_quotient_registro[5]
SLICE_X0Y83	LUT6 (Prop_lut6_I0_O)	0.045	0.185 r	quotient[5]_i_1/O
SLICE_X0Y83	net (fo=1, routed)	0.000	0.185	p_0_in[5]
SLICE_X0Y83	FDCE		r	quotient_reg[5]/D
<hr/>				
(clock clk4_my_pll rise edge)				
N15	net (fo=0)	0.000	0.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.365	0.365 r	tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	net (fo=1, routed)	0.481	0.846	tp1_pll/inst/clk_in1_my_pll
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT3)	-2.657	-1.811 r	tp1_pll/inst/plle2_adv_inst/CLKOUT3
BUFGCTRL_X0Y0	net (fo=1, routed)	0.556	-1.255	tp1_pll/inst/clk4_my_pll
BUFGCTRL_X0Y0	BUFQ (Prop_bufq_I_O)	0.029	-1.226 r	tp1_pll/inst/clkout4_buf/O
SLICE_X0Y83	net (fo=51, routed)	0.868	-0.359	clk4
SLICE_X0Y83	FDCE		r	quotient_reg[5]/C
SLICE_X0Y83	clock pessimism	0.089	-0.269	
SLICE_X0Y83	clock uncertainty	0.214	-0.056	
SLICE_X0Y83	FDCE (Hold_fdce_C_D)	0.091	0.035	quotient_reg[5]
<hr/>				
	required time		-0.035	
	arrival time		0.185	
<hr/>				
	slack		0.150	

## Abel DIDOUH

### From Clock: clk2\_my\_pll To Clock: clk4\_my\_pll

Max Delay Paths

```

Slack (MET) : 6.989ns (required time - arrival time)
Source: div2_remainder_reg[7]/C
         (rising edge-triggered cell FDCE clocked by clk2_my_pll {rise@10.000ns
fall@25.000ns period=30.000ns})
Destination: remainder_reg[7]/D
         (rising edge-triggered cell FDCE clocked by clk4_my_pll {rise@0.000ns fall@5.000ns
period=10.000ns})
Path Group: clk4_my_pll
Path Type: Setup (Max at Slow Process Corner)
Requirement: 10.000ns (clk4_my_pll rise@20.000ns - clk2_my_pll rise@10.000ns)
Data Path Delay: 2.675ns (logic 0.642ns (24.002%) route 2.033ns (75.998%))
Logic Levels: 1 (LUT6=1)
Clock Path Skew: -0.201ns (DCD - SCD + CPR)
Destination Clock Delay (DCD): -2.633ns = ( 17.367 - 20.000 )
Source Clock Delay (SCD): -2.961ns = ( 7.039 - 10.000 )
Clock Pessimism Removal (CPR): -0.530ns
Clock Uncertainty: 0.214ns ((TSJ^2 + DJ^2)^1/2) / 2 + PE
Total System Jitter (TSJ): 0.071ns
Discrete Jitter (DJ): 0.173ns
Phase Error (PE): 0.120ns

```

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
<hr/>				
	(clock clk2_my_pll rise edge)			
N15		10.000	10.000 r	
	net (fo=0)	0.000	10.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.948	10.948 r	tp1_pll/inst/clk_in1
	net (fo=1, routed)	1.253	12.201	tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT1)	-8.590	3.611 r	tp1_pll/inst/plle2_adv_inst/CLKOUT1
	net (fo=1, routed)	1.704	5.315	tp1_pll/inst/clk2_my_pll
BUFGCTRL_X0Y2	BUFG (Prop_bufg_I_O)	0.096	5.411 r	tp1_pll/inst/clkout2_buf/O
	net (fo=50, routed)	1.627	7.039	clk2
SLICE_X8Y72	FDCE		r	div2_remainder_reg[7]/C
<hr/>				
SLICE_X8Y72	FDCE (Prop_fdce_C_Q)	0.518	7.557 r	div2_remainder_reg[7]/Q
	net (fo=1, routed)	2.033	9.589	div2_remainder_reg[7]
SLICE_X8Y70	LUT6 (Prop_lut6_I2_O)	0.124	9.713 r	remainder[7]_i_1/O
	net (fo=1, routed)	0.000	9.713	remainder[7]_i_1_n_0
SLICE_X8Y70	FDCE		r	remainder_reg[7]/D
<hr/>				
	(clock clk4_my_pll rise edge)			
N15		20.000	20.000 r	
	net (fo=0)	0.000	20.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.814	20.814 r	tp1_pll/inst/clk_in1
	net (fo=1, routed)	1.181	21.995	tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT3)	-7.855	14.141 r	tp1_pll/inst/plle2_adv_inst/CLKOUT3
	net (fo=1, routed)	1.625	15.766	tp1_pll/inst/clk4_my_pll
BUFGCTRL_X0Y0	BUFG (Prop_bufg_I_O)	0.091	15.857 r	tp1_pll/inst/clkout4_buf/O
	net (fo=51, routed)	1.510	17.367	clk4
SLICE_X8Y70	FDCE		r	remainder_reg[7]/C
	clock pessimism	-0.530	16.837	
	clock uncertainty	-0.214	16.624	
SLICE_X8Y70	FDCE (Setup_fdce_C_D)	0.079	16.703	remainder_reg[7]
<hr/>				
	required time		16.703	
	arrival time		-9.713	
	slack		6.989	

From Clock: clk2\_my\_pll To Clock: clk4\_my\_pll

Min Delay Paths

```

Slack (MET) :          0.134ns (arrival time - required time)
Source:           div2_quotient_registre_reg[8]/C
                  (rising edge-triggered cell FDCE clocked by clk2_my_pll {rise@10.000ns
fall@25.000ns period=30.000ns})
Destination:        quotient_reg[8]/D
                  (rising edge-triggered cell FDCE clocked by clk4_my_pll {rise@0.000ns fall@5.000ns
period=10.000ns})
Path Group:         clk4_my_pll
Path Type:        Hold (Min at Fast Process Corner)
Requirement:       0.000ns (clk4_my_pll rise@10.000ns - clk2_my_pll rise@10.000ns)
Data Path Delay:   0.759ns (logic 0.186ns (24.507%) route 0.573ns (75.493%))
Logic Levels:      1 (LUT6=1)
Clock Path Skew:   0.320ns (DCD - SCD - CPR)
Destination Clock Delay (DCD): -0.357ns = ( 9.643 - 10.000 )
Source Clock Delay (SCD):    -0.587ns = ( 9.413 - 10.000 )
Clock Pessimism Removal (CPR): -0.089ns
Clock Uncertainty: 0.214ns ((TSJ^2 + DJ^2)^1/2) / 2 + PE
Total System Jitter (TSJ): 0.071ns
Discrete Jitter (DJ): 0.173ns
Phase Error (PE): 0.120ns

```

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock clk2_my_pll rise edge)				
N15		10.000	10.000 r	
	net (fo=0)	0.000	10.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.177	10.177 r	tp1_pll/inst/clk_in1
	net (fo=1, routed)	0.440	10.617	tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT1)	-2.339	8.278 r	tp1_pll/inst/plle2_adv_inst/CLKOUT1
	net (fo=1, routed)	0.510	8.788	tp1_pll/inst/clk2_my_pll
BUFGCTRL_X0Y2	BUFG (Prop_bufg_I_O)	0.026	8.814 r	tp1_pll/inst/clkout2_buf/O
	net (fo=50, routed)	0.599	9.413	clk2
SLICE_X1Y87	FDCE		r	div2_quotient_registre_reg[8]/C
(clock clk4_my_pll rise edge)				
N15		10.000	10.000 r	
	net (fo=0)	0.000	10.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.365	10.365 r	tp1_pll/inst/clk_in1
	net (fo=1, routed)	0.481	10.846	tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT3)	-2.657	8.189 r	tp1_pll/inst/plle2_adv_inst/CLKOUT3
	net (fo=1, routed)	0.556	8.745	tp1_pll/inst/clk4_my_pll
BUFGCTRL_X0Y0	BUFG (Prop_bufg_I_O)	0.029	8.774 r	tp1_pll/inst/clkout4_buf/O
	net (fo=51, routed)	0.870	9.643	clk4
SLICE_X0Y85	FDCE		r	quotient_reg[8]/C
	clock pessimism	0.089	9.733	
	clock uncertainty	0.214	9.946	
SLICE_X0Y85	FDCE (Hold_fdce_C_D)	0.092	10.038	quotient_reg[8]
	required time		-10.038	
	arrival time		10.172	
	slack		0.134	

## Abel DIDOUH

### From Clock: clk3\_my\_pll To Clock: clk4\_my\_pll

Max Delay Paths

```
-----
Slack (MET) : 6.888ns (required time - arrival time)
Source:      div3_remainder_registre_reg[3]/C
              (rising edge-triggered cell FDCE clocked by clk3_my_pll {rise@20.000ns
fall@35.000ns period=30.000ns})
Destination: remainder_reg[3]/D
              (rising edge-triggered cell FDCE clocked by clk4_my_pll {rise@0.000ns fall@5.000ns
period=10.000ns})
Path Group:  clk4_my_pll
Path Type:   Setup (Max at Slow Process Corner)
Requirement: 10.000ns (clk4_my_pll rise@30.000ns - clk3_my_pll rise@20.000ns)
Data Path Delay: 2.643ns (logic 0.642ns (24.291%) route 2.001ns (75.709%))
Logic Levels: 1 (LUT6=1)
Clock Path Skew: -0.284ns (DCD - SCD + CPR)
Destination Clock Delay (DCD): -2.634ns = ( 27.366 - 30.000 )
Source Clock Delay (SCD): -2.879ns = ( 17.121 - 20.000 )
Clock Pessimism Removal (CPR): -0.530ns
Clock Uncertainty: 0.214ns ((TSJ^2 + DJ^2)^1/2) / 2 + PE
Total System Jitter (TSJ): 0.071ns
Discrete Jitter (DJ): 0.173ns
Phase Error (PE): 0.120ns
```

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock clk3_my_pll rise edge)				
N15		20.000	20.000 r	
		0.000	20.000 r	clk (IN)
N15	net (fo=0)	0.000	20.000	tp1_pll/inst/clk_in1
	IBUF (Prop_ibuf_I_O)	0.948	20.948 r	tp1_pll/inst/clkin1_ibufg/O
	net (fo=1, routed)	1.253	22.201	tp1_pll/inst/clk_in1_my_pll
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT2)	-8.590	13.611 r	tp1_pll/inst/plle2_adv_inst/CLKOUT2
	net (fo=1, routed)	1.704	15.315	tp1_pll/inst/clk3_my_pll
BUFGCTRL_X0Y3	BUFG (Prop_bufg_I_O)	0.096	15.411 r	tp1_pll/inst/clkout3_buf/O
	net (fo=50, routed)	1.709	17.121	clk3
SLICE_X6Y70	FDCE		r	div3_remainder_registre_reg[3]/C
(clock clk4_my_pll rise edge)				
N15		30.000	30.000 r	
		0.000	30.000 r	clk (IN)
N15	net (fo=0)	0.000	30.000	tp1_pll/inst/clk_in1
	IBUF (Prop_ibuf_I_O)	0.814	30.814 r	tp1_pll/inst/clkin1_ibufg/O
	net (fo=1, routed)	1.181	31.995	tp1_pll/inst/clk_in1_my_pll
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT3)	-7.855	24.141 r	tp1_pll/inst/plle2_adv_inst/CLKOUT3
	net (fo=1, routed)	1.625	25.766	tp1_pll/inst/clk4_my_pll
BUFGCTRL_X0Y0	BUFG (Prop_bufg_I_O)	0.091	25.857 r	tp1_pll/inst/clkout4_buf/O
	net (fo=51, routed)	1.509	27.366	clk4
SLICE_X9Y71	FDCE		r	remainder_reg[3]/C
	clock pessimism	-0.530	26.836	
	clock uncertainty	-0.214	26.623	
SLICE_X9Y71	FDCE (Setup_fdce_C_D)	0.029	26.652	remainder_reg[3]
required time				
			26.652	
arrival time				
			-19.764	
slack				
			6.888	

From Clock: clk3\_my\_pll To Clock: clk4\_my\_pll

Min Delay Paths

```

Slack (MET) :          0.186ns (arrival time - required time)
Source:           div3_quotient_registre_reg[2]/C
                  (rising edge-triggered cell FDCE clocked by clk3_my_pll {rise@20.000ns
fall@35.000ns period=30.000ns})
Destination:        quotient_reg[2]/D
                  (rising edge-triggered cell FDCE clocked by clk4_my_pll {rise@0.000ns fall@5.000ns
period=10.000ns})
Path Group:         clk4_my_pll
Path Type:        Hold (Min at Fast Process Corner)
Requirement:       0.000ns (clk4_my_pll rise@20.000ns - clk3_my_pll rise@20.000ns)
Data Path Delay:   0.810ns (logic 0.209ns (25.795%) route 0.601ns (74.205%))
Logic Levels:      1 (LUT6=1)
Clock Path Skew:   0.320ns (DCD - SCD - CPR)
Destination Clock Delay (DCD): -0.391ns = ( 19.609 - 20.000 )
Source Clock Delay (SCD): -0.621ns = ( 19.379 - 20.000 )
Clock Pessimism Removal (CPR): -0.089ns
Clock Uncertainty: 0.214ns ((TSJ^2 + DJ^2)^1/2) / 2 + PE
Total System Jitter (TSJ): 0.071ns
Discrete Jitter (DJ): 0.173ns
Phase Error (PE): 0.120ns

```

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock clk3_my_pll rise edge)				
N15		20.000	20.000 r	
	net (fo=0)	0.000	20.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.177	20.177 r	tp1_pll/inst/clk_in1
	net (fo=1, routed)	0.440	20.617	tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT2)	-2.339	18.278 r	tp1_pll/inst/plle2_adv_inst/CLKOUT2
	net (fo=1, routed)	0.510	18.788	tp1_pll/inst/clk3_my_pll
BUFGCTRL_X0Y3	BUFG (Prop_bufg_I_O)	0.026	18.814 r	tp1_pll/inst/clkout3_buf/O
	net (fo=50, routed)	0.565	19.379	clk3
SLICE_X8Y80	FDCE		r	div3_quotient_registre_reg[2]/C
(clock clk4_my_pll rise edge)				
N15		20.000	20.000 r	
	net (fo=0)	0.000	20.000 r	clk (IN)
N15	IBUF (Prop_ibuf_I_O)	0.365	20.365 r	tp1_pll/inst/clk_in1
	net (fo=1, routed)	0.481	20.846	tp1_pll/inst/clkin1_ibufg/O
PLLE2_ADV_X0Y1	PLLE2_ADV (Prop_plle2_adv_CLKIN1_CLKOUT3)	-2.657	18.189 r	tp1_pll/inst/plle2_adv_inst/CLKOUT3
	net (fo=1, routed)	0.556	18.745	tp1_pll/inst/clk4_my_pll
BUFGCTRL_X0Y0	BUFG (Prop_bufg_I_O)	0.029	18.774 r	tp1_pll/inst/clkout4_buf/O
	net (fo=51, routed)	0.836	19.609	clk4
SLICE_X9Y82	FDCE		r	quotient_reg[2]/C
	clock pessimism	0.089	19.699	
	clock uncertainty	0.214	19.912	
SLICE_X9Y82	FDCE (Hold_fdce_C_D)	0.091	20.003	quotient_reg[2]
required time			-20.003	
arrival time			20.189	
slack			0.186	

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