ABEL TESFAI

Abelntesfai@gmail.com • +1 (651) 399 3785 • 3 Villar Ct, Saint Paul, MN, 55116

WORK EXPERIENCE

SIGNAL & POWER INTEGRITY ENGINEER IBM Rochester 06/21/2021-Present

- Provided technical guidance to circuit/package/board teams to ensure electrical design meets signal and power integrity targets.
- Collaborated with validation teams to define test plans and support lab debug across silicon, board, and package interfaces.
- Participated in cross-functional design closure reviews and system-level PI/SI debug.
- Performed full-package and board-level PI/SI analysis across DDR, Core and PCIe power domains.
- Designed and optimized multi-tier decoupling networks including Diecap, package cap, and card cap.
- Directed loop inductance extraction, capacitor placement refinement, and Z-targeting for critical high-current rails.
- Spearheaded signal integrity design and verification for high-speed interfaces; defined SILO structure and validated routing against SI constraints.
- Performed full-wave SI simulations to evaluate eye margin, crosstalk, and channel impedance.
- Partnered with cross-functional teams including layout, silicon design, packaging, and board teams to deliver optimized PDNs.

Hardware Engineer Internship IBM Rochester 05/20/2019-06/21/2021

- Supported the Quantum Hardware team with lab measurements and hardware validation tasks.
- Performed VNA, TDR, and oscilloscope measurements to support simulation correlation.
- Gained hands-on experience soldering components (decaps, resistors) to boards for testing.
- Assisted with test setup configuration and data collection for system-level debug.

EDUCATION

Minnesota State University, MANKATO **Bachelor's Degree in Electrical Engineering**

Minnesota State University, MANKATO **Masters's Degree in Electrical Engineering**

PROFESSIONAL SKILLS

- PI Simulation: PowerDC, Siwave, PowerSI, OptimizePI, Ansys Circuit, Simplis, Hspice
- SI Simulation: HFSS, HFSS 3D Layout, 2D Extractor, Siwave, Hspice
- High-Speed Interface Focus: DDR4, DDR5, LPDDR, PCIe
- Layout and Modeling: Cadence Allegro, layout stack-up design, Z-targeting, decap planning
- Programming: Python, C, Perl
- Measurement Familiarity: VNA, TDR, PDN impedance
- Strong communication, debug strategy, and technical documentation skills