2021 Digital IC Design Homework 2

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Simulation Result

Functional simulation	Level	Gate-level simulation	Level	Gate-level simulation time	simulation time (ns) 123792.400

```
#         4024 data is correct
#         4025 data is correct
#         4026 data is correct
#         4027 data is correct
#         4028 data is correct
#         4029 data is correct
#         4030 data is correct
#         4031 data is correct
#         4032 data is correct
# --------------------PASS-----
# All data have been generated
# Break in Module booth_tb at

VSIM 67>
```

(your pre-sim result)

```
#         4027 data is correct
#         4028 data is correct
#         4029 data is correct
#         4030 data is correct
#         4031 data is correct
#         4032 data is correct
# --------------------PASS--------------------
# All data have been generated successfully!
# ** Note: $finish    : D:/hsuan/PhD/109_2/D
#    Time: 123792400 ps  Iteration: 0  Instar
# 1
# Break in Module booth_tb at D:/hsuan/PhD/1(

VSIM 21>
```

(your post-sim result)

Synthesis Result

Total logic elements	132
Total memory bit	0
Embedded multiplier 9-bit element	0
Clock width (Cycle)	30.7

Flow Summary	
Flow Status	Successful - Sat Apr 03 18:18:57 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	booth
Top-level Entity Name	booth
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	132 / 68,416 (< 1 %)
Total combinational functions	132 / 68,416 (< 1 %)
Dedicated logic registers	0 / 68,416 (0 %)
Total registers	0
Total pins	24 / 622 (4 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

(your flow summary)

Description of your design

主要依照 hw2 文件的敘述使用 for loop 去描述本作業的硬體，每次 loop 會根據最後兩個位元採取不同的 case (加、減或不變)。

Scoring = Clock width