

2021 Digital IC Design Homework 4

NAME	黃柏瑄																																						
Student ID	P78081528																																						
Simulation Result																																							
Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	simulation time (ns) 5308457.027																																		
<pre> VSM 203> run -all # ----- # START!!! Simulation Start # ----- # Result image is correct ! # ----- # ----- S U M M A R Y ----- # Congratulations! Result image data have been generated successfully! The result is PASS!! # ----- # ** Note: \$finish : D:/hsuan/PhD/109_2/DIC/DIC_hw/HW4/src/testfixture.v(123) # Time: 3276820 ns Iteration: 0 Instance: /testfixture # 1 # Break in Module testfixture at D:/hsuan/PhD/109_2/DIC/DIC_hw/HW4/src/testfixture.v line 123 </pre> <p style="text-align: center; color: gray;">(your pre-sim result)</p>			<pre> VSM 254> run -all # ----- # START!!! Simulation Start # ----- # Result image is correct ! # ----- # ----- S U M M A R Y ----- # Congratulations! Result image data have been generated successfully! The result is PASS!! # ----- # ** Note: \$finish : D:/hsuan/PhD/109_2/DIC/DIC_hw/HW4/src/simulation/modelsim/testfixtu # Time: 5308457027 ps Iteration: 0 Instance: /testfixture # 1 # Break in Module testfixture at D:/hsuan/PhD/109_2/DIC/DIC_hw/HW4/src/simulation/modelsim/ # Compile of testfixture.v was successful. </pre> <p style="text-align: center; color: gray;">(your post-sim result)</p>																																				
Synthesis Result																																							
Total logic elements		339																																					
Total memory bit		0																																					
Embedded multiplier 9-bit element		0																																					
Clock width (Cycle)		16.2																																					
<div style="display: flex; align-items: flex-start;"> <table border="1" style="width: 40%; border-collapse: collapse; background-color: #f0f0f0;"> <thead> <tr style="background-color: #0070c0; color: white;"> <th colspan="2">Flow Summary</th> </tr> </thead> <tbody> <tr><td>Flow Status</td><td>Successful - Wed May 26 15:52:26 2021</td></tr> <tr><td>Quartus II 64-Bit Version</td><td>13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition</td></tr> <tr><td>Revision Name</td><td>MFE</td></tr> <tr><td>Top-level Entity Name</td><td>MFE</td></tr> <tr><td>Family</td><td>Cyclone II</td></tr> <tr><td>Device</td><td>EP2C70F896C8</td></tr> <tr><td>Timing Models</td><td>Final</td></tr> <tr><td>Total logic elements</td><td>339 / 68,416 (< 1 %)</td></tr> <tr><td> Total combinational functions</td><td>338 / 68,416 (< 1 %)</td></tr> <tr><td> Dedicated logic registers</td><td>109 / 68,416 (< 1 %)</td></tr> <tr><td>Total registers</td><td>109</td></tr> <tr><td>Total pins</td><td>57 / 622 (9 %)</td></tr> <tr><td>Total virtual pins</td><td>0</td></tr> <tr><td>Total memory bits</td><td>0 / 1,152,000 (0 %)</td></tr> <tr><td>Embedded Multiplier 9-bit elements</td><td>0 / 300 (0 %)</td></tr> <tr><td>Total PLLs</td><td>0 / 4 (0 %)</td></tr> </tbody> </table> <div style="margin-left: 20px; color: gray;">(your flow summary)</div> </div>						Flow Summary		Flow Status	Successful - Wed May 26 15:52:26 2021	Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition	Revision Name	MFE	Top-level Entity Name	MFE	Family	Cyclone II	Device	EP2C70F896C8	Timing Models	Final	Total logic elements	339 / 68,416 (< 1 %)	Total combinational functions	338 / 68,416 (< 1 %)	Dedicated logic registers	109 / 68,416 (< 1 %)	Total registers	109	Total pins	57 / 622 (9 %)	Total virtual pins	0	Total memory bits	0 / 1,152,000 (0 %)	Embedded Multiplier 9-bit elements	0 / 300 (0 %)	Total PLLs	0 / 4 (0 %)
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Description of your design																																							
<p>主要流程：走到中心點直到第 16383 個 → 讀九宮格進來排序 → 把中位數寫入中心點位置→走到下一個中心點。本作業所使用的排序為插入排序，做法是在每一個暫存器前進行比較，並將輸入放到按照順序的暫存器中，寫入時將第 4 個（也就是中間的數值）輸出。Padding 部分是使用邊界偵測，如果有超出邊界則會傳入 0 到排序的暫存器中。Software Verification 部分是使用 python 以及 scikit-image 提供的工具，並按照作業文件提供的流程從輸入圖片產生兩個檔案。</p>																																							

Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (longest gate-level simulation time in ns)