2021 Digital IC Design Homework 5

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Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	simulation time (ns): 17210.900

```
# ------------------------------------------------------
# FFT dataout on pattern         880 ~         895, PASS!!
# FFT dataout on pattern         896 ~         911, PASS!!
# FFT dataout on pattern         912 ~         927, PASS!!
# FFT dataout on pattern         928 ~         943, PASS!!
# FFT dataout on pattern         944 ~         959, PASS!!
# FFT dataout on pattern         960 ~         975, PASS!!
# FFT dataout on pattern         976 ~         991, PASS!!
# FFT dataout on pattern         992 ~        1007, PASS!!
# FFT dataout on pattern        1008 ~        1023, PASS!!
# ------------------------------------------------------
#
# Congratulations! All data have been generated successfully!
#
# -------------------------PASS-------------------------
#
# ** Note: $finish    : D:/hsuan/PhD/109_2/DIC/DIC_hw/HW5/src/t
#    Time: 53450 ns  Iteration: 0  Instance: /testfixture1
# 1
# Break in Module testfixture1 at D:/hsuan/PhD/109_2/DIC/DIC_hw
```

(your pre-sim result)

```
# ------------------------------------------------------
# FFT dataout on pattern         880 ~         895, PASS!!
# FFT dataout on pattern         896 ~         911, PASS!!
# FFT dataout on pattern         912 ~         927, PASS!!
# FFT dataout on pattern         928 ~         943, PASS!!
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# FFT dataout on pattern         960 ~         975, PASS!!
# FFT dataout on pattern         976 ~         991, PASS!!
# FFT dataout on pattern         992 ~        1007, PASS!!
# FFT dataout on pattern        1008 ~        1023, PASS!!
# ------------------------------------------------------
#
# Congratulations! All data have been generated successfully!
#
# -------------------------PASS-------------------------
#
# ** Note: $finish    : D:/hsuan/PhD/109_2/DIC/DIC_hw/HW5/src/simulat
#    Time: 17210900 ps  Iteration: 0  Instance: /testfixture1
# 1
# Break in Module testfixture1 at D:/hsuan/PhD/109_2/DIC/DIC_hw/HW5/s
```

(your post-sim result)

Synthesis Result

Total logic elements	9548
Total memory bit	0
Embedded multiplier 9-bit element	142
Clock width (Cycle)	16.1

Flow Summary

Flow Status	Successful - Mon Jun 21 20:40:28 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	FAS
Top-level Entity Name	FAS
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	9,548 / 68,416 (14 %)
Total combinational functions	9,003 / 68,416 (13 %)
Dedicated logic registers	5,028 / 68,416 (7 %)
Total registers	5028
Total pins	554 / 622 (89 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	142 / 300 (47 %)
Total PLLs	0 / 4 (0 %)

(your flow summary)

Description of your design

因為本次作業很明顯的分成三個模組，所以我用最外層的模組 FAS 來描述三個子模組的接線，接著將子模組實作測試，再換下一個子模組。

首先是 FIR，我按照課程投影片的方法設計，使得每一個 cycle 會將前一個輸入傳下去，最後將乘完的結果作累加後當作輸出。

在處理 FFT 子模組時，我有遇到來自 FIR 的誤差會導致 FFT 輸出無法通過 tb，詢問助教後，將原先的輸入部分

```
y[15] <= fir_d;
```

改成

```
y[15] <= fir_d + {15'd0, fir_d[15]};
```

後就可以避免誤差了。關於 FFT 有不同的 stage，我的實作方式沒有採用之前的 control unit 的 state 設計方式，而是在處理 stage 時觸發下一個 stage 可以在下一個 cycle 進行。

最後 Analysis 需要找出最大，由於不需要排序，所以我原先採用 O(n)的方式找出最大值，結果 cycle 降到 30 左右就會跑出錯誤結果。因此後來改用 O(lg(n))也就是先兩兩比較，再將大者做比較，此種做法就可以用更低的 cycle 來完成。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (longest gate-level simulation time in ns)*