2021 Digital IC Design Homework 1

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Simulation Result

Functional simulation	Level	Gate-level simulation	Level	Gate-level simulation time	simulation time (ns) 14436

```
#          503 data is correct
#          504 data is correct
#          505 data is correct
#          506 data is correct
#          507 data is correct
#          508 data is correct
#          509 data is correct
#          510 data is correct
#          511 data is correct
# --------------------PASS--------------------
# All data have been generated successfully!
# Break in Module RCA_tb at D:/hsuan/PhD/109_

VSIM 3>
```

(your pre-sim result)

```
#          506 data is correct
#          507 data is correct
#          508 data is correct
#          509 data is correct
#          510 data is correct
#          511 data is correct
# --------------------PASS--------------------
# All data have been generated successfully!
# ** Note: $finish    : D:/hsuan/PhD/109_2/DI
#    Time: 14436 ns  Iteration: 0  Instance:
# 1
# Break in Module RCA_tb at D:/hsuan/PhD/109_

VSIM 19>
```

(your post-sim result)

Synthesis Result

Total logic elements	10
Total memory bit	0
Embedded multiplier 9-bit element	0
Clock Width (Cycle)	1.4

Flow Summary	
Flow Status	Successful - Sat Apr 03 12:03:58 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	RCA
Top-level Entity Name	RCA
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	10 / 68,416 (< 1 %)
Total combinational functions	10 / 68,416 (< 1 %)
Dedicated logic registers	0 / 68,416 (0 %)
Total registers	0
Total pins	14 / 622 (2 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

(your flow summary)

Description of your design

按照 hw1 文件的步驟，先使用 XOR 及 AND 做出一個半加器 (Half adder)，再使用兩個半加器產生一個全加器 (Full adder)，最後用四個全加器拼成一個 4-bit 加法器。