2021 Digital IC Design Homework 4

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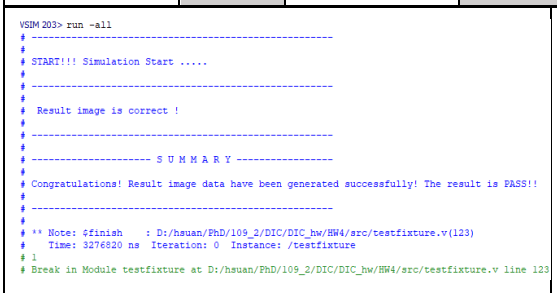
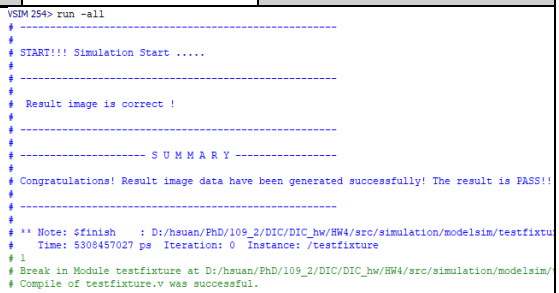
Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	simulation time (ns) 5308457.027



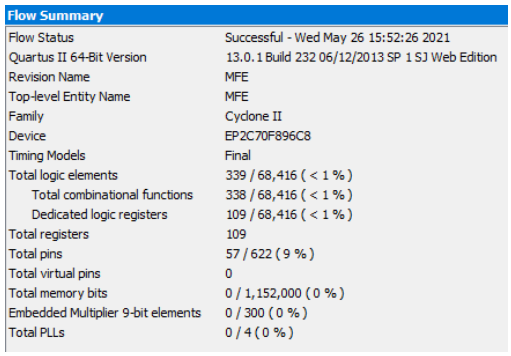
(your pre-sim result)



(your post-sim result)

Synthesis Result

Total logic elements	339
Total memory bit	0
Embedded multiplier 9-bit element	0
Clock width (Cycle)	16.2



Flow Summary	
Flow Status	Successful - Wed May 26 15:52:26 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	MFE
Top-level Entity Name	MFE
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	339 / 68,416 (< 1 %)
Total combinational functions	338 / 68,416 (< 1 %)
Dedicated logic registers	109 / 68,416 (< 1 %)
Total registers	109
Total pins	57 / 622 (9 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

(your flow summary)

Description of your design

主要流程：走到中心點直到第 16383 個 → 讀九宮格進來排序 → 把中位數寫入中心點位置→走到下一個中心點。本作業所使用的排序為插入排序，做法是在每一個暫存器前進行比較，並將輸入放到按照順序的暫存器中，寫入時將第 4 個 (也就是中間的數值) 輸出。Padding 部分是使用邊界偵測，如果有超出邊界則會傳入 0 到排序的暫存器中。Software Verification 部分是使用 python 以及 scikit-image 提供的工具，並按照作業文件提供的流程從輸入圖片產生兩個檔案。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (longest gate-level simulation time in ns)*