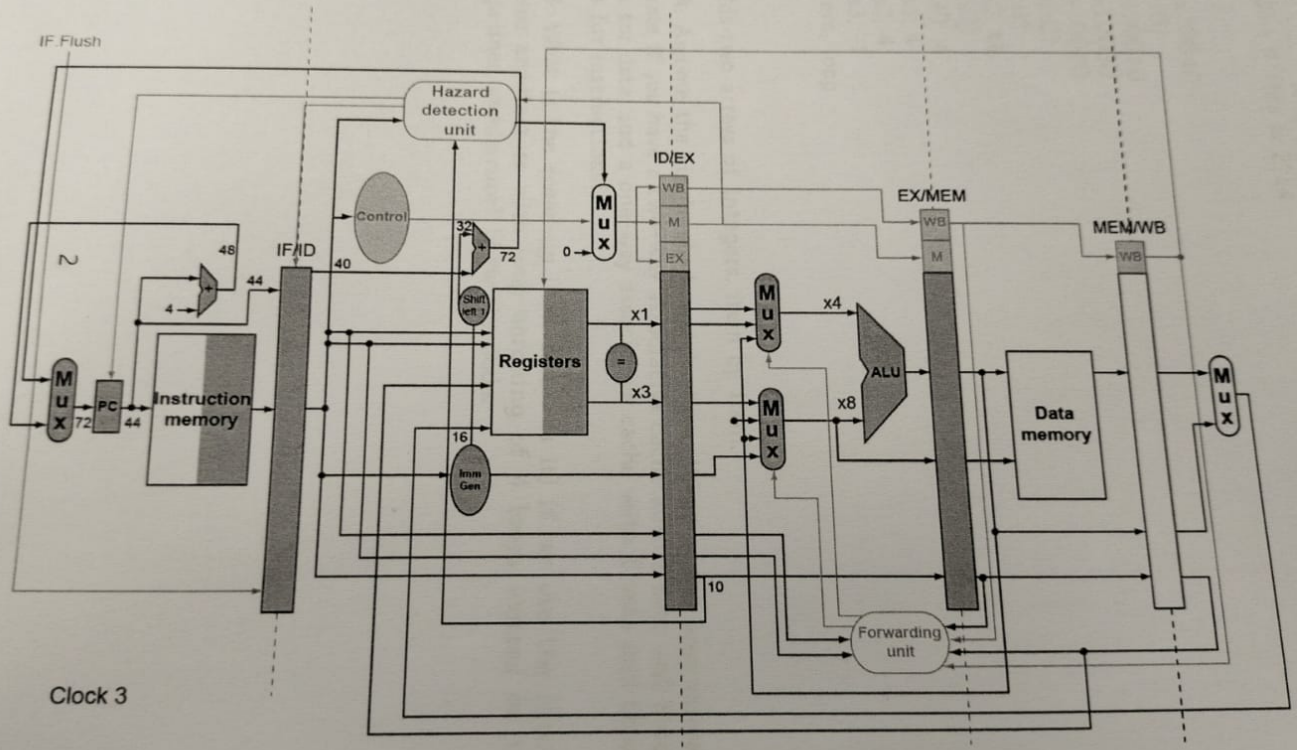
IF.Flush
Hazard detection unit
Control
ID/EX
EX/MEM
MEM/WB
WB
M
EX
IF/ID
Mux
PC
Instruction memory
Registers
Shift left 1
Imm Gen
ALU
Data memory
Forwarding unit
x1
x3
x4
x8
0
2
4
48
44
40
32
72
16
10

Clock 3

Exercise 2. Consider the following code:

```
.data
v:      .word 10,-1,-72,45,2,...    # array of 16384 integers
w:      .word 8,9,-7,-4,25,...      # array of 16384 integers
z:      .word 0,0,0,...     # array of 16384 integers
n:      .word 16384 # This is 2^14

.text
        lui s0, 0x10040
        lw s3, 0(s0)
        lui s0, 0x10010
        lui s1, 0x10020
        lui s2, 0x10030
loop:   lw t0, 0(s0)
        lw t1, 0(s1)
        add t2, t0, t1
        sw t2, 0(s2)
        addi s0, s0, 4
        addi s1, s1, 4
        addi s2, s2, 4
        addi s3, s3, -1
        bne s3, zero, loop
        li a7, 10
        ecall
```

This program adds two arrays of integers, item by item.

1. **Question A:** Assume the single clock architecture. What is the approximate total miss rate if you have a two-way associative cache with 8 sets and blocks of 64 bytes for data, and a one-way associative cache with 8 sets and blocks of 64 bytes for instructions?

2. **Question B:** What is the speed-up (how faster is it) if we use the Risc-V multiple issue architecture with loop unrolling of 4 loops instead of the standard pipelined architecure? Show the code.

Exercise 3. Uncle Jack doesn't like incomplete explanations. He just told me that he is not too thrilled about Figure 1, the pipeline architecture. Too many details missing. In particular, there is no forwording unit for the comparator used in stage IF to implement branches, and no hazard detection unit as well. Can we make Uncle Jack happy? Can you show an example (code) of forwarding for a branch instruction and an example (code) of a bubble caused by a branch istruction? Then, please give a design for the forwarding unit needed to implement branches correctly.