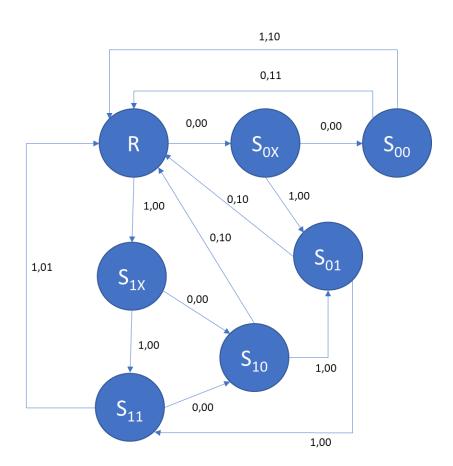
Exam - Computer Architecture Unit I [18/01/2023] (A) - Solution

Exercise 1 (8 points) Design a sequential circuit with an input x and two outputs z1 and z0. The output z1 must be equal to 1 if the last three bits on input contain at least two 0, whereas z0 must be equal to 1 if the last three bits are the same (i.e., 3 zeros or 3 ones). Do not consider overlaps. Draw the sequential circuit (use a ROM for the combinational part).

Example x 10100000111 z1 00010010000

z0 00000010001



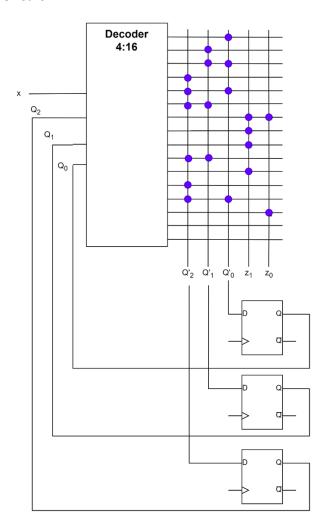
States encoding:

| R | 000 |
|------------|-----|
| SOX | 001 |
| S1X | 010 |
| S00 | 011 |
| S01 | 100 |
| S10 | 101 |
| S11 | 110 |

Outputs and next state table:

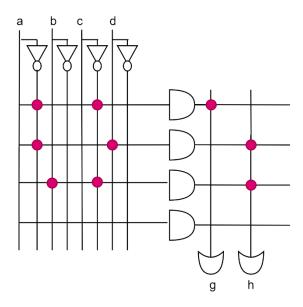
| CS | S ₂ | S ₁ | S ₀ | х | NS | S ₂ ' | S ₁ ' | S ₀ ' | z1 | z0 |
|-----|----------------|----------------|----------------|---|-----|------------------|------------------|------------------|----|----|
| R | 0 | 0 | 0 | 0 | SOX | 0 | 0 | 1 | 0 | 0 |
| R | 0 | 0 | 0 | 1 | S1X | 0 | 1 | 0 | 0 | 0 |
| SOX | 0 | 0 | 1 | 0 | S00 | 0 | 1 | 1 | 0 | 0 |
| SOX | 0 | 0 | 1 | 1 | S01 | 1 | 0 | 0 | 0 | 0 |
| S1X | 0 | 1 | 0 | 0 | S10 | 1 | 0 | 1 | 0 | 0 |
| S1X | 0 | 1 | 0 | 1 | S11 | 1 | 1 | 0 | 0 | 0 |
| S00 | 0 | 1 | 1 | 0 | R | 0 | 0 | 0 | 1 | 1 |
| S00 | 0 | 1 | 1 | 1 | R | 0 | 0 | 0 | 1 | 0 |
| S01 | 1 | 0 | 0 | 0 | R | 0 | 0 | 0 | 1 | 0 |
| S01 | 1 | 0 | 0 | 1 | S11 | 1 | 1 | 0 | 0 | 0 |
| S10 | 1 | 0 | 1 | 0 | R | 0 | 0 | 0 | 1 | 0 |
| S10 | 1 | 0 | 1 | 1 | S01 | 1 | 0 | 0 | 0 | 0 |
| S11 | 1 | 1 | 0 | 0 | S10 | 1 | 0 | 1 | 0 | 0 |
| S11 | 1 | 1 | 0 | 1 | R | 0 | 0 | 0 | 0 | 1 |

Circuit:



Exercise 2 (1+2+1+2 points) Consider the PLA shown below.

- Write the boolean expressions for functions $g \in h$
- Transform the boolean expression $f=g\oplus h$, using boolean algebra's axiom, rules, and theorems, in canonical SOP form
- Write down the truth table for *f*
- ullet Write down the minimal SOP and POS expressions for f



$$g = \bar{a}\bar{c}$$

$$h = \bar{a}d + b\bar{c}$$

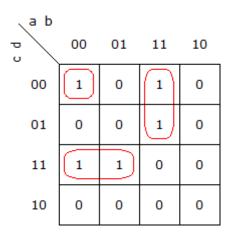
Canonical SOP form:

$$f = \bar{a}\bar{c} \ \oplus (\bar{a}d + b\bar{c}) = ab\bar{c} + \bar{a}cd + \bar{a}\bar{b}\bar{c}\bar{d} = ab\bar{c}d + ab\bar{c}\bar{d} + \bar{a}bcd + \bar{a}\bar{b}cd + \bar{a}\bar{b}\bar{c}\bar{d}$$

Truth table for f:

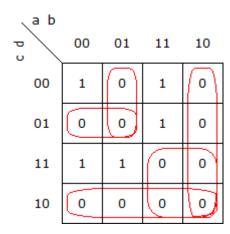
| а | b | С | d | f |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

Minimal SOP:



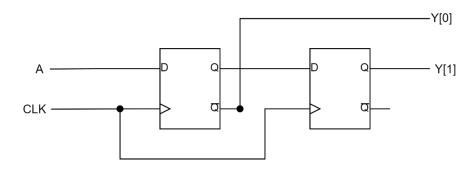
$$f = \bar{a}\bar{b}\bar{c}\bar{d} + ab\bar{c} + \bar{a}cd$$

Minimal POS:



$$f = (\bar{a} + b)(\bar{c} + d)(\bar{a} + \bar{c})(a + c + \bar{d})(a + \bar{b} + c)$$

Exercise 3 (4 points) Describe the following circuit using SystemVerilog:



Exercise 4 (3 points)

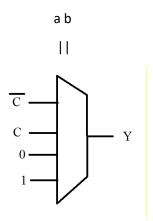
endmodule

A circuit receives the boolean inputs a, b, c, d and produces an output y such that:

y=1 if
$$a \cdot b = 1$$
 or $\bar{b} + \bar{c} = 0$ or $\bar{a}\bar{b}\bar{c} = 1$

- Write down the truth table
- Implement y with a 4-to-1 MUX using inputs a e b as control variables
- Draw the circuit corresponding to the NAND-NAND equation for the given circuit

| а | b | С | d | f |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

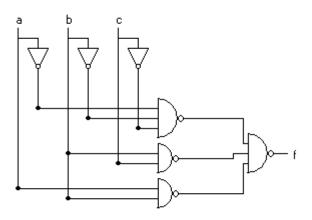


NAND-NAND:

Minimal POS: A'B'C' + BC + AB

NAND-NAND = ((A'B'C')' (BC)' (AB)')'

Circuit:



Exercise 5 (1+2+1 points)

Represent A= -3.25 using the IEEE half-precision floating point standard. Sum A and B (using the algorithm for summing IEEE floating point numbers), with B = 0100_0110_0100_0000 and represent the result as a IEEE half-precision floating point number. Last, represent the 16-bits of the result in hexadecimal format.

A = -3.25
$$\rightarrow$$
 -11.01₂ = -1*2¹*1.101₂
Sign = 1 (negative)
Exponent = 1
Exponent+bias = 1+15 = 16 = 10000₂
Mantissa = 1010000000
A = 1100_0010_1000_0000
B:
Sign = 0 (positive)
Exponent+bias = 10001₂ = 17
Exponent = 17-15 = 2

Mantissa =
$$1001000000_2$$

B = $1*2^2*1.1001_2 = 110.01_2 \rightarrow 6.25$

 $11.0011 + (x 2^2)$

 $01.1001 = (x 2^2)$

 $00.1100 (x 2^2)$

 $= 11.00_2 = 3_{10} = 1.100_2 \times 2^1$

Sign = 0 (positive)

Exponent = 1

Exponent+bias=1+15=16=100002

Mantissa=1000000000

IEEE Representation = 0100 0010 0000 0000 = 0x4200

Exercise 6 (5 points) Given the function

$$f = \bar{a}d \oplus (a\bar{b} + bc)$$

Represent it in POS form using Boolean algebra axiom, rules, and theorems.

$$f = (d\bar{a}) \oplus (a\bar{b} + bc) =$$

$$d\bar{a}(a\bar{b} + bc) + \bar{d}\bar{a}(a\bar{b} + bc) = d\bar{a} \cdot (\bar{a}\bar{b}) \cdot (\bar{b}c) + (\bar{d} + a)(a\bar{b} + bc) =$$

$$d \cdot \bar{a} \cdot (\bar{a} + b) \cdot (\bar{b} + \bar{c}) + (\bar{d} + a)(a\bar{b} + bc) =$$

$$d \cdot \bar{a} \cdot (\bar{b} + \bar{c}) + (\bar{d} + a)(a + b)(a + c)(\bar{b} + c) =$$

$$= (a + b + d)(a + c + d)(\bar{b} + c + d)(\bar{a} + \bar{b} + c)(a + \bar{b} + \bar{c} + \bar{d})$$