Exam - Computer Architecture Unit I [18/07/2023] (A)

Surname: _____ Name: _____

Student ID Number (Matricola): _____

Exercise 1 (7 points)

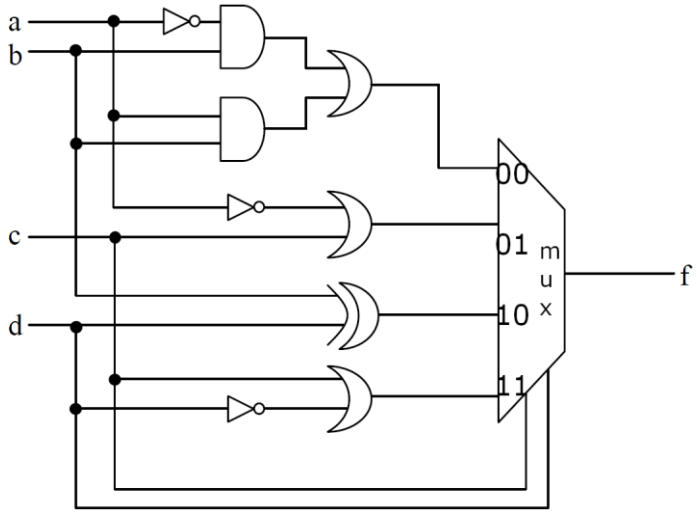
Design a sequential circuit with a binary input **x** and a binary output **y**. The output is equal to 1 if and only if the last three bits contain at least two 1s. Overlaps are allowed. Ignore the first two outputs (they can be any value). Show the transition diagram and draw the circuit.

Example:

```
INPUT:  01011001011100100
OUTPUT: --011100011110000
```

Exercise 2 (7 points)

Consider the following combinational circuit.



(a) Derive the Boolean expression of *f*. Then simplify it using Boolean theorems and axioms to minimal SOP form.
(b) Write down the truth table for *f.*
(c) Write down the minimal POS form for *f.*
(d) Implement *f* using only NOR and NOT ports.

Solution

(a) f = [(a'b)+(ab)](c'd') + (a'+ c)(c'd) + (b XOR d)(cd') + (c+d')(cd) =
= bc'd' + a'c'd + (b'd + bd')(cd') + cd =
= bc'd' + a'c'd + bcd' + cd =
= bd'(c'+c) + a'c'd + cd =
= bd' + a'c'd + cd =
= bd' + d(a'c' + c) =
= bd' + d(a' + c) =
= bd' + a'd + cd

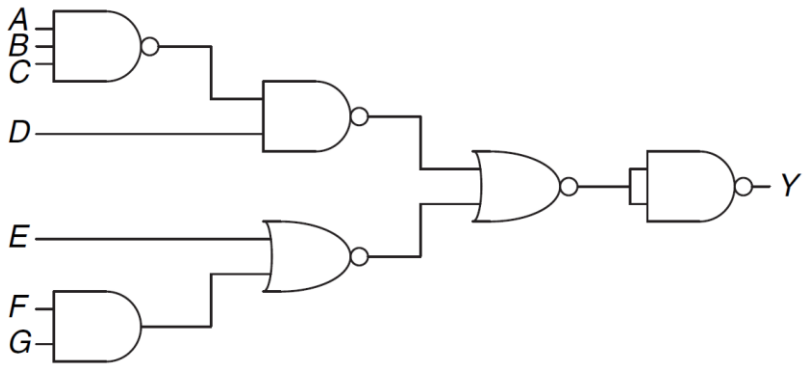
(b)

a	b	c	d	f
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

(c) Minimal POS: (b or d) and (c or ~a or ~d)

(d) ((b NOR d) NOR (c NOR ~a NOR ~d))

Exercise 3 (3 points)
Write a SystemVerilog module that implements the following circuit.



Solution

```
module ex4_17(input  logic a, b, c, d, e, f, g
              output logic y);

  logic n1, n2, n3, n4, n5;

  assign n1 = ~(a & b & c);
  assign n2 = ~(n1 & d);
  assign n3 = ~(f & g);
  assign n4 = ~(n3 | e);
  assign n5 = ~(n2 | n4);
  assign y = ~(n5 & n5);
endmodule
```

Exercise 4 (6 points)
a) Consider the hexadecimal numbers **F3B3** and **75DF.** Convert them into 16-bit binary sequences and interpret those sequences as two IEEE half-precision format numbers (**X** and **Y** respectively).
b) Compute X+Y and X-Y and write the results into IEEE half-precision format. If needed, round results to nearest.

Solution
(a) F3B3 -> 1111_0011_1011_0011
Sign = 1 (negative)
Biased Exponent = 11100 = 28
Exponent = 28 – 15 = 13
Mantissa = 1110110011
X = 1.1110110011 x 2^13

75DF -> 0111_0101_1101_1111
Sign = 0 (positive)
Biased Exponent = 11101 = 29
Exponent = 29 – 15 = 14
Mantissa = 0111011111
Y = 1.0111011111 x 2^14 = 10.111011111 x 2^13

(b) To compute X+Y, we observe that X is negative. We thus compute the difference between Y's and X' fractions.

```
10.1110111110 -
01.1110110011 =
---------------
01.0000001011 x 2^13
```

Because Y's fraction is larger than X's fraction, the sign of the result will be positive. So for X+Y we have:

Sign = 0 (positive)
Exponent = 11100
Fraction = 0000001011

To compute X-Y, both numbers will be negative, so we can just sum their fractions, and then consider a negative sign in the result.

```
01.1110110011 +
10.1110111110 =
---------------
100.1101110001 x 2^13 = 1.001101110001 x 2^15
```

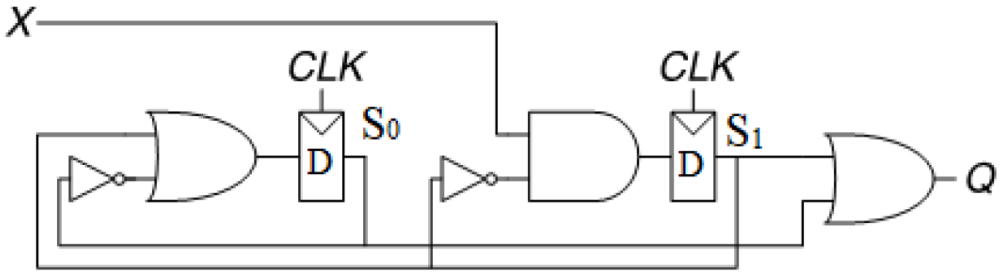
Thus we have:

Sign = 1 (negative)

Exponent = 15+15 = 30 = 11110
Fraction = 001101110001

This number would require 12 mantissa bits. We thus need to round to nearest fraction, which is:
Fraction = 0011011100

Exercise 5 (5 points)
Analyze the state machine shown in the figure. Write down next state and output tables and draw the state transition diagram.



Solution

S1	S0	x	S1'	S0'	Q
0	0	0	0	1	0
0	0	1	1	1	0
0	1	0	0	0	1
0	1	1	1	0	1
1	0	0	0	1	1
1	0	1	0	1	1
1	1	0	0	1	1
1	1	1	0	1	1

PS	x	NS	Q
S0	0	S1	0
S0	1	S3	0
S1	0	S0	1
S1	1	S2	1
S2	0	S1	1
S2	1	S1	1
S3	0	S1	1
S3	1	S1	1

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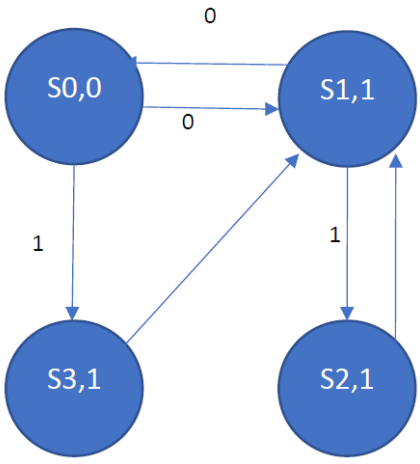

Exercise 6 (2 points)
Using Boolean algebra axioms and theorems simplify the following function to its minimal POS form.

$$(x + y)z + x\overline{yz}$$

Solution

$$(x + y)z + x\overline{yz} = xz + yz + x(\bar{y} + \bar{z}) = xz + yz + x\bar{y} + x\bar{z} = x + yz + x\bar{y} = x + yz = (x + y)(x + z)$$