Exam - Computer Architecture Unit I [04/06/2024] (A)

Surname: _____ Name: _____

Student ID Number (Matricola): _____

Exercise 1 (7 points) A sequential circuit has two inputs x1 and x0, and an output z. Consider the natural number composed by the last two bits of x1, followed by the last two bits of x0. If the division between that number and 3 has a reminder of 1, the output is equal to 1. Otherwise the output is equal to 0. Design the state transition diagram and the sequential circuit.
Overlaps are allowed. Ignore the first output (it can be set to any value).

Example:	INPUT:	x1	11001
		x0	00100
	Output:	z	-0001

Exercise 2 (4 points) Using Boolean's algebra axioms and theorems, verify the following equation:

$$\bar{a} \oplus b + \overline{(\bar{a}c + b)}(a + b)(a + c) = a + \bar{b}$$

Exercise 3 (4 points) Convert the base-10 number X=0.625 to IEEE 754 half-precision format. Then, consider the number Y=0x2200, interpret the resulting bits as an IEEE 754 half-precision number, and multiply it by X (in IEEE 754 representation).

Exercise 4 (6 points) The function f(a,b,c,d), is equal to 0 if:

- a(b $\oplus$ c)=1, or
- a+b+d=0

- Write down the truth table for f
- Write down the minimal SOP and POS forms for f
- Implement f using a MUX with 4 inputs
- Write down f in ALL-NAND form

Exercise 5 (5 points) Describe in SystemVerilog a RAM memory composed of 1024 memory locations, each on 8 bits.

Exercise 6 (4 points):

Consider this PLA and write down:

- The expressions for A and B
- The canonical SOP form for A+B
- The minimal POS form for A+B