Computer Architecture - Unit 2

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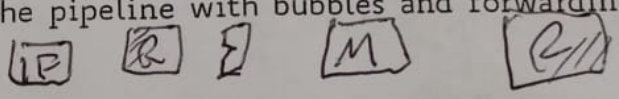
Exercise 1. How many clock cycles are needed to complete the following code on the Risc-V pipeline architecure? (Figure in the next page. Please note that the figure does not shows all the details of the architecture. Please consider the complete architecture. In case of doubt write your assumptions.) Remember that:

- Execution completes when the last instruction exits the pipeline.
- If you read and write the same register of the register file in the same clock cycle, the value that is read is the value that is being witten.

Show a figure of the pipeline with bubbles and forwardings.




```
add s1, s0, s0
lw s2, 8(s3)
add s2, s1, s3
sw s2, 12(s7)
lw s7, 0(s1)
add s7, s2, s2
sub s3, s7, s0
lw s5,4(s3)
add a0, a0, s5
```

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Figure drawn on the back

Exercise 2. Consider the following code:

```
.data
v:      .word 10,-1,-72,45,2,...    # array of 16368 integers
w:      .word 8,9,-7,-4,25,...      # array of 16368 integers
n:      .word 16384 # This is 2^16

.text
        lui s0, 0x10030
        lw s2, 0(s0)
        lui s0, 0x10010
        lui s1, 0x10020
        mov a0, zero
loop:   lw t0, 0(s0)
        add a0, a0, t0
        lw t0, 0(s1)
        add a0, a0, t0
        addi s0, s0, 4
        addi s1, s1, 4
        addi s2, s2, -1
        bne s2, zero, loop
        li a7, 1
        ecall
        li a7, 10
        ecall
```

This program adds all the values in two arrays of the same length.

1. **Question A:** Assume the single clock architecture. What is the approximate total miss rate if you have two one-way associative caches with 8 blocks of 64 bytes, one for instructions and the other one for data?

2. **Question B:** What is the speed-up (how faster is it) if we use the Risc-V multiple issue architecture with loop unrolling of 4 loops instead of the standard pipelined architecure? Show the code.

Exercise 3. In the eerie depths of Rome, a chilling encounter unfolded. It involved a professor of Computer Architecture and the enigmatic figure known as Uncle Jack. The air crackled with a palpable tension as the professor unveiled the draft of the final test for the dreaded Computer Architecture Unit 2. "Too easy," Uncle Jack scoffed, his voice a mere echo in the night. "And, by the way," he continued, his voice dripping with an unsettling blend of knowledge and foreboding. "No one with basic knowledge of caches would have written the code of Exercise 2 that way."

This is probably true. Can you rewrite the loop of Exercise 2 in a more cache friendly way? Choose the best cache system possible that uses approximately the same amount of memory of the two caches of Exercise 2 combined (max block size 128 bytes), show the cache friendly code, and compute the approximate miss rate in this new setting.