Exam - Computer Architecture Unit I [05/04/2024] (A)

Surname: _____ Name: _____

Student ID Number (Matricola): _____

Exercise 1 (7 points)

Design a finite state machine with two inputs x and y. Being x(t) and x(t-1) the bits received in the last two cycles for the input x, and y(t) and y(t-1) the bits received in the last two cycles for the input y, the FSM produces the output z1 and z0, so that:

- z1(t) is the XOR between x(t), x(t-1), y(t), y(t-1)
- z0(t)=1 if the pairs x(t)x(t-1) and y(t)y(t-1) are equal, or if one is the complement of the other.

Draw the sequential circuit.

Example:

Input x: 00011101101101
y: 00101000010111
Output z1: -0101111000111
z0: -1010000111000

Exercise 2 (6 points): Being A = a1a0 and B = b1b0 two binary numbers on 2 bits each. Design a circuit with the 4 bits {a1, a0, b1, b0} as input, and which produces an output Y = A – 2*B. Y is a 2-complement number on 3 bits {y2, y1, y0}. If Y can't be represented, use don't cares.

- Design the circuit using a ROM
- Design the circuit using a PLA
- Implement y1 using only NAND gates

Exercise 3 (3 points) Prove, using Boolean's algebra axiom, the following equation:

$$\bar{a}\bar{b}\bar{c} + a + b + c = 1$$

Important: Name at least one of the axiom/theorems used

Exercise 4 (3 points) Design a 4:1 multiplexer using 4 tri-state buffers and the necessary AND/OR/NOT gates

Exercise 5 (5 points) Consider the following boolean expression

$$f = \left(\bar{a} + \overline{b(b + \overline{\overline{cde}})}\right) \oplus (\bar{a} + cd)$$

1. Derive the normal SOP form
2. Derive the minimal POS form
3. Derive the ALL-NOR form

Exercise 6 (6 points)

- Convert the base-10 number X=9,375 to base-2 fixed point notation.
- Then, convert it to IEEE 754 half precision format.
- Consider the hexadecimal number Y=0xBE00. Consideri ita s a IEEE 754 half precision number and compute Z=X-Y.