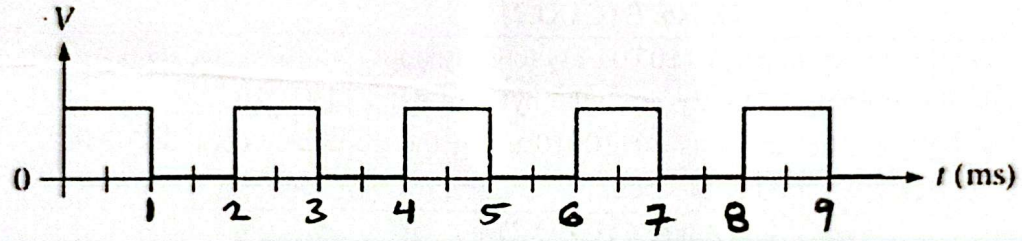
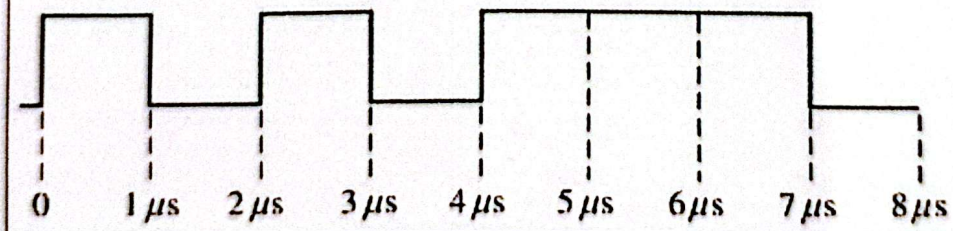
Air University
(Mid-Term Examination: Spring 2024)

Subject:	Digital Logic Design	Total Marks:	100
Course Code:	EE-123	Date:	6th April, 2024
Class:	BS-CYS	Time:	11:00-13:00
Semester:	II	Duration:	2 Hours
Section:	A & B	FM Name:	Dr. Bahman R. Alyaei

HoD Signatures: _____ FM Signatures: _____

Note:

- **This is closed book exam, All questions must be attempted.**
- **This examination carries 25% weight towards the final grade.**
- **Calculators are not allowed**

	Q. No. 1 (CLO 1)	15 Marks
a	For the periodic signal shown in the figure below, **determine** the following: **(i)** The period of the signal. **(ii)** The frequency. **(iii)** The duty cycle. 	5
b	For the signal shown in the figure below, **determine** the following: **(i)** The bit duration. **(ii)** The transmission or the bit rate. **(iii)** What is the total serial transfer time for the eight bits? **(iv)** What is the total parallel transfer time? 	10
	Q. No. 2 (CLO 1)	**25 Marks**
b	**Convert** the decimal number $(821)_{10}$ to (i) Binary number (ii) Hexadecimal number (iii) BCD number	5+5+5=15
c	**Convert** the binary number $(10101010)_2$ to (i) Decimal number (ii) Hexadecimal number	2.5+2.5=5
d	**Convert** the Hexadecimal number $(F2A)_{16}$ to (i) Decimal number.	2.5+2.5=5

	(ii) Binary number.	
	Q. No. 3 (CLO 1)	**20 Marks**
a	**Evaluate** the following unsigned numbers addition and subtraction, assume a 4 bit register size (i) 101 + 110 (ii) 100 – 011	5+5
b	**Evaluate** the following unsigned numbers multiplication and division, assume a 6 bit register size (i) 101 × 110 (ii) 110 ÷ 011	5+5
	Q. No. 4 (CLO 1)	**15 Marks**
a	**Express** the decimal number $(-31)_{10}$ using 8-bit word using the following sign-number system: (i) Sign-Magnitude form. (ii) 1's complement form. (iii) 2's complement form.	3+3+3=9
b	**Evaluate** the following signed numbers addition and subtraction, assume a 4 bit register size (i) 1010 + 1001 (ii) 0111 - 1010	3+3=6
	Q. No. 5 (CLO 2)	**15 Marks**
a	(i) **Convert** the binary code $(10101011)_2$ to Gray code. (ii) **Attach** the proper even parity bit to the bytes of data, $(10101011)_2$. (iii) **Apply** CRC to the data bits 10110010 using the generator code 1010 to produce the transmitted CRC code.	5+5+5
	Q. No. 6 (CLO 2)	**10 Marks**
a	**Evaluate** the truth table of the following logic gates: (i) NAND Gate. (ii) XOR Gate. (iii)OR Gate. (iv)NOT Gate. (v) AND Gate	10

********** End of Question Paper **********