Microelectronics Reliability xxx (2012) xxx–xxx

Contents lists available at SciVerse ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Introductory Invited Paper

Revisiting MOSFET threshold voltage extraction methods

Adelmo Ortiz-Conde [a,*], Francisco J. García-Sánchez [a], Juan Muci [a], Alberto Terán Barrios [a], Juin J. Liou [b,c], Ching-Sung Ho [d]

[a] Solid State Electronics Laboratory, Universidad Simón Bolívar, Caracas 1080A, Venezuela
[b] Department of Electrical and Computer Engineering, University of Central Florida, Orlando, FL 32816-2450, USA
[c] Department of ISEE, Zhejiang University, Hangzhou, China
[d] Powerchip Technology Corp., Hsinchu Science-Based Industrial Park, Hsinchu, Taiwan

A R T I C L E I N F O

Article history:
Received 26 September 2012
Accepted 26 September 2012
Available online xxxx

A B S T R A C T

This article presents an up-to-date review of the several extraction methods commonly used to determine the value of the threshold voltage of MOSFETs. It includes the different methods that extract this quantity from the drain current versus gate voltage transfer characteristics measured under linear operation conditions for crystalline and non-crystalline MOSFETs. The various methods presented for the *linear region* are adapted to the *saturation region* and tested as a function of drain voltage whenever possible. The implementation of the extraction methods is discussed and tested by applying them to real state-of-the-art devices in order to compare their performance. The validity of the different methods with respect to the presence of parasitic series resistance is also evaluated using 2-D simulations.

1. Introduction

The threshold voltage (V_T) is perhaps the most descriptive aspect of MOSFET operation [1–6]. It is generally understood simply as the gate voltage (V_G) at which significant drain current starts to flow. In traditional MOSFET models V_T was phenomenologically viewed as the gate voltage that drives the channel into strong charge inversion conditions [7]. This historical description was qualitatively related to the particular channel band-bending condition where the surface potential becomes approximately equal to twice the bulk Fermi potential. Such definition, although simple, is not always adequate for many modern MOSFETs, including such types as undoped channel multi-gate MOSFETs [5], junctionless transistors [8], tunnel P–I–N FETs [9], ion sensitive FETs [10], nanowire FETs [11], and non-crystalline TFTs [12,13]. Therefore, it is better to consider an operational concept of threshold, which applies in a more general sense to a wider range of devices, and can be functionally described simply as the value of V_G needed for the transition from weak to strong source–drain conduction to take place in the MOSFET's channel.

The successful fabrication of the first MOSFET in 1960 [14] motivated the fast developments of MOSFET's models. In 1961, Ihantola developed the first MOSFET model based on threshold voltage [15]. That model inspired during various decades the development of many MOSFET models, all based on threshold voltage, for SPICE simulation, such as Level = 1, 2, 3 and BSIM [16]. On the other hand, Pao and Sah proposed the first surface potential model, which was based on a double-integration [17]. Pao and Sah's model constitutes the basis of present day compact models [18,19]. It also inspired Brews [20] and Baccarani et al. [21] to independently develop charge-sheet models.

Traditional MOSFET models relied on accurately establishing the value of V_T because their regional nature entailed defining separate equations for the current, valid either below or above threshold. Therefore, the exact definition of V_T and the subsequent extraction of its value constituted pillars of traditional regional MOSFET modeling. However, with the arrival and present prevalence of modern non-regional MOSFET models, where this parameter is not explicitly present, the significance of the V_T concept for modeling purposes *per se* has declined considerably.

Notwithstanding the absence of V_T as an explicit parameter from most modern MOSFET models, knowledge of its value remains a very useful asset for several important and practical reasons. Not only V_T still is the essential quantity to consider in most MOSFET circuit design metrics, but also serves as the most effective quality control indicator when evaluating device reliability [22,23]. Threshold voltage is often used for assessing and predicting device performance variability due to manufacturing processes technological parameter fluctuations, such as gate length, channel thickness, doping and equivalent oxide thickness [24], as well as other operation reliability factors, such as radiation damage, hot-carrier stressing, temperature instability and aging degradation [25–27]. The persistent usefulness of being able to determine the value of V_T for device and circuit design, analysis,

* Corresponding author.
E-mail addresses: ortizc@ieee.org (A. Ortiz-Conde), fgarcia@ieee.org (F.J. García-Sánchez), liou@eecs.ucf.edu (J.J. Liou), chingho@powerchip.com (C.-S. Ho).

0026-2714/$ - see front matter © 2012 Elsevier Ltd. All rights reserved.
http://dx.doi.org/10.1016/j.microrel.2012.09.015

and reliability assessment, still provokes enormous interest today, especially regarding the extraction methods to be used for its reliable measurement.

Several books and articles [1–6,28–31] have reviewed over time the different V_T definitions and methods available for its extraction. Many definitions have been proposed [32–35] and there exist numerous extraction methods [36–81]. Some extraction circuits have been also proposed [33,82–84] to automatically measure V_T. For the most part the procedures available to determine V_T are based on the measurement of the static transfer (I_D–V_G) characteristics [36–47,49–51,53–58,61–73], of a single transistor. Most of these I_D–V_G methods rely on extracting V_T from the strong inversion region [37,38,41,43,46,47,49,51,53,54,57,58,64,70,77], while only a few consider the weak inversion region [39,40,55]. Extraction is mostly performed at low drain voltages so that the device operates in the linear region [36–41,43,45–47,49–51,53–58,64]. However, V_T extraction with the device operating in saturation is also frequently done for digital circuit applications [61,62].

A frequent concern regarding V_T extraction methods based on the transfer characteristics is the strong dependence of the resulting value of the extracted V_T on source and drain parasitic series resistances and channel mobility degradation [78]. This dependence is highly detrimental to unequivocal extraction, because for the V_T value to be unambiguous it should only depend on intrinsic parameters. Some methods propose measuring capacitance as a function of voltage to eliminate the influence of these unwanted effects [52,60,85]. Such C–V methods require measuring very small capacitances, particularly in present day small geometry MOSFETs, and thus require elaborate set-ups and sophisticated equipment. Some approaches to remove the influence of parasitic series resistances involve either measuring the transfer characteristics of a number of devices with various mask channel lengths [42,59], or measuring several devices connected together [44,48]. Such multi-device approaches are useful to solve this problem, but they call for additional work and the availability of supplementary devices specifically manufactured for this purpose. Another method proposes repeated measurements and the use of a proportional difference operator to meet this challenge [57,58]. Others propose using S-parameter measurements to determine the V_T of microwave MOSFETs [74].

Considering that non-crystalline MOSFETs exhibit much smaller currents than their mono-crystalline counterparts, extraction of V_T in these devices is best carried out in the saturation region. Amorphous and polycrystalline thin film transistors (TFTs) present an additional difficulty: their saturation drain current in strong inversion is described by a power-law type function of the gate voltage with an exponent usually different from 2 [75,86]. Therefore, the use of the same V_T extraction methods as conventionally utilized for mono-crystalline devices will normally yield inaccurate or unrealistic values. Therefore V_T extraction methods for non-crystalline MOSFETs must also be capable of extracting the value of the unknown power-law exponent parameter, to enable its use in the V_T extraction procedure. Some methods have been put forward specifically for the task of extracting the correct value of V_T in non-crystalline thin MOSFET TFTs [75,86].

In the following section we will review available methods for extracting V_T from the I_D–V_G transfer characteristics in mono-crystalline MOSFETs, biased in the *linear region*. The following methods will be examined: (1) Constant Current (CC) method, which defines V_T as the gate voltage corresponding to a certain predefined practical constant drain current [1,2,4,6,54,64,71,79]; (2) Match-Point (MP) method, which defines V_T as the gate voltage at a pre-established deviation percentage of the drain current from its extrapolated weak inversion conduction behavior [39]; (3) Linear Extrapolation (LE) method, which defines V_T as the gate voltage axis intercept of the tangent of the I_D–V_G characteristics at its maximum first derivative (slope) point, [1,2,4,6,80,81,87]; (4) Second Derivative (SD) method, which defines V_T as the gate voltage at the maximum of the second derivative of the I_D–V_G characteristics [36]; (5) Third-derivative (TD) method which defines V_T as the gate voltage at the maximum of the third derivative of the I_D–V_G characteristics, in contradiction to the SD method [63]; (6) Current-to-square-root-of-the-Transconductance Ratio (CsrTR) method, which defines V_T as the gate voltage axis intercept of the ratio of the drain current to the square root of the transconductance [37,38,46,70,77]; (7) Transition method which defines V_T at the transition between weak and strong conduction behaviors [56], inspired on the integral difference function D [88,89]; (8) Normalized Mutual Integral Difference Method (NMID), also an integration-based method following the ideas of the previous one [65]; (9) Normalized Reciprocal H function (NRH) method, which is an improvement to the NMID method; and (10) Transconductance-to-Current-Ratio (TCR) [31,45,68,72,73], and its integration-based counterpart the Reciprocal H function (RH) method [69]. These methods, intended for use at small drain voltages in the *linear* operation *regime*, will be will tested, whenever possible, for higher drain voltages up to and including the *saturation region*.

In addition to presenting an updated review of the above mentioned methods, the following new aspects have been included: (a) an improvement to the CsrTR method, based on the Lambert W function, which is valid from weak to strong inversion; (b) a noise reduction technique for the SD method, based on nonlinear optimization; and (c) a new method, denoted Normalized Reciprocal H function method, which is a combination of previous integral methods. In Section 3, 2-D simulations, using the "MOSFet" simulation tool [90], are carried out to ascertain the effect of the presence of parasitic series resistance and of high drain voltages on the various methods.

Finally, Section 4 reviews and discusses some non-crystalline device specific integration-based procedures [75,86,91], recently proposed to extract their threshold voltage. These integration-based methods for parameter extraction in two-terminal devices were originally reviewed in 2008 in two articles [92,93].

2. Extraction from measured I_D–V_G characteristics

The several linear region extraction methods reviewed here will be later applied to extract the value of V_T from the measured transfer characteristics of a state-of-the art enhancement-mode n-channel bulk mono-crystalline silicon MOSFET, in order to critically assess and compare them. The device, with a 70 nm mask channel length, a 2.6 nm gate oxide thickness, and a 5 μm mask channel width, will be used throughout this review for this purpose. It will be biased both in the linear region, by applying a drain voltage of 10 mV, and in the saturation region, by applying a drain voltage of 1.1 V. Fig. 1 presents the measured output characteristics of this test MOSFET as a general illustration of its overall behavior.

2.1. Constant-current (CC) method

The constant-current (CC) method [1–4,6,53,71,79] is widely used in industry because of its simplicity. It evaluates V_T as the value of the V_G corresponding to a predetermined, more or less arbitrary, constant drain current, I_D and $V_D < 100$ mV. Tsuno et al. proposed [53] that this constant drain current be $(W_m/L_m) \times 10^{-7}$, where W_m and L_m are the mask channel width and length, respectively. Recently, Bazigos and coworkers proposed [71] that the constant drain current should be dependent on drain voltage, V_D, in order to obtain a consistent V_T value in the saturations region. For the particular device used for illustration here with $V_D = 10$ mV, this constant drain current should be 2 μA, according to Bazigos's

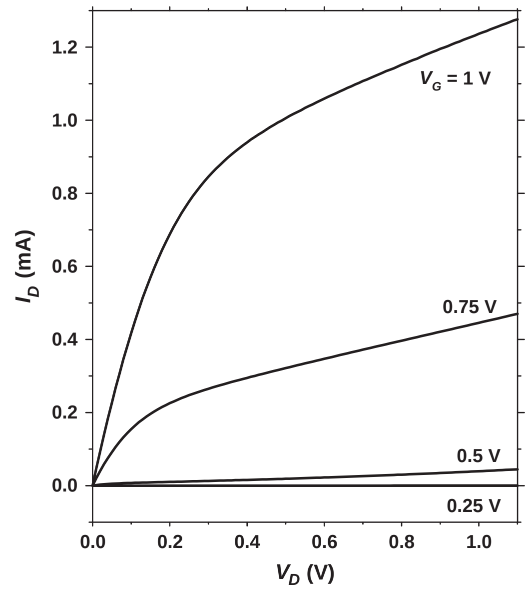

Fig. 1. Measured I_D–V_D output characteristics at four values of gate bias for the test bulk single-crystal n-channel MOSFET with 70 nm mask channel length, 2.6 nm gate oxide thickness, and 5 μm mask channel width.

formulation [71], and 7 μA according to Tsuno's formula [53]. The threshold voltage can be determined quickly with only one measurement, as shown in Fig. 2. We have selected here a value of 5 μA merely for illustrative purposes.

In spite of the obvious advantage that its simplicity offers, this method has the serious disadvantage of being totally dependent of the value of the drain current chosen to define threshold. Thus, the outcome depends on this choice, and inconsistent results for the value of V_T are likely to occur. This is evident observing the results shown in Fig. 2, where different gate voltages are taken at different I_D levels to represent V_T. To overcome this ambiguity, Zhou and his group have proposed [54,64] an improvement to the CC method. It consists on defining the I_D level chosen to define the V_T at the I_D value where d^2I_D/dV_G^2 has a maximum. This amounts to combining the CC method with the second-derivative of I_D method, to be presented latter. Bazigos and coworkers also have recently proposed to combine the CC method with other methods in order circumvent the ambiguity in defining the drain current level [71].

In order to extract the threshold voltage from the saturation region the device is biased at a V_D = 1.1 V. Fig. 3 shows the square root of the drain current as a function of V_G. The constant current method, according to Bazigos et al. [71], requires that the constant current be dependent on the drain voltage. In the present case, the constant current should be increased by a factor of 4, which implies that I_D = 20 μA defines a V_T = 0.45 V.

As already mentioned, the CC method is an attractive method for industrial applications because V_T can be determined quickly with only one voltage measurement. However, since it is highly dependent on arbitrary choice, inconsistent values of V_T may be obtained depending on the different constant I_D values chosen.

Instead of applying conventional data smoothing to reduce the possible uncertainties arising from measurement noise, an alternative is to use some appropriate model to be fitted to the measured data to serve the same purpose. For instance, semi-empirical transfer characteristics model equations similar to those proposed in [94] could be used in the linear region from weak to strong inversion.

Semi-empirical Lambert W function-based models inspired on the hypothetically undoped bulk MOSFET solution [95], could be useful for this task. Such solutions describe the drain current by an exponential behavior in weak conduction and asymptotically approaching a linear behavior in strong inversion. Following such a semi-empirical description, the current may be approximately described by the following equation:

$$I_D = \frac{I_o}{(1+\theta V_G)} W_0 \left[K(1+\theta V_G) e^{\frac{\beta V_G}{n}} \right], \tag{1}$$

where W_0 represents the principal branch of the Lambert W function, I_o and K are constants, n is the ideality factor in the sub-threshold regime, θ is a mobility degradation coefficient, and $\beta = 1/v_{th}$ is the inverse of the thermal voltage. The following lateral optimiza-

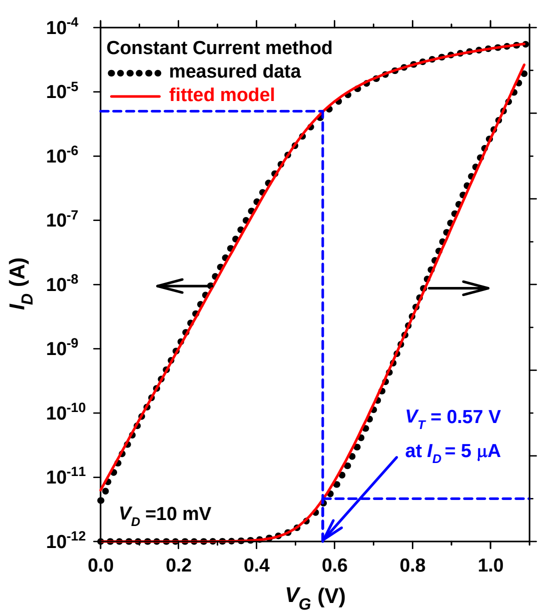

Fig. 2. Constant-current (CC) method implemented on the I_D–V_G transfer characteristics of the test device measured at V_D = 10 mV. V_T is extracted as the value of V_G corresponding to a predetermined constant I_D of 5 μA. A semi empirical model (solid lines) described by Eqs. (1) and (2), as fitted to the measured data (symbols), is also included.

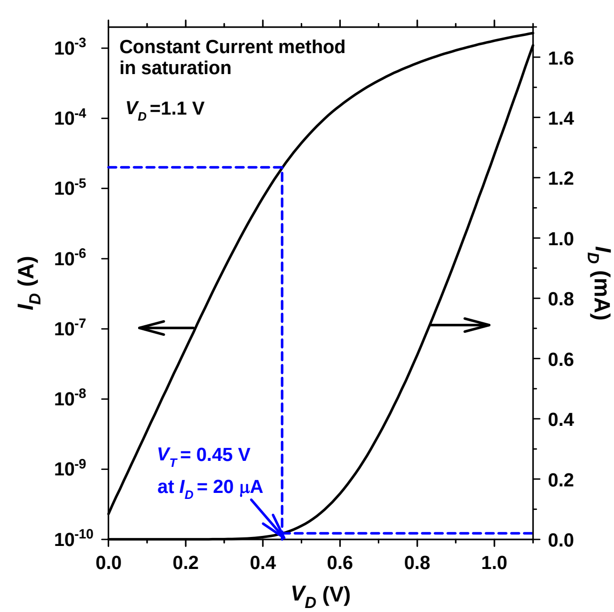

Fig. 3. Constant-current (CC) method implemented on the I_D–V_G transfer characteristics of the test device measured at V_D = 1.1 V. This method evaluates V_T as the value of V_G corresponding to a constant drain current of 20 μA.

Please cite this article in press as: Ortiz-Conde A et al. Revisiting MOSFET threshold voltage extraction methods. Microelectron Reliab (2012), http://dx.doi.org/10.1016/j.microrel.2012.09.015

tion procedure [96] of V_G versus I_D can be used for fitting it to measured data for noise reduction purposes:

$$V_G = \frac{n v_{th} \ln(I_D) + (\frac{n v_{th}}{I_o}) I_D - n v_{th} \ln(K I_o)}{1 - (\frac{n v_{th} \theta}{I_o}) I_D}. \quad (2)$$

Once this semi-empirical equation's parameters are extracted from the lateral optimization fitting procedure, the above equation can be directly evaluated at the previously chosen constant I_D value to immediately obtain the corresponding value of V_T, in this case using the CC method. This same semi-empirical model (1) will be used in the following sections with various other V_T extraction methods for the same purpose.

2.2. Match-Point (MP) method

A seldom used method, proposed in 1990, is the so-called Match-Point (MP) method [39]. This method arbitrarily establishes V_T at the value of V_G at which the exponential sub-threshold current semi-log extrapolation deviates by 5% from the measured I_D. This method overemphasizes the weak inversion region neglecting strong inversion. Fig. 4 presents the application of this method to the linear region of our test device producing an apparent V_T value of only 0.35 V. Fig. 5 illustrates the application of this method also to the saturation region producing an apparent V_T value of only 0.31 V. Of course, different values of V_T could be arbitrarily obtained by defining the deviation of the extrapolation at threshold at other values different from 5%.

2.3. Linear Extrapolation (LE) method

The Linear Extrapolation (LE) method in the linear region, often referred to as the extrapolated V_T, is perhaps the most widely used method for extracting V_T. It consists of finding the V_G axis intercept (i.e., $I_D = 0$) of the linear extrapolation of the I_D–V_G curve at its maximum first derivative (slope) point (i.e. the point of maximum transconductance, g_m) [1,4,6,80,81,87]. It is illustrated in Fig. 6 for the presently used test device. The value of V_T is calculated by adding $V_D/2$ to the resulting V_G axis intercept, which for this device happens to be $V_T = 0.57$ V. The main drawback of this traditional method is that the maximum slope point is actually

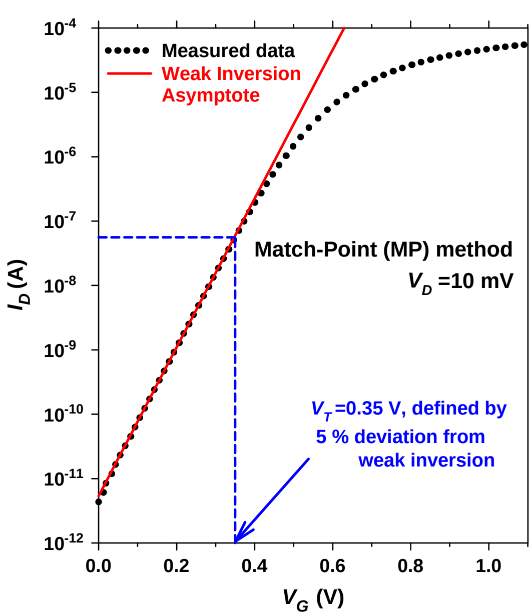

Fig. 4. Match-Point (MP) method implemented on the test bulk device measured at $V_D = 10$ mV.

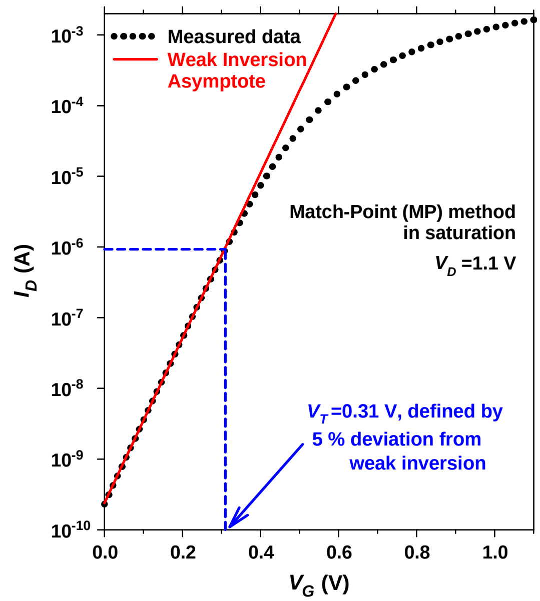

Fig. 5. Match-Point (MP) method implemented on the test bulk device measured at $V_D = 1.1$ V.

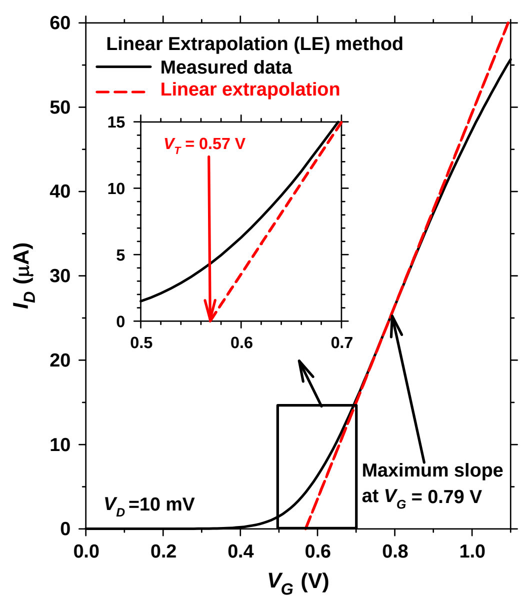

Fig. 6. Extrapolation in the Linear Region method (ELR) implemented on the I_D–V_G characteristics of the test bulk device, measured at $V_D = 10$ mV. This method finds V_T at the V_G axis intercept (i.e., $I_D = 0$) of the Linear Extrapolation of the I_D–V_G curve at its maximum slope point.

determined by mobility degradation and the presence of source and drain series parasitic resistances, when they are significant [3]. Therefore, the V_T value extracted using this method, can be strongly influenced by parasitic series resistances and mobility degradation effects.

The Linear Extrapolation method can be used in the saturation region, using the $I_D^{0.5} - V_G$ characteristics [1,6] as illustrated in Fig. 7. The value of V_T calculated for the present device results to be 0.41 V.

2.4. Second-Derivative (SD) method

The second-derivative method (SD), originally called transconductance change method [36], is one of the most popular threshold-

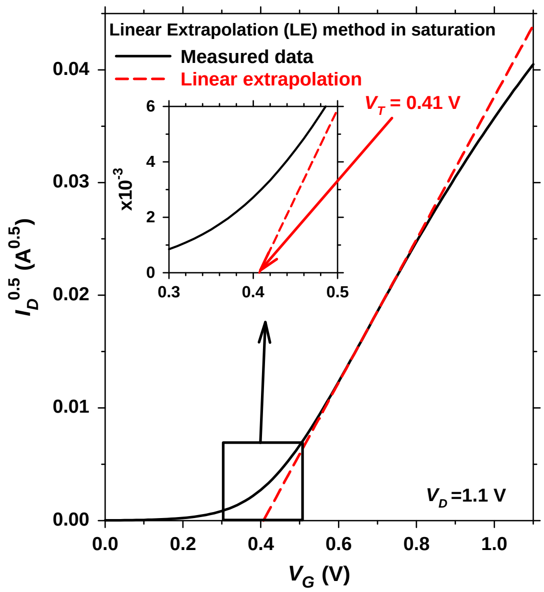

Fig. 7. Linear Extrapolation (LE) method in the saturation region implemented on the test bulk device $I_D^{0.5}-V_G$ characteristics at V_D = 1.1 V. This method finds V_T as the V_G axis intercept (i.e., $I_D^{0.5}=0$) of the Linear Extrapolation of the $I_D^{0.5}-V_G$ curve at its maximum slope point.

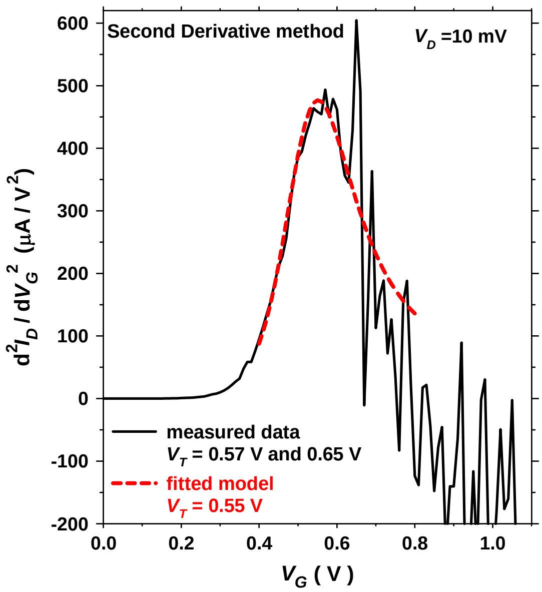

Fig. 8. Second-derivative method (SD) implemented on the test device, measured at V_D = 10 mV. This method finds V_T at the V_G value where d^2I_D/dV_G^2 has a maximum. The second derivatives of I_D for both the original data (solid line) and the fitted semi-empirical model (dashed line), as described by (1), are shown.

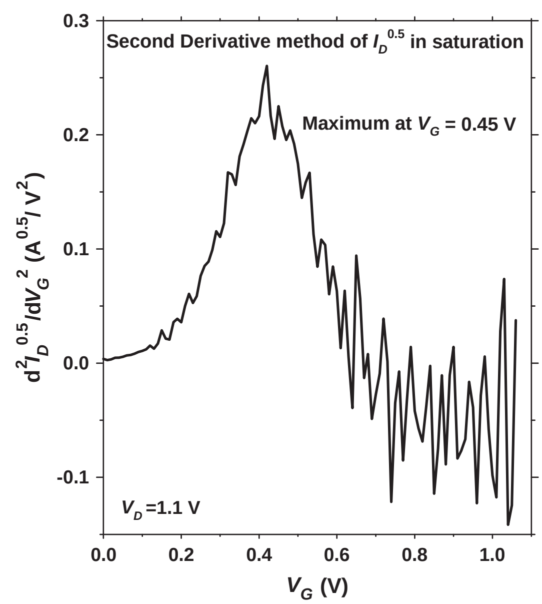

Fig. 9. Second-derivative method (SD) in saturation implemented on the test device, measured at V_D = 1.1 V. This method finds V_T at the V_G value where $d^2I_D^{0.5}/dV_G^2$ has a maximum.

voltage extraction methods. It was developed to avoid dependence on series resistances. It determines V_T as the V_G value at which the derivative of the transconductance (i.e., $dg_m/dV_G = d^2I_D/dV_G^2$) is a maximum. Its origin can be understood by the ideal case of a simple Level = 1 MOSFET SPICE model, where I_D = 0 for $V_G < V_T$, and I_D is directly proportional to V_G for $V_G > V_T$. With these assumption, dI_D/dV_G becomes a step function, which is zero for $V_G < V_T$ and is a positive constant for $V_G > V_T$. Therefore, d^2I_D/dV_G^2 will go to infinity exactly at $V_G = V_T$. Such a simple assumption is obviously not true in a real device, and thus d^2I_D/dV_G^2 will not become infinite at V_T. However, it will exhibit a maximum value at $V_G = V_T$.

The implementation of this method in the linear region is highly sensitive to measurement error and noise, because the second derivative amounts to applying a high-pass filter to the measurement. Notice that in the curve of Fig. 8 there are two apparent local maxima of d^2I_D/dV_G^2 at about V_G = 0.57 V and 0.65 V, because of the presence of measurement noise.

Measurement noise can be reduced, before taking the derivatives, by conventional numerical smoothing techniques [97] or by fitting the already mentioned semi-empiric model described in (1) and (2) to the measured data. Fig. 8 also presents the results of the second derivative after applying the semi-empiric model for the range of V_G = 0.4–0.8 V. With this approach the maximum is unique and smooth and appears to be around a value of V_G = 0.55 V.

Following the same ideas presented in Section 2.3, we could also extract the threshold voltage using the second-derivative method (SD) in the saturation region. Fig. 9 shows $d^2I_D^{0.5}/dV_G^2$ versus V_G for the saturation region with V_D = 1.1 V. We observe that the maximum value of this curve occurs at about V_G = 0.45 V. Semi-empiric model fitting could also be used in this case for data smoothing.

2.5. Third-Derivative (TD) method

It has been suggested that V_T could be extracted from the value of V_G at which the third derivative of the current (i.e., d^3I_D/dV_G^3) has a maximum [63]. However, the maximum and minimum of the third derivative always fall to the left and right of the second derivative maximum, which is located at $d^3I_D/dV_G^3=0$. Fig. 10, which for generality was synthetically generated using the empirical Eq. (1), clearly illustrates this fact. Therefore, the third derivative method is obviously incompatible with the widely used second derivative method.

Figs. 11 and 12 present the application of this method to the experimental test device in the linear and saturation regions, at drain voltages of 10 mV and 1.1 V, respectively. It is clear from these figures that the TD method is seriously affected by experimental noisy data. Although measurement noise could be reduced by numerical smoothing techniques [97] or by fitting the semi-empiric model previously described, as shown in Fig. 11, the extracted V_T value would still be incompatible with that extracted by the SD method.

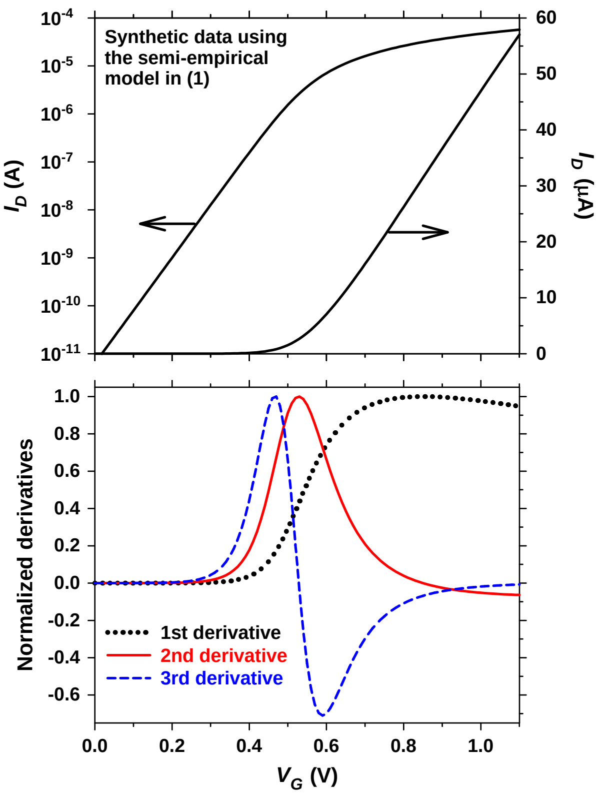

Fig. 10. (Upper pane) Synthetic I_D–V_G characteristics generated with the empirical Eq. (1). (Lower pane) Normalized first, second and third derivatives of the I_D–V_G characteristics.

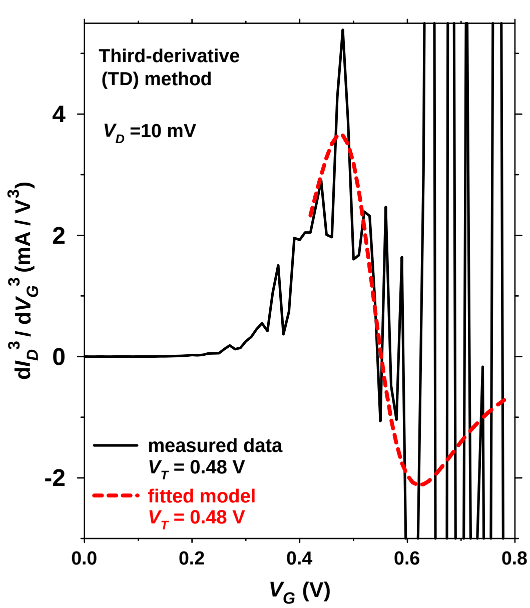

Fig. 11. Third-derivative (TD) method applied to the test bulk device in the linear region at V_D = 10 mV. The third derivatives of I_D for both the original data (solid line) and the fitted semi-empirical model (dashed line), as described by (1), are shown.

2.6. Current-to-square-root-of-the-Transconductance Ratio (CsrTR) method

The CsrTR method was developed to avoid the extracted V_T value dependence on mobility degradation and parasitic series resistance [37,38,46,70,77]. The ratio of the drain current to the square root of the transconductance, $(I_D/g_m^{0.5})$, in the linear region, is given by:

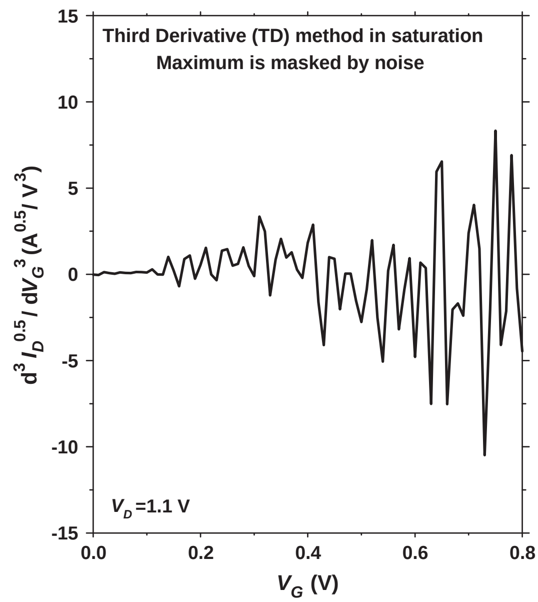

Fig. 12. Third-derivative (TD) method applied to the test bulk device in the saturation region at V_D = 1.1 V.

$$CsrTR \equiv \frac{I_D}{\sqrt{g_m}} \equiv \frac{I_D}{\sqrt{\frac{dI_D}{dV_G}}} = s^{-1/2}(V_G - V_T), \tag{3}$$

where s is a constant.

This method was originally published independently in 1988 by Jain [38] and by Ghibaudo [37]. Jain demonstrated that if the mobility degradation were negligible, the function $I_D/g_m^{0.5}$ would be independent of parasitic series resistance [38]. On the other hand, Ghibaudo showed that if the parasitic series resistance were negligible, the function $I_D/g_m^{0.5}$ would not depend on mobility degradation [37]. In 1995, Fikry and coworkers [46] proved that the function $I_D/g_m^{0.5}$ is independent of mobility degradation, parasitic series resistance and velocity saturation effects. The CsrTR method, sometimes called "the modified Y function method," has been recently improved [70,77] for application to modern devices using a more general mobility degradation model.

The values of V_T and s can be extracted from the intercept and the slope of the CsrTR versus V_G linear fit. Fig. 13 shows the results of applying this method to the present test device in the linear region. As can be observed, it is not very clear in the present case from where to linearly extrapolate to find the V_G axis intercept. It seems that the presently used test device's $I_D/g_m^{1/2}$ versus V_G curve does not adequately fulfill this method's assumptions, since it does not clearly show the supposedly expected linear behavior. Therefore, the linear extrapolation shown in Fig. 13 is only a guess, amidst the evident non-linearity present.

The CsrTR method can be significantly improved by using the semi-empirical Eq. (1) to obtain a CsrTR function valid from weak to strong inversion. For simplicity, and assuming that the CsrTR function eliminates mobility degradation, we use Eq. (1) with $\theta = 0$. Then the CsrTR is:

$$CsrTR \equiv \frac{I_D}{g_m^{1/2}} = \sqrt{n v_{th} I_o W\left(Ke^{\frac{\beta V_G}{n}}\right)\left[1 + W_0\left(Ke^{\frac{\beta V_G}{n}}\right)\right]}. \tag{4}$$

The above equation can be analytically solved for V_G so as to perform a lateral fitting optimization:

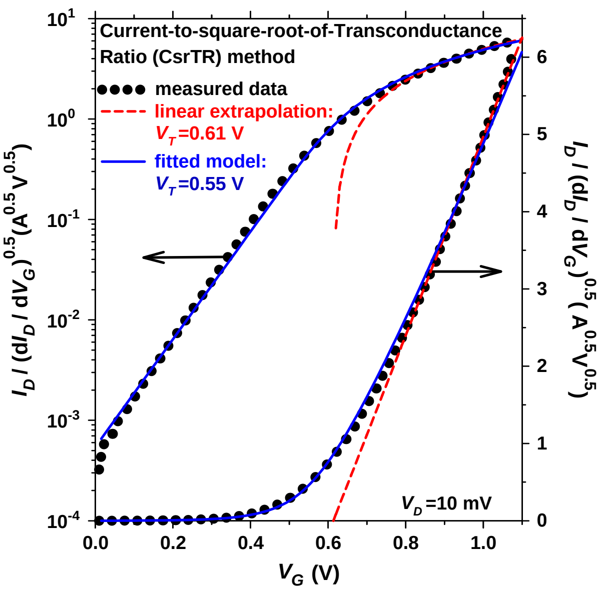

Fig. 13. Current-to-square-root-of-the-Transconductance Ratio method (CsrTR) implemented on the test bulk device in the linear region, measured at $V_D = 10$ mV. This method evaluates V_T from the V_G axis intercept of the curve's Linear Extrapolation (dashed lines). The CsrTR method is improved by using the semi-empiric model (1) fitted to the data (solid lines).

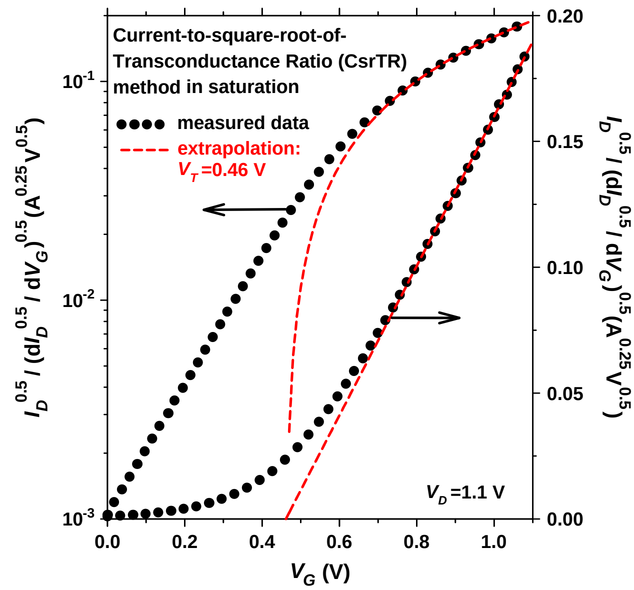

Fig. 14. Current-to-square-root-of-Transconductance Ratio method (CsrTR) implemented on the test bulk device in saturation, measured at $V_D = 1.1$ V. This method evaluates V_T from the V_G axis intercept of the Linear Extrapolation of $I_D^{0.5}/(dI_D^{0.5}/dV_G)^{0.5}$ versus V_G.

$$V_G = n v_{th}\left[\ln\left(-1+\sqrt{1+\frac{4CsrTR^2}{n v_{th} I_o}}\right)+\frac{1}{2}\sqrt{1+\frac{4CsrTR^2}{n v_{th} I_o}}-1/2-\ln(2K)\right]. \tag{5}$$

After extracting the parameters n, K and I_o, the threshold voltage can be obtained analytically by the second derivative method as:

$$V_T = n v_{th}\left[\frac{1}{2}-\ln(2K)\right]. \tag{6}$$

The above formula yields a value of $V_T = 0.55$ V, which is more reasonable than the 0.61 V obtained from the linear extrapolation.

This method can also be used in the saturation region by simply replacing I_D by $I_D^{0.5}$ in the definition of (3):

$$CsrTR_{sat} \equiv \frac{\sqrt{I_D}}{\sqrt{\frac{d\sqrt{I_D}}{dV_G}}}. \tag{7}$$

Fig. 14 shows the implementation of this method on the test bulk device yielding a value of $V_T = 0.46$ V.

2.7. Transition method

This method [56] was inspired by the properties of the integral difference function, D, which had been previously defined for a two-terminal device as [88,89]:

$$D(V,I) \equiv \int_0^I V dI - \int_0^V I dV = VI - 2\int_0^V I dV. \tag{8}$$

This function presents the useful property of eliminating the effect of any linear element (resistance) connected in series with the device. To extract V_T, the drain current is continuously measured from below to above threshold versus V_G with a small constant V_D. Next the following function, G_1, is numerically calculated from the measured data [56]:

$$G_1(V_G, I_D) \equiv \frac{D(V_G, I_D)}{I_D} = (V_G - V_{Gi}) - 2\frac{\int_{V_{Gi}}^{V_G} I_D dV_G}{I_D}, \tag{9}$$

where V_{Gi} represents the lower limit of integration corresponding to a gate voltage well below threshold, usually chosen at $V_{Gi} = 0$.

The reason for this method can be understood by analyzing the following ideal case of a MOSFET piecewise modeled as: $I_D = I_{Leakage}$ for $V_G < V_T$ and I_D is proportional to V_G for $V_G > V_T$. Using the previous simplifying assumption, we observe that: (a) function G_1 presents a discontinuity at V_T; (b) $G_1 = -V_G$ for $V_G < V_T$; and (c) $G_1 = +V_T$ for $V_G > V_T$. Since for a real device such simplifying assumptions are obviously not exactly true, function G_1 will present a maximum due to the mobility degradation and its value will be close to V_T.

A plot of G_1 versus V_G or ln I_D should result in a straight line below threshold, where the current is dominated by diffusion and consequently it is predominantly exponential. As soon as $V_G \to V_T$ function G_1 should drop due to mobility degradation. This is what is observed with the present test device, as shown in Fig. 15. It can be shown that this maximum value of G_1 approaches the V_T value of the device [56]. It should be noted that parasitic resistance and mobility degradation effects influence the shape of the above-threshold G_1, but not significantly its maximum value, unless those effects are highly pronounced. The effect of the parasitic series resistances is not totally eliminated because a MOSFET is not a two-terminal device with terminal current I_D and terminal voltage V_G.

In the saturation region function G_1 becomes:

$$G_{1sat}(V_G, I_D) = (V_G - V_{Gi}) - 2\frac{\int_{V_{Gi}}^{V_G} \sqrt{I_D} dV_G}{\sqrt{I_D}}. \tag{10}$$

Fig. 16 illustrates the application of this method for the saturation region.

2.8. Normalized Mutual Integral Difference (NMID) Method

The Normalized Mutual Integral Difference (NMID) Method was developed by He and coworkers in 2002 [65] and it was also

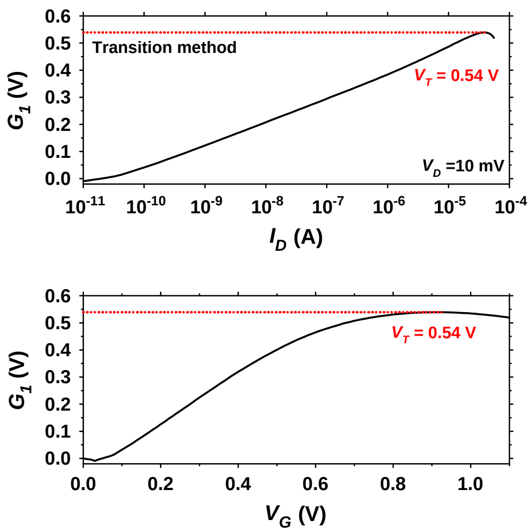

Fig. 15. Transition method implemented on the plot of function G_1, versus either the drain current (upper pane) or the gate voltage (lower pane), of the test bulk device measured at $V_D = 10$ mV. This method evaluates V_T as the value of the G_1 maximum.

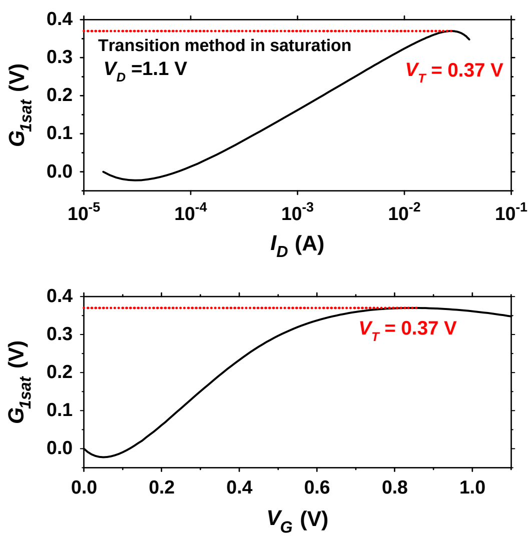

Fig. 16. Transition method implemented on the plot of function G_1, versus either the drain current (upper pane) or the gate voltage (lower pane), of the test bulk device measured in saturation at $V_D = 1.1$ V.

inspired by the integral difference function D [88,89], but in this case normalized by the product $I_D V_G$:

$$D_{normal}(V_G, I_D) \equiv \frac{D(V_G, I_D)}{I_D V_G} = 1 - 2\frac{\int_0^{V_G} I_D dV_G}{I_D V_G}. \tag{11}$$

Accordingly, a plot of D_{normal} versus V_G will present a maximum at $V_G = V_T$. Fig. 17 illustrates the application of this method to the test device producing a $V_T = 0.46$. Notice that the location of the maximum is independent of the constant term "1" which may be removed from (11). A drawback of this method is that the maximum is located in broad region. In the next section we will present an improved version of the NMID method.

For the saturation region, function D_{normal} becomes:

$$D_{normal-sat}(V_G, \sqrt{I_D}) \equiv 1 - 2\frac{\int_0^{V_G} \sqrt{I_D} dV_G}{\sqrt{I_D} V_G}. \tag{12}$$

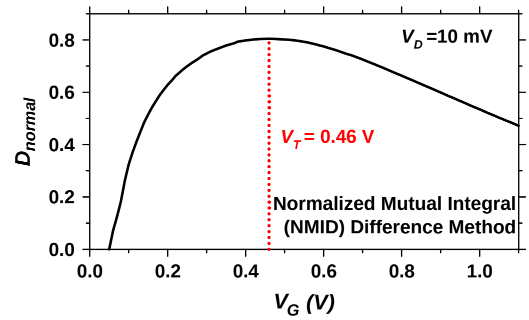

Fig. 17. Normalized Mutual Integral Difference Method implemented on the plot of function D_{normal} versus V_G of the test bulk device measured at $V_D = 10$ mV. This method evaluates the threshold voltage as V_G where D_{normal} is a maximum.

Fig. 18 shows the application of this method to the test device in saturation producing a $V_T = 0.47$ V.

2.9. Normalized Reciprocal H function (NRH) method

Removing the "1" term and the factor "2" from (11), and considering that $I_D \neq 0$ at $V_G = 0$, yields a normalized version of the H function originally proposed in 2001 for extracting the threshold voltage of amorphous thin film MOSFETs [86], and later revised in 2010 to evaluate the sub-threshold slope of MOSFETs [69]:

$$H_{normal}(V_G) = \frac{\int_0^{V_G} I_D(V_g) dV_g}{V_G[I_D - I_D(V_G = 0)]}. \tag{13}$$

We propose that instead of using (13), its reciprocal should be used to produce narrow maxima or minima:

$$H_{nr}(V_G) = \frac{V_g[I_D - I_D(V_G = 0)]}{2\int_0^{V_g} I_D(V_G) dV_G}. \tag{14}$$

A factor of 2 was added to the denominator of (14) to allow a simple graphical interpretation of its meaning. The numerator of (14) divided by 2 is the area of a triangle with a width of V_G and a height of I_D–$I_D(V_G = 0)$. Then, H_{nr} is the ratio of this triangle's area divided by the area under the plot (the integral).

Fig. 19 presents the application of this new method to the test device producing a narrow maximum at $V_G = 0.46$ V. This narrower width represents an improvement on the previous Normalized Mutual Integral Difference Method.

The corresponding function for the saturation region is:

$$H_{nr-sat}(V_G) = \frac{V_G[\sqrt{I_D} - \sqrt{I_D(V_G = 0)}]}{2\int_0^{V_G} \sqrt{I_D} dV_G}. \tag{15}$$

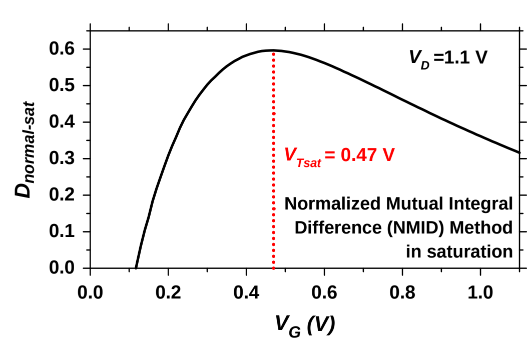

Fig. 18. Normalized Mutual Integral Difference Method implemented on the plot of function $D_{normal-sat}$ versus V_G of the test bulk device in saturation measured at $V_D = 1.1$ V.

Please cite this article in press as: Ortiz-Conde A et al. Revisiting MOSFET threshold voltage extraction methods. Microelectron Reliab (2012), http://dx.doi.org/10.1016/j.microrel.2012.09.015

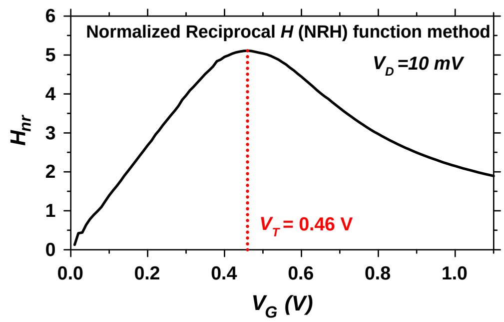

Fig. 19. Normalized Reciprocal H (NRH) function method implemented on the test bulk device in the linear region measured at $V_D = 10$ mV. This method evaluates V_T at the value of V_G where H_{ni} has a maximum.

Fig. 20 illustrates the application of this method to the test device indicating a $V_T = 0.47$ V.

2.10. Transconductance-to-Current-Ratio (TCR) and Reciprocal H function (RH) methods

These methods [31,68,72,73] are based on calculating the following ratio [98]:

$$TCR = \frac{g_m}{I_D} = \frac{dI_D/dV_G}{I_D} = \frac{d\ln(I_D)}{dV_G}. \quad (16)$$

The threshold voltage can be determined as the value of V_G where TCR presents its maximum negative slope. Seemingly inspired on the second-derivative method, Aoyama proposed in 1995 that V_T could be determined as the V_G where $d^2\ln(I_D)/dV_G^2$ has a minimum [45]. This Second Derivative of the Logarithm (SDL) method is also highly sensitive to experimental measurement noise. The recently proposed TCR methods [31,68,72,73] are mathematically related to Aoyama's SDL method since:

$$\frac{d^2\ln(I_D)}{dV_G^2} = \frac{d}{dV_G}\left(\frac{1}{I_D}\frac{dI_D}{dV_G}\right) = \frac{d}{dV_G}\left(\frac{g_m}{I_D}\right) = \frac{dTCR}{dV_G}. \quad (17)$$

Accordingly, the minimum value of $d^2\ln(I_D)/dV_G^2$ occurs at the same V_G where the negative slope of TCR is maximum.

It is worth mentioning that the V_T obtained from the SDL method seems to be more adequate than that obtained from the SD. Rudenko et al. [72,73] have proposed to evaluate V_T at 2/3 of the maximum value of TCR, to lessen the measurement noise related problems that arise when finding the maximum of TCR's negative slope.

Considering that TCR by itself significantly increases experimental noise, especially in weak inversion, an analogous function for low gate bias, was proposed in 2010 based on integration rather than on differentiation to reduce experimental noise [69]:

$$RH(V_G) = \frac{I_D - I_D(V_G = 0)}{\int_0^{V_G} I_D(V_G)dV_G}, \quad (18)$$

where RH is the reciprocal of function H. We now propose that this function could also be used to extract the threshold voltage. Then, V_T can be extracted from the maximum negative slope of function RH.

Fig. 21 shows the implementation of these methods for the present test device. A reasonable value for V_T of about 0.53 V is obtained, if measurement noise and error are reduced before taking the second derivative of the logarithm of the drain current. Rudenko's definition yields $V_T = 0.49$ V. On the other hand, the maximum slope of function RH yields $V_T = 0.55$ V.

Following the same ideas already presented and discussed in Section 2.8 about the Transconductance-to-Current-Ratio (TCR) method, we may also extend this method to extract the threshold voltage in the saturation region using the second derivative of the logarithm of the square root of the drain current (SDLsr). Accordingly, the corresponding function for the saturation region is:

$$RH_{sat}(V_G) = \frac{\sqrt{I_D} - \sqrt{I_D(V_G = 0)}}{\int_0^{V_G}\sqrt{I_D}dV_G}. \quad (19)$$

Fig. 22 shows $d^2\ln(I_D^{0.5})/dV_G^2$ versus V_G in the saturation region with $V_D = 1.1$ V. We observe that the maximum value of $d^2\ln(I_D^{0.5})/dV_G^2$ occurs at about $V_G = 0.44$ V.

Table 1 presents the resulting different threshold voltage values extracted for this device in the linear and saturation regions. All methods except two (the NMID and NRH methods) yield smaller values in the saturation region than in the linear region, as can be observed in the table.

3. Extraction from simulated I_D–V_G characteristics

We additionally carried out 2-D simulations, using the "MOSFet" simulation tool [90], to confirm the validity of the methods

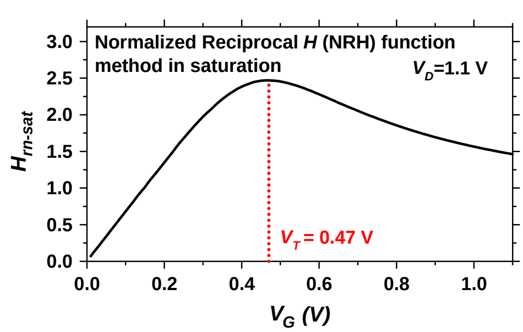

Fig. 20. Normalized Reciprocal H function method implemented on the test bulk device in the saturation region, measured at $V_D = 1.1$ V. This method evaluates V_T at the value of V_G where $H_{nr\text{-}sat}$ has a maximum.

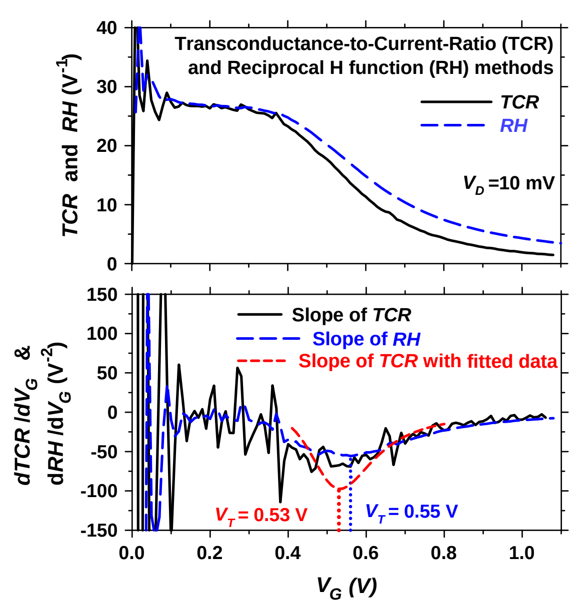

Fig. 21. (Upper pane) Transconductance-to-Current Ratio (TCR) and function RH versus V_G. The threshold voltage is defined at a given fraction of the maximum value. (Lower pane) Derivatives of TCR and RH with respect to V_G. The threshold voltage is defined at the maximum negative value. The derivative of TCR is noisier than the derivative of RH.

Please cite this article in press as: Ortiz-Conde A et al. Revisiting MOSFET threshold voltage extraction methods. Microelectron Reliab (2012), http://dx.doi.org/10.1016/j.microrel.2012.09.015

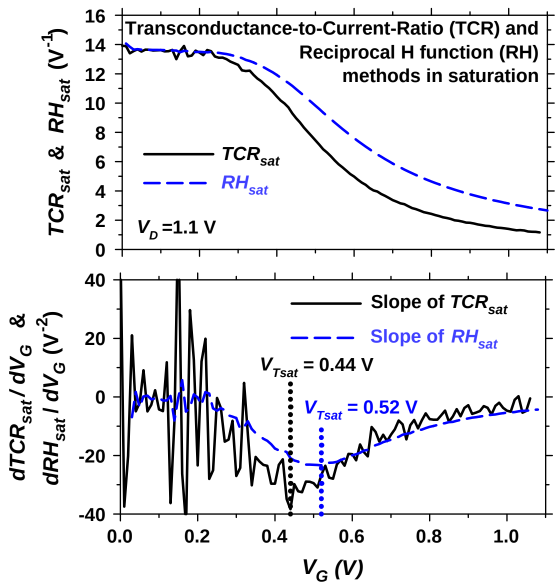

Fig. 22. (Upper pane) Transconductance-to-Current Ratio (TCR_{sat}) and function RH_{sat} versus V_G. in the saturation region. The threshold voltage is defined at a given fraction of the maximum value. (Lower pane) Derivatives of TCR_{sat} and RH_{sat} with respect to V_G. The threshold voltage is defined at the maximum negative value. The derivative of TCR_{sat} is noisier than the derivative of RH_{sat}.

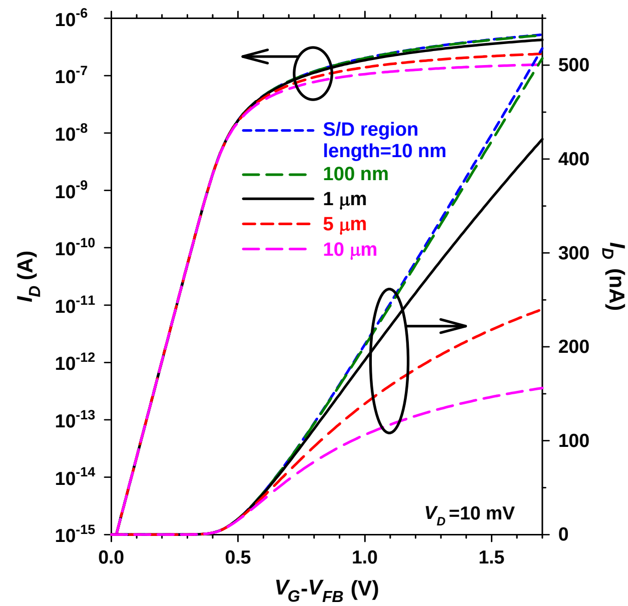

Fig. 23. 2-D simulations of the I_D–V_G transfer characteristics at V_D = 10 mV with S/D regions length varying from 10 nm to 10 μm.

Table 1
Threshold voltage values obtained from several extraction methods for a test short-channel single-crystal bulk device (L_m = 70 nm) biased in the linear and saturation regions.

Method's name	V_T (V) linear region (V_D = 10 mV)	V_{Tsat} (V) saturation region (V_D = 1.1 V)
CC	0.57	0.45
MP	0.35	0.31
LE	0.57	0.41
SD	0.55	0.45
TD	0.48	NA
CsrTR linear	0.61	0.46
CsrTR lambert	0.55	NA*
Transition	0.54	0.37
NMID	0.46	0.47
NRH	0.46	0.47
TCR at 2/3 of maximum value	0.49	NA*
Maximum slope of TCR or SDL	0.53	0.44
RH	0.55	0.52

* NA = not applicable.

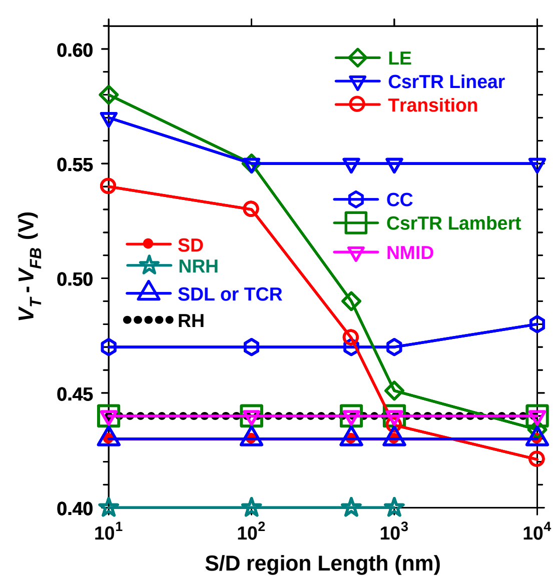

Fig. 24. Threshold voltage values extracted using several methods versus S/D region length (equivalent to a variable series resistance) from the 2-D simulations of Fig. 23.

with respect to the presence of parasitic series resistance. A double-gate MOSFET with n+ polysilicon gate, a 100 μm channel length, a channel doping concentration of 10^{18} cm^{-3}, and symmetrical S/D regions lengths from 10 nm to 10 μm, was simulated for this purpose [99]. The S/D length variation is a simple way to simulate a variable parasitic resistance as it is illustrated in Fig. 23.

Fig. 24 shows the threshold voltages extracted by several methods versus S/D region length for the 2-D simulations of Fig. 23. We conclude from this figure that: (1) The LE and Transition methods are strongly dependent on series resistance; (2) The CsrTR Linear, CC and NRH methods are weakly dependent on series resistance; and (3) The SD, SDL, NMID and CsrTR Lambert methods are independent of series resistance.

Fig. 25 presents 2-D simulations of the same I_D–V_G transfer characteristics for symmetrical S/D regions of 5 μm length at several drain voltages, to study the effect of the value of V_D used for measurement on the different methods.

Fig. 26 shows the threshold voltage values extracted using several methods versus S/D region length for the same 2-D simulations presented in Fig. 25. We conclude from this figure that: (1) The LE, CsrTR Linear, and Transition methods depend strongly on drain voltage; (2) The SD and CsrTR Lambert methods are weakly dependent on drain voltage; and (3) The SDL, NMID, CC (from Bazigos) and NRH methods do not dependent on drain voltage.

4. Extraction in non-crystalline MOSFETs

The transfer characteristics in the weak inversion or sub-threshold region of most MOSFETs may be modeled by an exponential function of V_G of the general form [100]:

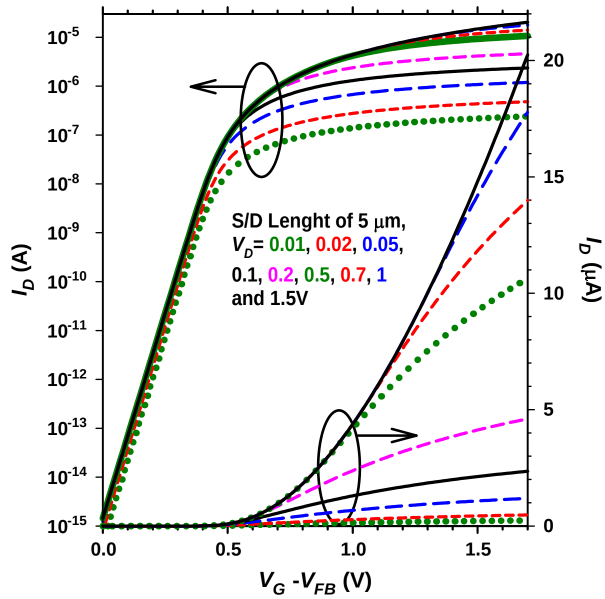

Fig. 25. 2-D simulations of the I_D–V_G transfer characteristics for S/D regions length of 5 μm and several values of drain voltage.

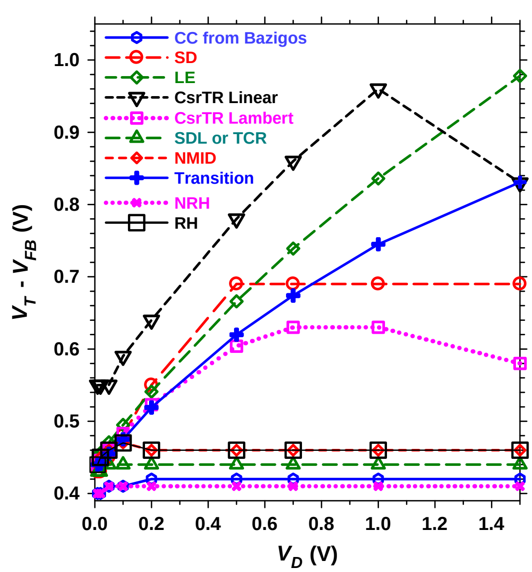

Fig. 26. Threshold voltage values extracted using several methods, versus measurement V_D, for the 2-D simulations.

$$I_{Dw} = I_0 \exp\left(\frac{V_G}{n v_{th}}\right), \tag{20}$$

where I_0 is some global coefficient, $v_{th} = k_BT/q$ is the thermal voltage, and n is the so-called sub-threshold ideality factor. The subscript w in I_{Dw} refers to the drain current in the weak inversion region. On the other hand, the above-threshold drain current of non-crystalline MOSFETs in the strong inversion region at low drain voltage exhibit a super linear behavior, that can be modeled by a power law monomial equation of the form [86]:

$$I_{Ds} = K(V_G - V_{Ts})^m V_D, \tag{21}$$

where K is a global conduction coefficient, m is the monomial's order, usually around 2, which reflects the distribution of states in the conduction band tail, and V_{Ts} is the $I_{Ds} = 0$ intercept, which can be viewed as a "strong inversion region-defined" V_T. Here the subscript s indicates that the equation is valid only in the strong inversion region.

In the next subsections we will first review the single integration method, developed in 2001 [86], and afterwards we will present the double integration method [91], which represents a significant improvement over the single integration method regarding noise reduction.

4.1. Single integration method

This integration-based method was proposed in 2001 for extracting model parameters of non-crystalline MOSFETs biased in the saturation region [86]. It lessens the effect of data noise, in contrast to other derivative-based procedures which inherently worsen the data noise problem. The auxiliary function used in this method was originally proposed in 1999 to extract the model parameters of PN junctions at very low forward voltages [101]. This auxiliary function has the form:

$$H_1(I_D, V_G) = \frac{\int_{V_{Glow}}^{V_G} I_D(V_G) dV_G}{I_D - I_{low}}, \tag{22}$$

where $I_{low} = I_D$ $(V_G = V_{Glow})$, and V_{Glow} is the lower limit of integration.

Substituting (20) into (22) and performing the indicated integration we get for the subthreshold region:

$$H_{1W}(V_G, I_D) = \frac{n v_{th} I_0 \left[\exp\left(\frac{V_G}{n v_{th}}\right) - 1\right]}{I_0 \left[\exp\left(\frac{V_G}{n v_{th}}\right) - 1\right]} = n v_{th}, \tag{23}$$

which equals a constant value that we name H_{weak}. Likewise, substituting (21) into (22) and performing the indicated integration we get for the strong inversion region:

$$H_{1S}(V_G, I_D) = \frac{V_G - V_{Ts}}{m+1}, \tag{24}$$

which is a linear equation on V_G with a reciprocal slope of $m + 1$.

This auxiliary function H_1 defined by (22) can be obtained by numerical integration of the I_D–V_G transfer data measured at a small constant V_D. Then it may be used to extract parameters I_0, n, m, and V_{Ts} by means of (23) and (24). The use of H_1 already is an improvement over derivative-based methods with respect to data noise reduction. However, because H_1 still contains the possibly noisy raw current data in the denominator of (22), in the next subsection we propose the use of another auxiliary function to further improve the noise immunity of the procedure.

4.2. Double Integration Method

The idea suggested by (22) is taken one step further with the purpose of reducing even more the effect of data noise [91]. To that end, let us define another function, H_2, based on successive double integration, to be used as an alternative to (22):

$$\begin{aligned} H_2(V_G, I_D) &\equiv \frac{\int_{V_{Glow}}^{V_G} \int_{V_{Glow}}^{V_G} I_D(V_G) dV_G dV_G}{\int_{V_{Glow}}^{V_G} [I_D(V_G) - I_D(V_G = V_{Glow})] dV_G} \\ &= \frac{\int_{V_{Glow}}^{V_G} \int_{V_{Glow}}^{V_G} I_D(V_G) dV_G dV_G}{\int_{V_{Glow}}^{V_G} I_D(V_G) dV_G - I_{low} V_G}, \end{aligned} \tag{25}$$

Replacing (20) into (25) and solving the integral yields for the sub-threshold region:

$$H_{2w}(V_G, I_D) = \frac{n v_{th} I_{low} \left\{ n v_{th} \left[\exp\left(\frac{V_G}{n v_{th}}\right) - 1 \right] - V_G \right\}}{n v_{th} I_{low} \left[\exp\left(\frac{V_G}{n v_{th}}\right) - 1 \right] - I_{low} V_G} = n v_{th}, \quad (26)$$

which is the exact same result obtained in (23) using H_1. However, as will be confirmed later, the use of H_2 provides better noise immunity than H_1. Replacing the strong inversion transfer Eq. (21) into (25) and solving the integral yields:

$$H_{2S}(V_G, I_D) = \frac{V_G - V_{Ts}}{m + 2}, \quad (27)$$

which is a linear equation on V_G with a reciprocal slope of $m + 2$, in a similar fashion as H_{1s} in (24) is also linear on V_G, except that in this case the reciprocal slope is $m + 2$.

4.3. Procedure for single and double integration methods

The procedure used to extract the parameter values is as follows:

(1) Numerically calculate the first and second integrals versus V_G of the measured $I_D(V_G)$ at low V_D. With these calculate function H_1 using (22) or H_2 by means of (25).
(2) Select an appropriate linear range of V_G in the strong inversion region to fit equation H_{1S} in (24) to the calculated H_1 data, or fit equation H_{2S} in (27) to the calculated H_2 data.
   2a. Extract the values of m and V_{Ts} from the linear fit.
   2b. Calculate K with (21) using the two extracted values of of m and V_{Ts}.
(3) Determine H_{weak} as the value of H_1, or H_2, in a range of the weak inversion region where it remains approximately constant.
(4) Calculate the phenomenological V_T as the value of V_G corresponding to the intersection of H_{weak} and the corresponding H_{1S} or H_{2S}.

4.4. Parameter extraction

Both extraction procedures were applied to experimental data of polycrystalline silicon nanowire n-channel MOSFETs [91], fabricated using a process similar to that reported in Ref. [102]. Three devices with the following makeup were used: Undoped poly-Si NW body with a rectangular cross section of 60 nm × 18 nm, channel lengths (L_m) of 0.4, 1.0, and 2.0 μm, n$^+$ polysilicon gate with 10^{21} cm^{-3} doping, gate SiO_2 oxide thickness of 20 nm, and S/D doping density of 5×10^{20} cm^{-3}. The measured transfer and output characteristics of three transistors with different mask channel lengths are presented together in Fig. 27 at V_D = 10 mV and V_G = 2.5 V respectively.

The first step in the procedure is to calculate functions H_1 and H_2 from the measured data using (22) and (25). The results for L_m = 0.4 μm at V_D = 10 mV, with V_{Glow} = 0, is plotted in Fig. 28a. The figure shows that the double-integral H_2 has significantly better noise reduction than the single-integral H_1. The main disadvantage of H_2 with respect to H_1 consists in that it requires one additional integration step. It is worth mentioning that the extraction of V_T in non-crystalline MOSFETs is more conveniently performed in the saturation region where both methods offer improved noise reduction.

Notice that in Fig. 28a the weak inversion below threshold H_{1W} and H_{2W} have approximately the same value, as expected from (23) and (26), although the curve corresponding to H_2 is less noisy. However, despite H_{1S} and H_{2S} having the same shape above-threshold, they have different slopes in this region, as expected from the

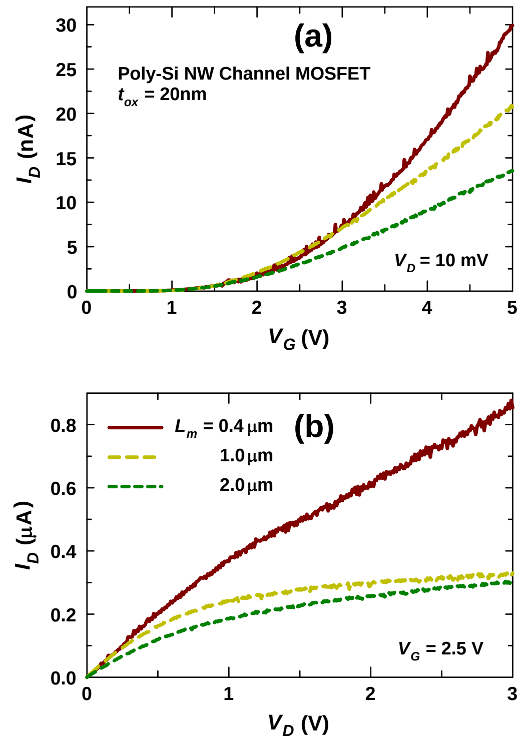

Fig. 27. Transfer (a) and output (b) characteristics of the experimental poly-Si nanowire n-channel MOSFETs, with L_m = 0.4, 1.0 and 2.0 μm gate lengths.

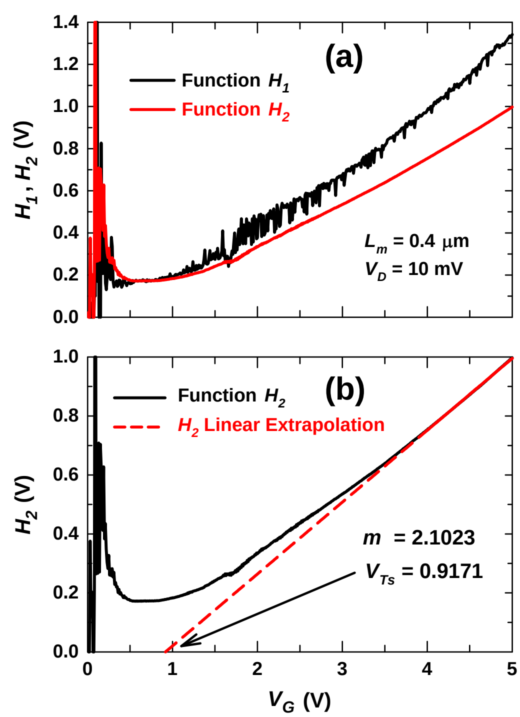

Fig. 28. (a) Plot of both H_1 and H_2 functions versus V_G, to illustrate the noise reduction effect obtained by using H_2. (b) Plot of H_2 versus V_G for device with L_m = 0.4 μm and V_D = 10 mV, and its Linear Extrapolation (red dashed line) used to determine the value of V_{Ts} as the intersection with the V_G-axis. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

$m + 1$ and $m + 2$ reciprocal slope behaviors dictated by (24) and (27). The curve corresponding to H_{2S} is also visibly less noisy.

Next, an appropriate V_G range is selected in the strong inversion region to extract the parameters m and V_{Ts} by fitting Eq. (27) to the corresponding segment of H_{2S}. This function is plotted in Fig. 28b together with the linear extrapolation of its strong inversion region. The values extracted from the straight line are $m = 2.1023$, and $V_{Ts} = 0.9171$ V.

The value of K is then calculated using (21) in the same range, with the extracted values of m and V_{Ts}. The result is shown in Fig. 29. Notice that K looks fairly constant at a mean value of $K = 158.78$ nA/V$^{(m+1)}$, for the chosen V_G range. The procedure's

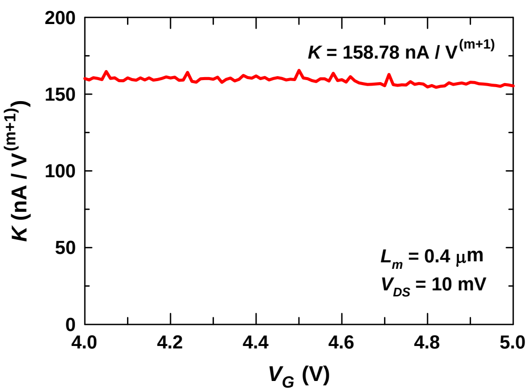

Fig. 29. Plot of K versus V_G as calculated from (21), using the extracted values of m and V_{Ts} for the device with $L_m = 0.4$ μm at $V_D = 10$ mV. The value of K shown corresponds to the mean value of the curve.

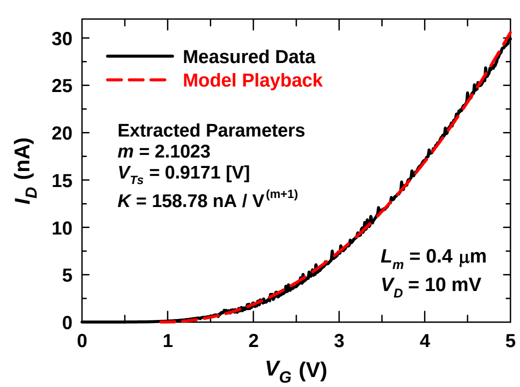

Fig. 30. Measured transfer characteristic and model Playback (red dashed line) resulting from the extracted parameters. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

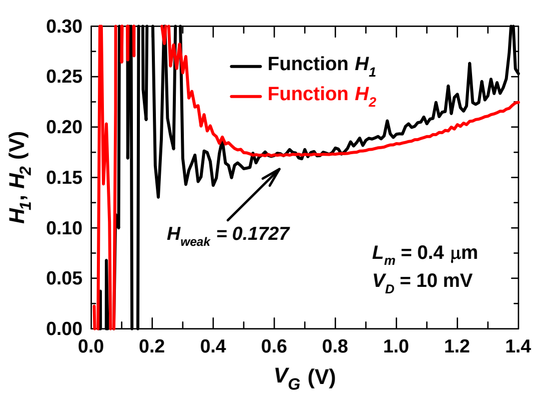

Fig. 31. Close up view of the subthreshold H_1 and H_2 functions. From this region, a mean value of $H_{weak} = 0.1727$ is found.

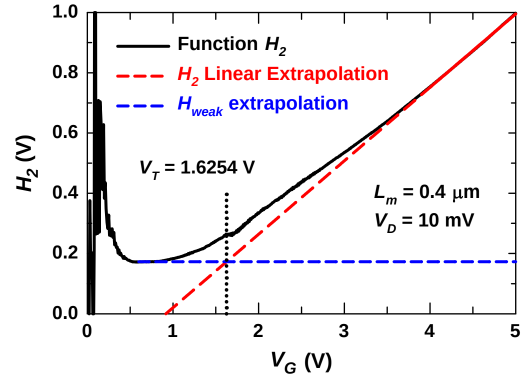

Fig. 32. H_2 versus V_G and its two asymptotic Linear Extrapolations: Strong (oblique straight red dashed line) and Weak (horizontal blue dashed line) regions. The value of V_G at which the intersection occurs, corresponds to V_T. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

effectiveness is confirmed by Fig. 30, which presents the measured transfer characteristic together with the model playback, calculated with (21) using the extracted values of m, V_{Ts} and K, for the device of $L_m = 0.4$ μm at $V_D = 10$ mV.

Recall that V_{Ts} is the $I_{Ds} = 0$ intercept, which has been referred to as the "strong inversion region-defined" V_T. Based on this, we propose that a more phenomenological definition of threshold voltage, V_T, for these devices could be the weak inversion-to-strong inversion transition gate voltage. In order to find it, the value of the sub-threshold H_{weak} must be determined. Fig. 31 presents a close-up view of H_2 in a range of low V_G. We see that function H_2 is approximately constant from $V_G = 0.6$ V to 0.8 V, and has a mean value of $H_{weak} = 0.1727$. This phenomenological threshold voltage is obtained as the value of V_G where H_{weak} intersects the linear extrapolation of the strong inversion region of H_2 (H_{2S}). A value of $V_T = 1.6254$ V is the result for the device with $L_m = 0.4$ μm at $V_D = 10$ mV. Fig. 32 shows this last step of the procedure.

5. Conclusions

We have presented, reviewed and critically compared several extraction methods currently used to determine the threshold voltage value of bulk single-crystal and non-crystalline thin film MOSFETs from their drain current versus gate voltage transfer characteristics measured either in the linear or the saturation operation regimes. The relative performance of the reviewed methods was illustrated and compared under the same conditions by applying them to the measured characteristics of real test devices: (a) an enhancement-mode n-channel single-crystal silicon bulk MOSFET with state-of-the-art 70 nm mask channel length, and (b) an experimental polycrystalline silicon nanowire n-channel MOSFET.

A total of twelve methods were applied to the single-crystal bulk device. The several resulting threshold voltage values for this device were presented in tabular form for quick comparison purposes. Six out of the twelve methods produce very similar results, of about 0.55 V in the linear region, and six yield a threshold voltage value of about 0.45 V in the saturation region. The different values of linear region and saturation region threshold voltage values is mainly due to the square root operation used to extract the saturation region threshold voltage, and to a lesser extent to the value of V_D used for its measurement, as suggested by 2D simulations. The simulations also suggest that second derivative of the logarithm (SDL) of the drain current, better known as the Transconductance-to-Current-Ratio (TCR), is the method that is more immune to the presence of parasitic series resistance and

Please cite this article in press as: Ortiz-Conde A et al. Revisiting MOSFET threshold voltage extraction methods. Microelectron Reliab (2012), http://dx.doi.org/10.1016/j.microrel.2012.09.015

to variations of V_D. The Reciprocal H function (RH) method is an attractive alternative to the TCR method to lessen the effect of measurement noise. In the line of using integration to reduce the effect of measurement noise, two additional integration-based methods were reviewed and tested on a non-crystalline MOSFET.

References

[1] Liou JJ, Ortiz-Conde A, García-Sánchez FJ. Analysis and design of MOSFETs: Modeling, Simulation and Parameter Extraction. New York: Springer; 1998. ISBN: 978-0-412-14601-5.
[2] Ortiz-Conde A, García-Sánchez FJ, Liou JJ. An overview of parameter extraction in field effect transistors. Acta Científica Venezolana 2000;51:176–87.
[3] Ortiz-Conde A, García-Sánchez FJ, Liou JJ, Cerdeira A, Estrada M, Yue Y. A review of recent MOSFET threshold voltage extraction methods. Microelectron Reliab 2002;42:583–96.
[4] Terada K, Nishiyama K, Hatanaka KI. Comparison of MOSFET-threshold-voltage extraction methods. Solid-State Electron 2001;45:35–40.
[5] Garcia-Sánchez FJ, Ortiz-Conde A, Muci J. Understanding threshold voltage in undoped-body MOSFETs: an appraisal of various criteria. Microelectron Reliab 2006;46:731–42.
[6] Schroeder DK. Semiconductor material and device characterization. 3rd ed. New York: Wiley; 2006.
[7] Richman P. Theoretical threshold voltages for MOS field effect transistors. Solid-State Electron 1968;11(9):869–76.
[8] Doria Trevisoli R, Trevisoli Doria R, de Souza M, Pavanello MA. Threshold voltage in junctionless nanowire transistors. Semicond Sci Technol 2011;26:105009.
[9] Liu L, Mohata D, Datta S. Scaling length theory of double-gate interband tunnel field-effect transistors. IEEE Trans Electron Dev 2012;59:902–8.
[10] Dutta JC, Warjri PS. Threshold voltage and I-V characteristics of cylindrical, surrounding-electrolyte ISFET. In: Int Conf Dev Circ Syst (ICDCS); 2012. p. 678–80.
[11] Bekaddour A, Pala MG, Chabane-Sari N, Ghibaudo G. Deterministic method to evaluate the threshold voltage variability induced by discrete trap charges in Si-nanowire FETs. IEEE Trans Electron Dev 2012;59:1462–7.
[12] He H, Deng W, He J, Zheng X. On the grain boundary barrier height and threshold voltage of undoped polycrystalline silicon thin-film transistors. In: 12th Intl Workshop Junction Technol (IWJT); 2012. p. 160–3.
[13] Oudwan M, Abramov A, Daineka D, Roca i Cabarrocas P. Mechanisms of threshold voltage shift in polymorphous and microcrystalline silicon bottom gate thin-film transistors. J Display Technol 2012;8:23–6.
[14] Kahng D. A historical perspective on the development of MOS transistors and related devices. IEEE Trans Electron Dev 1976;23:655–7.
[15] Ihantola HKJ, Moll JL. Design theory of a surface field-effect transistor. Solid-State Electron 1964;7:423–30.
[16] Fotty D. MOSFET modeling with SPICE: principles and practice. Englewood Cliffs, N.J.: Prentice-Hall; 1997.
[17] Pao HC, Sah CT. Effects of diffusion current on characteristics of metal-oxide (insulator)-semiconductor transistors. Solid-State Electron 1966;9:927–37.
[18] Gildenblat G, Li X, Wu W, Wang H, Jha A, Van Langevelde R, et al. PSP: an advanced surface-potential-based MOSFET model for circuit simulation. IEEE Trans Electron Dev 2006;53:1979–93.
[19] Miura-Mattausch M, Feldmann U, Rahm A, Bollu M, Savignac D. Unified complete MOSFET model for analysis of digital and analog circuits. IEEE Trans Computer-Aided Design 1996;15:1–7.
[20] Brews JR. A charge-sheet model of the MOSFET. Solid-State Electron 1978;21:345–55.
[21] Baccarani G, Rudan M, Spadini G. Analytical IGFET model including drift and diffusion currents. IEE J Solid-State Electron Dev 1978;2:62–8.
[22] Miranda M. When every atom counts. IEEE Spectr 2012;49:32–7.
[23] Damrongplasit N, Zamudio L, Balasubramanian S. Threshold voltage and DIBL variability modeling for SRAM and analog MOSFETs. In: Symposium on VLSI Technology (VLSIT); 2012. p. 187–8.
[24] A User's Guide to MASTAR 4 – Model for Assessment of cmoS Technologies and Roadmaps. <http://www.itrs.net/Links/2011ITRS/MASTAR2011/instructions.pdf>.
[25] Tudor B, Wang J, Chen Z, Tan R, Liu W, Lee F. An accurate MOSFET aging model for 28 nm integrated circuit simulation. Microelectron Reliab 2012;52:1565–70.
[26] Kaczer B, Franco J, Toledano-Luque M, Roussel PJ, Bukhori MF, Asenov A, et al. The relevance of deeply-scaled FET threshold voltage shifts for operation lifetimes. IEEE Int Reliab Phys Symp (IRPS) 2012;5A:2.1–6.
[27] Sato T, Awano H, Shimizu H, Tsutsui H, Ochi H. Statistical observations of NBTI-induced threshold voltage shifts on small channel-area devices. In: 13th Int Symp Quality Electron Design (ISQED); 2012. p. 306–11.
[28] Akers LA, Sánchez JJ. Threshold voltage models of short, narrow and small geometry MOSFET's: a review. Solid State Electron 1982;25:621–41.
[29] Boudinet D, Le Blevennec G, Serbutoviez C, Verilhac JM, Yan H, Horowitz G. Contact resistance and threshold voltage extraction in n-channel organic thin film transistors on plastic substrates. J Appl Phys 2009;105:084510.
[30] Giraudet L, Simonetti O. Threshold voltage and turn-on voltage in organic transistors: sensitivity to contact parasitic. Organic Electron Phys Mat Appl 2011;12:219–25.
[31] Siebel OF, Schneider MC, Galup-Montoro C. MOSFET threshold voltage: definition, extraction, and some applications. Microelectron J 2012;43:329–36.
[32] Ortiz-Conde A, Rodríguez J, García-Sánchez FJ, Liou JJ. An improved definition for modeling the threshold voltage of MOSFETS. Solid-State Electron 1998;42:1743–6.
[33] Salcedo JA, Ortiz-Conde A, García-Sánchez FJ, Muci J, Liou JJ, Yue Y. New approach for defining the threshold voltage of MOSFETs. IEEE Trans Electron Dev 2001;48:809–13.
[34] Benson J, D'Halleweyn NV, Redman-White W, Easson CA, Uren MJ, Faynot O, et al. A physically based relation between extracted threshold voltage and surface potential flat band voltage for MOSFET compact modeling. IEEE Trans Electron Dev 2001;48:1019–21.
[35] Medury AS, Bhat KN, Bhat N. Threshold voltage modeling under size quantization for ultra-thin silicon double-gate metal-oxide-semiconductor field-effect transistor. J Appl Phys 2012;112:024513.
[36] Wong HS, White MH, Krutsick TJ, Booth RV. Modeling of transconductance degradation and extraction of threshold voltage in thin oxide MOSFET's. Solid-State Electron 1987;30:953.
[37] Ghibaudo G. New method for the extraction of MOSFET parameters. Electron Lett 1988;24:543–5.
[38] Jain S. Measurement of threshold voltage and channel length of submicron MOSFETs. IEE Proc Cir Dev Syst 1988;135:162.
[39] El-Kareh B, Tonti WR, Titcomb SL. A submicron MOSFET parameter extraction technique. IBM J Res Develop 1990;34:243–9.
[40] Yan ZX, Deen MJ. Physically-based method for measuring the threshold voltage of MOSFETs. IEE Proc G - Circ Dev Syst 1991;138:351–7.
[41] McAndrew CC, Layman PA. MOSFET effective channel length, threshold voltage, and series resistance determination by robust optimization. IEEE Trans Electron Dev 1992;39:2298–311.
[42] Taur Y, Zicherman DS, Lombardi DR, Restle PJ, Hsu CH, Hanafi HY, et al. A new "shift and ratio" method for MOSFET channel-length extraction. IEEE Electron Dev Lett 1992;13:267–9.
[43] Corsi F, Marzocca C, Portacci GV. New experimental technique for fast and accurate MOSFET threshold extraction. Electron Lett 1993;29:1358–60.
[44] Galup-Montoro C, Schneider MC, Koerich AL, Pinto RLO. MOSFET threshold extraction from voltage-only measurements. Electron Lett 1994;30:1458–9.
[45] Aoyama K. A method for extracting the threshold voltage of MOSFET based on current components. Simul Semicond Dev Proc 1995;6:118–21.
[46] Fikry W, Ghibaudo G, Haddara H, Cristoloveanu S, Dutoit M. Method for extracting deep submicrometer MOSFET parameters. Electron Lett 1995;31:762–4.
[47] Karlsson PR, Jeppson KO. An efficient method for determining threshold voltage, series resistance and effective geometry of MOS transistors. IEEE Trans Semicond Manufact 1996;9:215–22.
[48] Tsay JH, Liu SI, Wu YP. A simple and accurate method to measure the threshold voltage of a MOSFET using MOS active attenuator. Int J Electron 1996;81:49–58.
[49] Katto H. Device parameter extraction in the linear region of MOSFET's. IEEE Electron Dev Lett 1997;18:408–10.
[50] Ortiz-Conde A, Gouveia E, Liou JJ, Hassan MR, García-Sánchez FJ, De Mercato G, et al. A new approach to extract the threshold voltage of MOSFETs. IEEE Trans Electron Dev 1997;44:1523–8.
[51] Tsuno M, Suga M, Tanaka M, Shibahara K, Miura-Mattausch M, Hirose M. Reliable threshold voltage determination for sub-0.1 μm gate length MOSFETs. In: Proc Asia South Pacific Conf; 1998. p. 111–6.
[52] Lau MM, Chiang CYT, Yeow YT, Yao ZQ. Measurement of V/sub T/and L/sub eff/using MOSFET gate-substrate capacitance. In: Proc Int Conf Microelectron Test Struct; 1999. p. 152–5.
[53] Tsuno M, Suga M, Tanaka M, Shibahara K, Miura-Mattausch M, Hirose M. Physically-based threshold voltage determination for MOSFETs of all gate lengths. IEEE Trans Electron Dev 1999;46:1429–34.
[54] Zhou X, Lim KY, Lim D. A simple and unambiguous definition of threshold voltage and its implications in deep-submicron MOS device modeling. IEEE Trans Electron Dev 1999;46:807–9.
[55] Dobrescu L, Petrov M, Dobrescu D, Ravariu C. Threshold voltage extraction methods for MOS transistors. In: Proc Int Semicond Conf; 2000. p. 371–4.
[56] García-Sánchez FJ, Ortiz-Conde A, Mercato GD, Salcedo JA, Liou JJ, Yue Y. New simple procedure to determine the threshold voltage of MOSFETs. Solid-State Electron 2000;44:673–5.
[57] Tan C, Xu M, Wang Z. Proportional difference operator method and its application in studying subthreshold behavior of MOSFETs. Solid-State Electron 2000;44:1059–67.
[58] Wang J, Xu M, Tan C. An accurate relationship for determining the key parameters of MOSFETs by proportional difference operator meted. Solid-State Electron 2000;44:959–62.
[59] Cretu B, Boutchacha T, Ghibaudo G, Balestra F. New ratio method for effective channel length and threshold voltage extraction in MOS transistors. Electron Lett 2001;37:717–9.
[60] Lau MM, Chiang CYT, Yeow YT, Yao ZQ. A new method of threshold voltage extraction via MOSFET gate-to-substrate capacitance measurement. IEEE Trans Electron Dev 2001;48:1742–4.

Please cite this article in press as: Ortiz-Conde A et al. Revisiting MOSFET threshold voltage extraction methods. Microelectron Reliab (2012), http://dx.doi.org/10.1016/j.microrel.2012.09.015

[61] Ortiz-Conde A, García-Sánchez FJ, Cerdeira A, Estrada M, Flandre D, Liou JJ. A procedure to extract mobility degradation, series resistance and threshold voltage of SOI MOSFETs in the saturation region. In: Sixth Int Conf Solid-State Integr Circ Technol. Shanghai, China; 2001.
[62] Ortiz-Conde A, García-Sánchez FJ, Cerdeira A, Estrada M, Flandre D, Liou JJ. A method to extract mobility degradation and total series resistance of fully-depleted SOI MOSFETs. IEEE Trans Electron Dev 2002;49:82–8.
[63] Wong JS, Ma JG, Yeo KS, Do MA. A new approach for the extraction of threshold voltage for MOSFETs. Mod Simul of Microsyst (MSM) 2001:534–7.
[64] Zhou X, Lim KY, Qian W. Threshold voltage definition and extraction for deep-submicron MOSFETs. Solid-State Electron 2001;45:507–10.
[65] He J, Xi X, Chan M, Cao K, Hu C, Li Y, et al. Normalized mutual integral difference method to extract threshold voltage of MOSFETs. IEEE Electron Dev Lett 2002;23:428–30.
[66] Picos R, Roca M, Íñiguez B, García-Moreno E. A new procedure to extract the threshold voltage of MOSFETs using noise-reduction techniques. Solid-State Electron 2003;47:1953–8.
[67] Picos R, Calvo O, Íñiguez B, García-Moreno E, García R, Estrada M. Optimized parameter extraction using fuzzy logic. Solid-State Electron 2007;51:683–90.
[68] Flandre D, Kilchytska V, Rudenko T. Gm/Id method for threshold voltage extraction applicable in advanced MOSFETs with nonlinear behavior above threshold. IEEE Electron Dev Lett 2010;31:930–2.
[69] Ortiz-Conde A, García-Sánchez FJ, Liou JJ, Ho C-S. Integration-based approach to evaluate the sub-threshold slope of MOSFETs. Microelectron Reliab 2010;50:312–5.
[70] Subramanian N, Ghibaudo G, Mouis M. Parameter extraction of nano-scale MOSFETs using modified Y function method. In: Proc Eur Solid State Dev Res Conf (ESSDERC); 2010. p. 309–12.
[71] Bazigos A, Bucher M, Assenmacher J, Decker S, Grabinski W, Papananos Y. An adjusted constant-current method to determine saturated and linear mode threshold voltage of MOSFETs. IEEE Trans Electron Dev 2011;58:3751–8.
[72] Rudenko T, Kilchytska V, Arshad MKM, Raskin J-P, Nazarov A, Flandre D. On the MOSFET threshold voltage extraction by transconductance and transconductance-to-current ratio change methods: Part I-Effect of gate-voltage-dependent mobility. IEEE Trans Electron Dev 2011;58:4172–9.
[73] Rudenko T, Kilchytska V, Arshad MKM, Raskin J-P, Nazarov A, Flandre D. On the MOSFET threshold voltage extraction by transconductance and transconductance-to-current ratio change methods: Part II-Effect of drain voltage. IEEE Trans Electron Dev 2011;58:4180–8.
[74] Álvarez-Botero G, Torres-Torres R, Murphy-Arteaga R. Using S-parameter measurements to determine the threshold voltage, gain factor, and mobility degradation factor for microwave bulk-MOSFETs. Microelectron Reliab 2011;51:342–9.
[75] Cerdeira A, Estrada M, García R, Ortiz-Conde A, García-Sánchez FJ. New procedure for the extraction of basic a-Si:H TFT model parameters in the linear and saturation regions. Solid-State Electron 2001;45:1077–80.
[76] Chang-Liao KS, Chang HM. Extraction method of threshold voltage and transconductance to asses radiation effects on MOS circuits. J Nucl Sci Technol 1999;36:630–2.
[77] Jomaah J, Fadlallah M, Ghibaudo G. DC characterization of different advanced MOSFET architectures. Adv Mat Res 2011;324:407–10.
[78] Natali D, Fumagalli L, Sampietro M. Modeling of organic thin film transistors: effect of contact resistances. J Appl Phys 2007;101:014501.
[79] White MH, Cricchi JR. Complementary MOS transistors. Solid-State Electron 1966;9:991–1008.
[80] Das MB. Physical limitations of MOS structures. Solid-State Electron 1969;12:305–36.
[81] Sah CT. Characteristics of metal-oxide-semiconductor transistors. IEEE Trans Electron Dev 1964;11:324–45.
[82] Lee HG, Oh SY, Fuller G. A simple and accurate method to measure the threshold voltage of an enhancement-mode MOSFET. IEEE Trans Electron Dev 1982;29:346–8.
[83] Cilimgiroglu U, Hoon SK. An accurate self-bias threshold voltaje extractor using differential difference feedback amplifier. IEEE Int Symp Cir Syst; 2000. p. V209–12.
[84] Thomas F, Holman WT. MOSFET threshold voltage extractor circuits based on square-law behavior. In: IEEE 42nd Midwest Symp Cir Syst, vol. 2; 2000. p. 1118–21.
[85] Tsuji K, Terada K, Takeda R, Tsunomura T, Nishida A, Mogami T. Threshold voltage variation extracted from MOSFET C-V curves by charge-based capacitance measurement. In: IEEE Int Conf Microelectron Test Struct; 2012. p. 82–6.
[86] Ortiz-Conde A, Cerdeira A, Estrada M, García Sánchez FJ, Quintero R. A simple procedure to extract the threshold voltage of amorphous thin film MOSFETs in the saturation region. Solid-State Electron 2001;45:663–7.
[87] Vadasz L, Grove AS. Temperature dependence of MOS transistor characteristics below saturation. IEEE Trans Electron Dev 1966;13:863–6.
[88] García-Sánchez FJ, Ortiz-Conde A, De Mercato G, Liou JJ, Recht L. Eliminating parasitic resistances in parameter extraction of semiconductor device models. In: Proc First IEEE Int Caracas Conf Dev Cir Sys (ICCDCS); 1995. p. 298.
[89] García-Sánchez FJ, Ortiz-Conde A, Liou JJ. A parasitic series resistance-independent method for device-model parameter extraction. IEE Proc Cir Dev Sys 1996;143:68.
[90] Mannino M, Ahmed SS, Klimeck G, Vasileska D, Wang X, Pal H, et al. "MOSFet"; 2012. doi:10254/nanohub-r452.18.
[91] Ortiz-Conde A, Latorre Rey AD, Liu W, Chen W-C, Lin H-C, Liou JJ, et al. Parameter extraction in polysilicon nanowire MOSFETs using new double integration-based procedure. Solid-State Electron 2010;54:635–41.
[92] García-Sánchez FJ, Ortiz-Conde A, De Mercato G. The Development of integration-based methods to extract parameters of two-terminal device models. In: 9th Int Conf Solid-State Integr-Cir Technol (ICSICT) Beijing, China; 2008. p. 432–5.
[93] Ortiz-CondeA, García Sánchez FJ, Salazar R. On integration-based Methods for MOSFET model parameter extraction. In: 9th Int Conf Solid-State Integr-Cir Technol (ICSICT) Beijing, China; 2008. p. 428–31.
[94] Fjeldly TA, Ytterdal T, Shur M. Introduction to device modeling and circuit simulation. New York: Wiley; 1998.
[95] Ortiz-Conde A, García-Sánchez FJ, Guzmán M. Exact analytical solution of channel surface potential as an explicit function of gate voltage in undoped-body MOSFETs using the lambert w function and a threshold voltage definition the refrom. Solid-State Electron 2003;47:2067–74.
[96] Ortiz-Conde A, Ma Y, Thomson J, Santos E, Liou JJ, García-Sánchez FJ, et al. Direct extraction of semiconductor device parameters using lateral optimization method. Solid-State Electron 1999;43:845–8.
[97] Yang H, Inokawa H. A differential smoothing technique for the extraction of MOSFET threshold voltage using extrapolation in the linear region. Solid-State Electron 2012;76:5–7.
[98] Tsividis Y. Moderate inversion in MOS devices. Solid-State Electron 1982;25:1099–104.
[99] Ortiz-Conde A, García-Sánchez FJ. A rigorous classical solution for the drain current of doped symmetric double-gate MOSFETs. IEEE Trans Electron Dev 2012;59:2390–5.
[100] Liou JJ, Shireen R, Ortiz-Conde A, García-Sánchez FJ, Cerdeira A, Gao X, et al. Influence of polysilicon-gate depletion on the subthreshold behavior of submicron MOSFETs. Microelectron Reliab 2002;42:343–7.
[101] Ranuarez JC, García-Sánchez FJ, Ortiz-Conde A. Procedure for the determination of diode model parameters at very low forward voltage. Solid-State Electron 1999;43:2129–33.
[102] Hsu H-H, Liu T-W, Chan L, Lin C-D, Huang T-Y, Lin H-C. Fabrication and characterization of multiple-gated poly-SI nanowire thin-film transistors and impacts of multiple-gate structures on device fluctuations. IEEE Trans Electron Dev 2008;55:3063–9.

Please cite this article in press as: Ortiz-Conde A et al. Revisiting MOSFET threshold voltage extraction methods. Microelectron Reliab (2012), http://dx.doi.org/10.1016/j.microrel.2012.09.015